AMD Xilinx - XC2S50-5TQG144C Datasheet

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Applications of Embedded - FPGAs

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Details	
Product Status	Active
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	92
Number of Gates	50000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s50-5tqg144c

Spartan-II FPGA Family: Introduction and Ordering Information

DS001-1 (v2.8) June 13, 2008

Product Specification

Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

Table 1: **Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	92	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information.
10/31/00	2.1	Removed Power down feature.
03/05/01	2.2	Added statement on PROMs.
11/01/01	2.3	Updated Product Availability chart. Minor text edits.
09/03/03	2.4	Added device part marking.
08/02/04	2.5	Added information on Pb-free packaging options and removed discontinued options.
06/13/08	2.8	Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

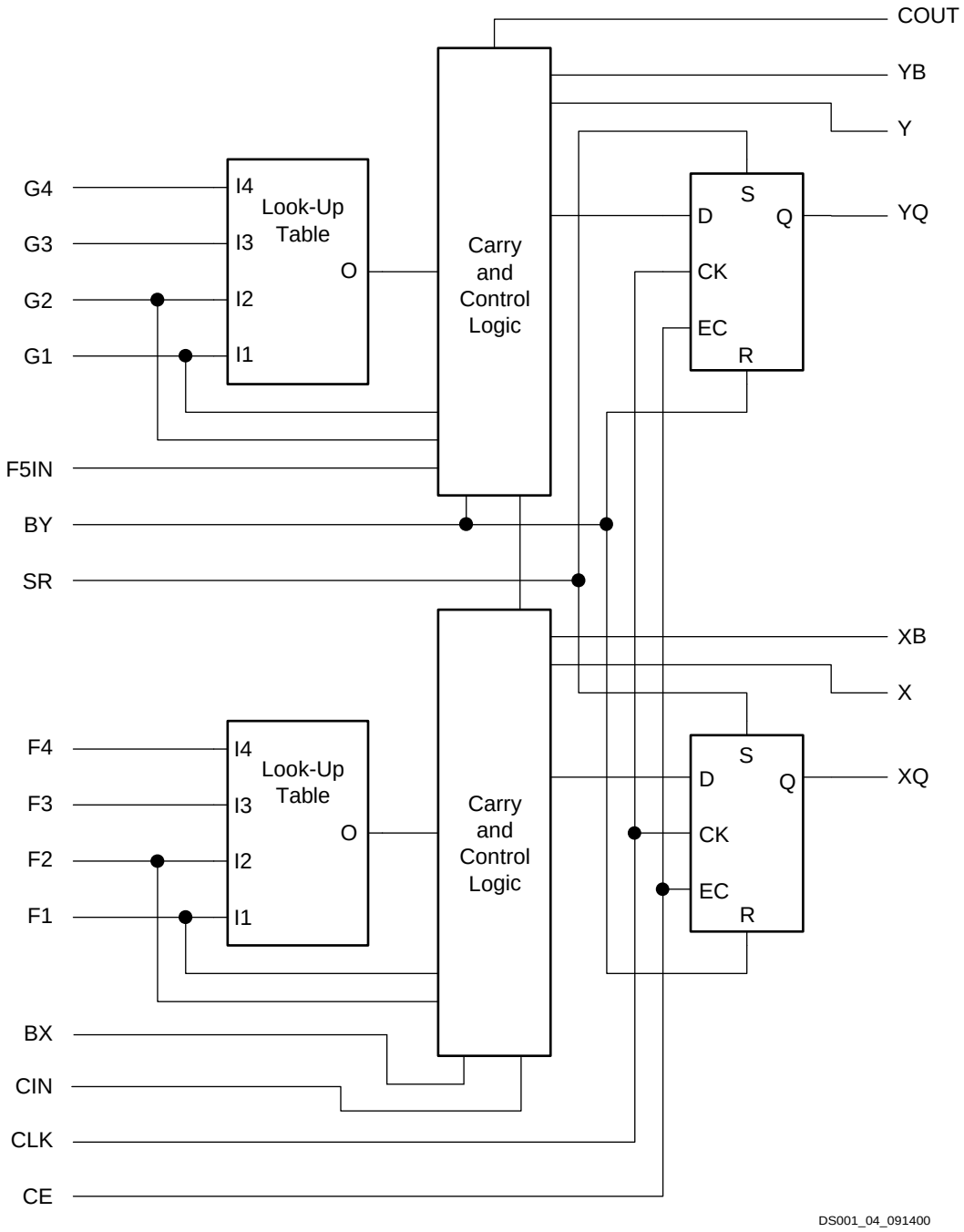


Figure 4: **Spartan-II CLB Slice** (two identical slices in each CLB)

Storage Elements

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 7: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx® reserved instructions

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

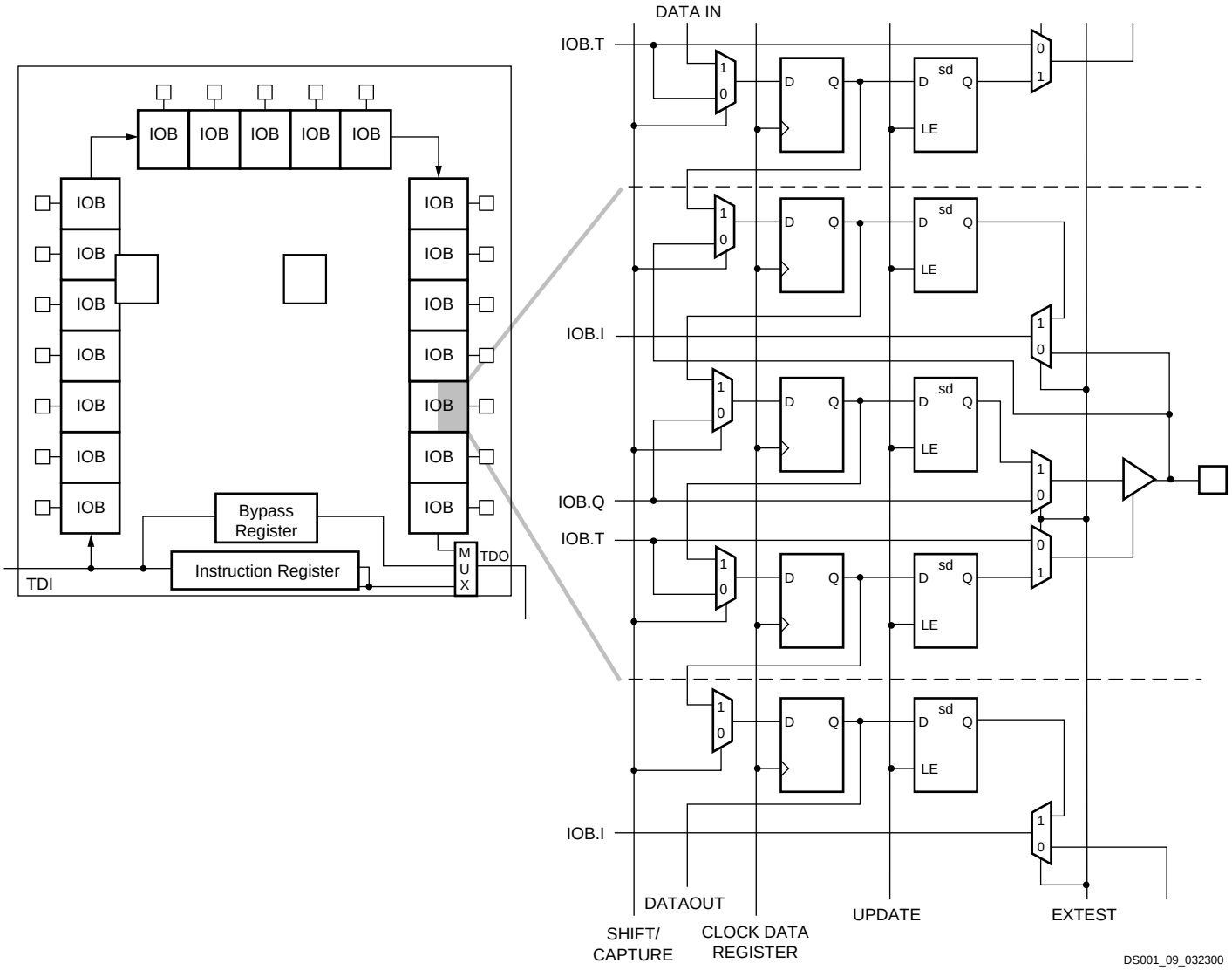


Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

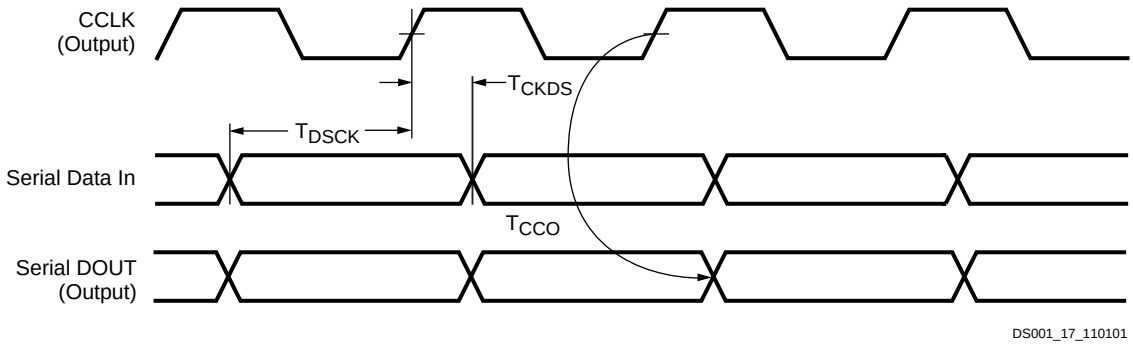
From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.



Symbol		Description		Units
T_{DSCK}	CCLK	DIN setup	5.0	ns, min
T_{CKDS}		DIN hold	0.0	ns, min
		Frequency tolerance with respect to nominal	+45%, –30%	-

Figure 17: **Master Serial Mode Timing**

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency F_{CCNH} above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{\text{WRITE}}$. See "Readback," page 25.

Design Considerations

This section contains more detailed design information on the following features:

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

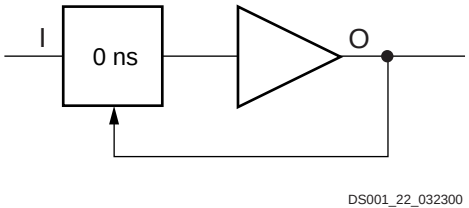


Figure 22: **Simplified DLL Macro BUFGDLL**

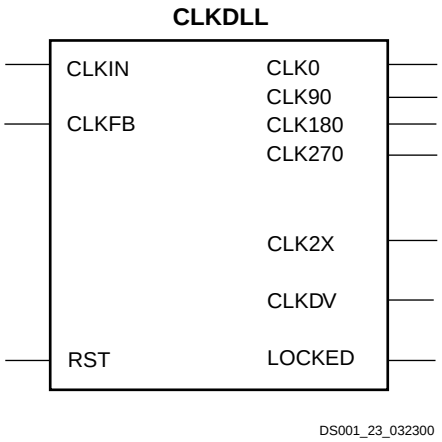


Figure 23: **Standard DLL Primitive CLKDLL**

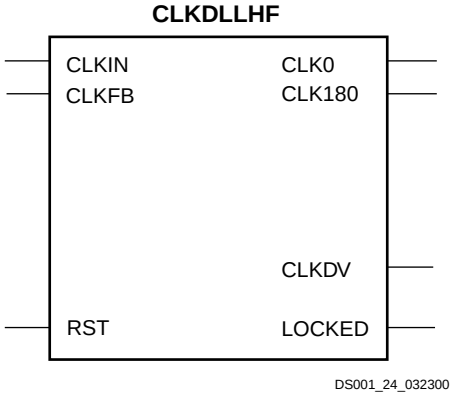


Figure 24: **High-Frequency DLL Primitive CLKDLLHF**

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S4 RAMB4_S4_S4 RAMB4_S4_S8 RAMB4_S4_S16	4	N/A 4 8 16
RAMB4_S8 RAMB4_S8_S8 RAMB4_S8_S16	8	N/A 8 16
RAMB4_S16 RAMB4_S16_S16	16	N/A 16

Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

Table 12: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ([ADDR_{port} + 1] * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 13 shows low order address mapping for each port width.

Table 13: **Port Address Mapping**

Port Width	Port Addresses															
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

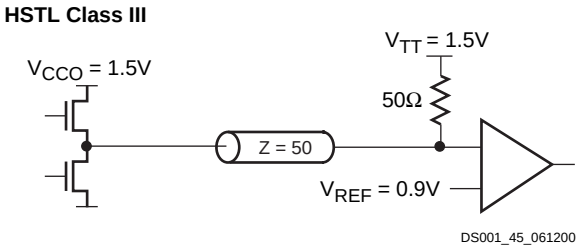


Figure 45: **Terminated HSTL Class III**

Table 23: **HSTL Class III Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

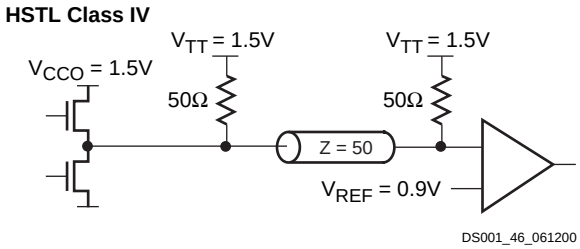


Figure 46: **Terminated HSTL Class IV**

Table 24: **HSTL Class IV Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

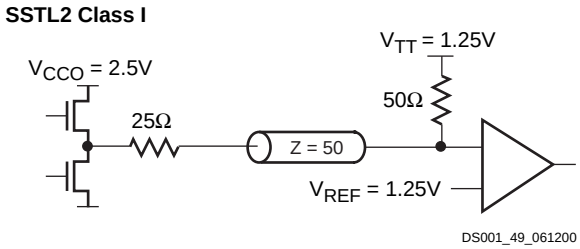


Figure 49: **Terminated SSTL2 Class I**

Table 27: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.61$	1.76	-	-
$V_{OL} \leq V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

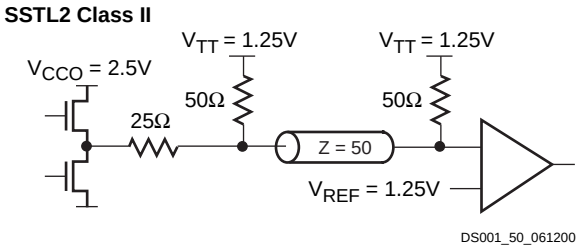


Figure 50: **Terminated SSTL2 Class II**

Table 28: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.8$	1.95	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 32: **LVTTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	5.5
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:
1. V_{OL} and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 33: **LVCMOS2 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	5.5
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL} at V_{OL} (mA)	12	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 34: **AGP-2X Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$ (1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} \geq V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} \leq V_{REF} - 0.2$	-	1.12	1.28
$V_{OH} \geq 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} \leq 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL} at V_{OL} (mA)	Note 2	-	-

Notes:
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	200	60	180	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	25	100	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.0	-	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	2.5	-	3.0	-	ns

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

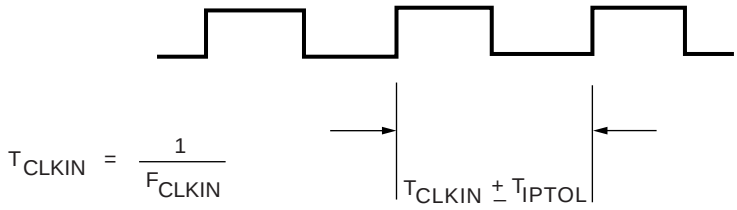
Figure 52, page 63, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(1)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(2)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(3)		-	±140	-	±140	ps
T_{PHIOM}	Maximum phase difference between CLKIN and CLKO(4)		-	±160	-	±160	ps
T_{PHOOM}	Maximum phase difference between clock outputs on the DLL(5)		-	±200	-	±200	ps

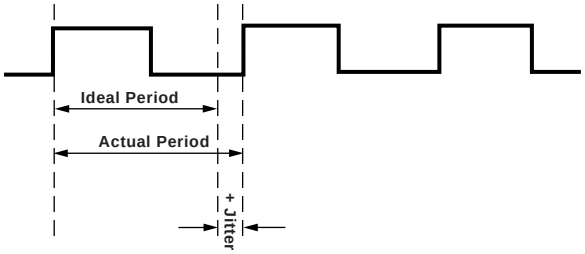
Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference

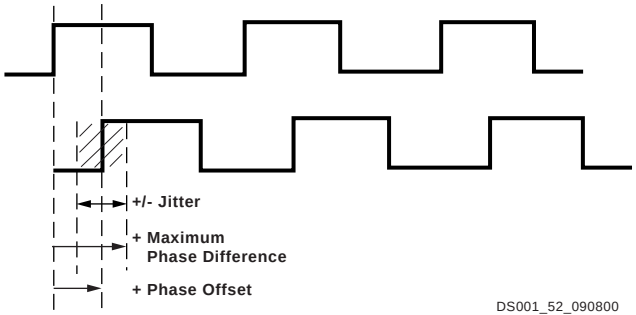


Figure 52: **Period Tolerance and Clock Jitter**

CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
$T_{SHCKO16}$	Clock CLK to X/Y outputs (WE active, 16 x 1 mode)	-	2.2	-	2.6	ns
$T_{SHCKO32}$	Clock CLK to X/Y outputs (WE active, 32 x 1 mode)	-	2.5	-	3.0	ns
Setup/Hold Times with Respect to Clock CLK(1)						
T_{AS} / T_{AH}	F/G address inputs	0.7 / 0	-	0.7 / 0	-	ns
T_{DS} / T_{DH}	BX/BY data inputs (DIN)	0.8 / 0	-	0.9 / 0	-	ns
T_{WS} / T_{WH}	CE input (WS)	0.9 / 0	-	1.0 / 0	-	ns
Clock CLK						
T_{WPH}	Minimum pulse width, High	-	2.9	-	2.9	ns
T_{WPL}	Minimum pulse width, Low	-	2.9	-	2.9	ns
T_{WC}	Minimum clock period to meet address write cycle time	-	5.8	-	5.8	ns

Notes:
1. A zero hold time listing indicates no hold time or a negative hold time.

CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T_{REG}	Clock CLK to X/Y outputs	-	3.47	-	3.88	ns
Setup Times with Respect to Clock CLK						
T_{SHDICK}	BX/BY data inputs (DIN)	0.8	-	0.9	-	ns
T_{SHCECK}	CE input (WS)	0.9	-	1.0	-	ns
Clock CLK						
T_{SRPH}	Minimum pulse width, High	-	2.9	-	2.9	ns
T_{SRPL}	Minimum pulse width, Low	-	2.9	-	2.9	ns

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
11/02/00	2.1	Removed Power Down feature.
01/19/01	2.2	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.
03/09/01	2.3	Added note on power sequencing. Clarified power-on current requirement.
08/28/01	2.4	Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum V_{CCINT} ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range.
07/26/02	2.5	Clarified that I/O leakage current is specified over the Recommended Operating Conditions for V_{CCINT} and V_{CCO}.
08/26/02	2.6	Added references for XAPP450 to Power-On Current Specification.
09/03/03	2.7	Added relaxed minimum power-on current (I_{CCPO}) requirements to page 53. On page 64, moved T_{RPW} values from maximum to minimum column.
06/13/08	2.8	Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

XC2S15 Device Pinouts *(Continued)*

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GND	-	-	P61	J12	-
I/O (D5)	3	P57	P60	J13	245
I/O	3	P58	P59	H10	248
I/O, V_{REF}	3	P59	P58	H11	251
I/O (D4)	3	P60	P57	H12	254
I/O	3	-	P56	H13	257
V_{CCINT}	-	P61	P55	G12	-
I/O, TRDY(1)	3	P62	P54	G13	260
V_{CCO}	3	P63	P53	G11	-
V_{CCO}	2	P63	P53	G11	-
GND	-	P64	P52	G10	-
I/O, IRDY(1)	2	P65	P51	F13	263
I/O	2	-	P50	F12	266
I/O (D3)	2	P66	P49	F11	269
I/O, V_{REF}	2	P67	P48	F10	272
I/O	2	P68	P47	E13	275
I/O (D2)	2	P69	P46	E12	278
GND	-	-	P45	E11	-
I/O (D1)	2	P70	P44	E10	281
I/O	2	P71	P43	D13	284
I/O, V_{REF}	2	P72	P41	D11	287
I/O	2	-	P40	C13	290
I/O (DIN, D0)	2	P73	P39	C12	293
I/O (DOUT, BUSY)	2	P74	P38	C11	296
CCLK	2	P75	P37	B13	299
V_{CCO}	2	P76	P36	B12	-
V_{CCO}	1	P76	P35	A13	-
TDO	2	P77	P34	A12	-
GND	-	P78	P33	B11	-
TDI	-	P79	P32	A11	-
I/O ($\overline{CS}$)	1	P80	P31	D10	0
I/O ($\overline{WRITE}$)	1	P81	P30	C10	3
I/O	1	-	P29	B10	6
I/O, V_{REF}	1	P82	P28	A10	9
I/O	1	P83	P27	D9	12
I/O	1	P84	P26	C9	15
GND	-	-	P25	B9	-
V_{CCINT}	-	P85	P24	A9	-
I/O	1	-	P23	D8	18
I/O	1	-	P22	C8	21

XC2S15 Device Pinouts *(Continued)*

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
I/O, V_{REF}	1	P86	P21	B8	24
I/O	1	-	P20	A8	27
I/O	1	P87	P19	B7	30
I, GCK2	1	P88	P18	A7	36
GND	-	P89	P17	C7	-
V_{CCO}	1	P90	P16	D7	-
V_{CCO}	0	P90	P16	D7	-
I, GCK3	0	P91	P15	A6	37
V_{CCINT}	-	P92	P14	B6	-
I/O	0	-	P13	C6	44
I/O, V_{REF}	0	P93	P12	D6	47
I/O	0	-	P11	A5	50
I/O	0	-	P10	B5	53
V_{CCINT}	-	P94	P9	C5	-
GND	-	-	P8	D5	-
I/O	0	P95	P7	A4	56
I/O	0	P96	P6	B4	59
I/O, V_{REF}	0	P97	P5	C4	62
I/O	0	-	P4	A3	65
I/O	0	P98	P3	B3	68
TCK	-	P99	P2	C3	-
V_{CCO}	0	P100	P1	A2	-
V_{CCO}	7	P100	P144	B2	-

04/18/01

Notes:
1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S15 Package Pins

VQ100

Not Connected Pins					
P28	P29	-	-	-	-

11/02/00

TQ144

Not Connected Pins					
P42	P64	P78	P101	P104	P105
P116	P138	-	-	-	-

11/02/00

CS144

Not Connected Pins					
D3	D12	J4	K13	M3	M4
M10	N3	-	-	-	-

11/02/00

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	5	P99	P63	P6	326
GND	-	P98	P64	GND*	-
V_{CCO}	5	-	P65	V_{CCO} Bank 5*	-
V_{CCINT}	-	P97	P66	V_{CCINT}*	-
I/O	5	P96	P67	R6	329
I/O	5	P95	P68	M7	332
I/O	5	-	P69	N7	338
I/O	5	-	P70	T6	341
I/O	5	-	P71	P7	344
GND	-	-	P72	GND*	-
I/O, V_{REF}	5	P94	P73	P8	347
I/O	5	-	P74	R7	350
I/O	5	-	-	T7	353
I/O	5	P93	P75	T8	356
V_{CCINT}	-	P92	P76	V_{CCINT}*	-
I, GCK1	5	P91	P77	R8	365
V_{CCO}	5	P90	P78	V_{CCO} Bank 5*	-
V_{CCO}	4	P90	P78	V_{CCO} Bank 4*	-
GND	-	P89	P79	GND*	-
I, GCK0	4	P88	P80	N8	366
I/O	4	P87	P81	N9	370
I/O	4	P86	P82	R9	373
I/O	4	-	-	N10	376
I/O	4	-	P83	T9	379
I/O, V_{REF}	4	P85	P84	P9	382
GND	-	-	P85	GND*	-
I/O	4	-	P86	M10	385
I/O	4	-	P87	R10	388
I/O	4	-	P88	P10	391
I/O	4	P84	P89	T10	397
I/O	4	P83	P90	R11	400
V_{CCINT}	-	P82	P91	V_{CCINT}*	-
V_{CCO}	4	-	P92	V_{CCO} Bank 4*	-
GND	-	P81	P93	GND*	-
I/O	4	P80	P94	M11	403
I/O	4	P79	P95	T11	406
I/O	4	P78	P96	N11	409
I/O	4	-	-	R12	412

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	4	-	P97	P11	415
I/O, V_{REF}	4	P77	P98	T12	418
GND	-	-	-	GND*	-
I/O	4	-	P99	T13	421
I/O	4	-	-	N12	424
I/O	4	P76	P100	R13	427
I/O	4	-	-	P12	430
I/O	4	P75	P101	P13	433
I/O	4	P74	P102	T14	436
GND	-	P73	P103	GND*	-
DONE	3	P72	P104	R14	439
V_{CCO}	4	P71	P105	V_{CCO} Bank 4*	-
V_{CCO}	3	P70	P105	V_{CCO} Bank 3*	-
$\overline{PROGRAM}$	-	P69	P106	P15	442
I/O ($\overline{INIT}$)	3	P68	P107	N15	443
I/O (D7)	3	P67	P108	N14	446
I/O	3	-	-	T15	449
I/O	3	P66	P109	M13	452
I/O	3	-	-	R16	455
I/O	3	-	P110	M14	458
GND	-	-	-	GND*	-
I/O, V_{REF}	3	P65	P111	L14	461
I/O	3	-	P112	M15	464
I/O	3	-	-	L12	467
I/O	3	P64	P113	P16	470
I/O	3	P63	P114	L13	473
I/O (D6)	3	P62	P115	N16	476
GND	-	P61	P116	GND*	-
V_{CCO}	3	-	P117	V_{CCO} Bank 3*	-
V_{CCINT}	-	-	P118	V_{CCINT}*	-
I/O (D5)	3	P60	P119	M16	479
I/O	3	P59	P120	K14	482
I/O	3	-	-	L16	485
I/O	3	-	P121	K13	488
I/O	3	-	P122	L15	491
I/O	3	-	P123	K12	494
GND	-	-	P124	GND*	-
I/O, V_{REF}	3	P58	P125	K16	497
I/O (D4)	3	P57	P126	J16	500

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V_{CCINT}	-	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	GND*	-
I/O	6	P118	P41	K4	T1	314
I/O, V_{REF}	6	P117	P42	M1	R4	317
I/O	6	-	-	-	T2	320
I/O	6	P116	P43	L4	U1	323
I/O	6	-	-	M2	R5	326
I/O	6	-	P44	L3	U2	332
I/O, V_{REF}	6	P115	P45	N1	T3	335
V_{CCO}	6	-	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	-	GND*	GND*	-
I/O	6	-	P46	P1	T4	338
I/O	6	-	-	L5	W1	341
I/O	6	-	-	-	U4	344
I/O	6	P114	P47	N2	Y1	347
I/O	6	-	-	M4	W2	350
I/O	6	P113	P48	R1	Y2	356
I/O	6	P112	P49	M3	W3	359
M1	-	P111	P50	P2	U5	362
GND	-	P110	P51	GND*	GND*	-
M0	-	P109	P52	N3	AB2	363
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	Y4	364
I/O	5	-	-	N5	V7	374
I/O	5	P103	P57	T2	Y6	377
I/O	5	-	-	-	AA4	380
I/O	5	-	-	P5	W6	383
I/O	5	-	P58	T3	Y7	386
GND	-	-	-	GND*	GND*	-
V_{CCO}	5	-	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P102	P59	T4	AA5	389
I/O	5	-	P60	M6	AB5	392
I/O	5	-	-	T5	AB6	398
I/O	5	P101	P61	N6	AA7	401
I/O	5	-	-	-	W7	404

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O, V_{REF}	5	P100	P62	R5	W8	407
I/O	5	P99	P63	P6	Y8	410
GND	-	P98	P64	GND*	GND*	-
V_{CCO}	5	-	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P97	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P96	P67	R6	AA8	413
I/O	5	P95	P68	M7	V9	416
I/O	5	-	-	-	AB9	419
I/O	5	-	P69	N7	Y9	422
I/O	5	-	P70	T6	W10	428
I/O	5	-	P71	P7	AB10	431
GND	-	-	P72	GND*	GND*	-
I/O, V_{REF}	5	P94	P73	P8	Y10	434
I/O	5	-	P74	R7	V11	437
I/O	5	-	-	T7	W11	440
I/O	5	P93	P75	T8	AB11	443
V_{CCINT}	-	P92	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P91	P77	R8	Y11	455
V_{CCO}	5	P90	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P90	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P89	P79	GND*	GND*	-
I, GCK0	4	P88	P80	N8	W12	456
I/O	4	P87	P81	N9	U12	460
I/O	4	P86	P82	R9	Y12	466
I/O	4	-	-	N10	AA12	469
I/O	4	-	P83	T9	AB13	472
I/O, V_{REF}	4	P85	P84	P9	AA13	475
GND	-	-	P85	GND*	GND*	-
I/O	4	-	P86	M10	Y13	478
I/O	4	-	P87	R10	V13	481
I/O	4	-	P88	P10	AA14	487
I/O	4	-	-	-	V14	490
I/O	4	P84	P89	T10	AB15	493
I/O	4	P83	P90	R11	AA15	496
V_{CCINT}	-	P82	P91	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	4	-	P92	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P81	P93	GND*	GND*	-
I/O	4	P80	P94	M11	Y15	499

XC2S150 Device Pinouts

XC2S150 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V_{REF}	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY(1)	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	326
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V_{REF}	6	P31	J3	N2	344
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V_{REF}	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V_{REF}	6	P45	N1	T3	401
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts

XC2S200 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V_{REF}	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V_{REF}	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY(1)	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	380
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V_{REF}	6	P31	J3	N2	407
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V_{REF}	6	P42	M1	R4	443