Lattice Semiconductor Corporation - LC4032ZE-4MN64C Datasheet

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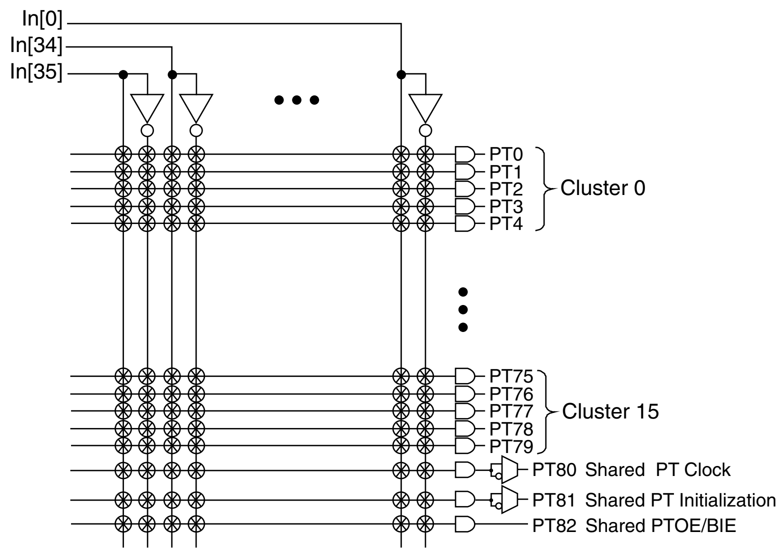
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.4 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TFBGA, CSPBGA
Supplier Device Package	64-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032ze-4mn64c

Figure 3. AND Array



Note:
⊗ Indicates programmable fuse.

Enhanced Logic Allocator

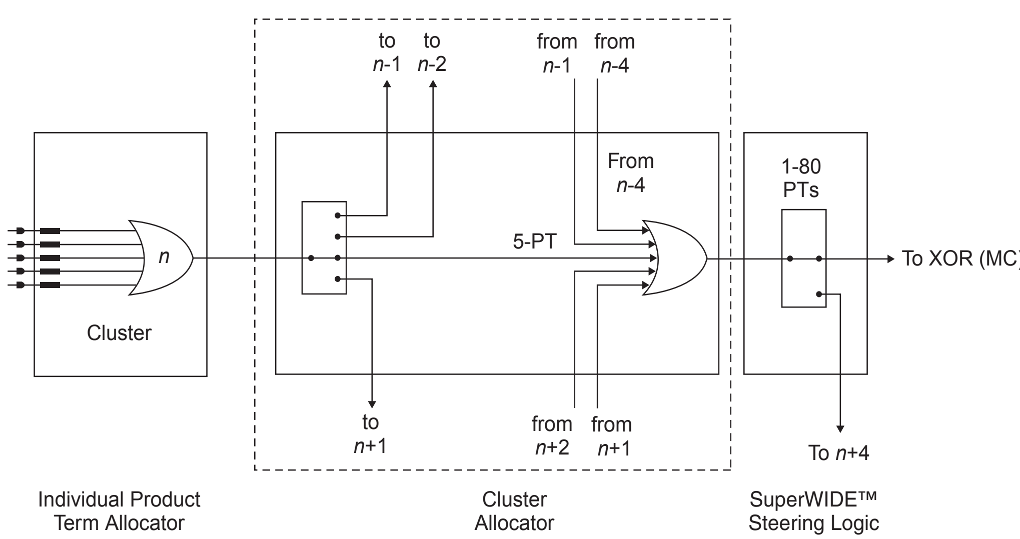
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

Table 2. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 3. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 4]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 5]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 6]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 7]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 8]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 9]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 10]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 11]	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M3, M4, M5, M6, M7, M8, M9, M10
[GLB] [MC 4]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 5]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 6]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 7]	M7, M8, M9, M10, M11, M12, M13, M14
[GLB] [MC 8]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 9]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 10]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 11]	M11, M12, M13, M14, M15, M0, M1, M2
[GLB] [MC 12]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 13]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 14]	M14, M15, M0, M1, M2, M3, M4, M5
[GLB] [MC 15]	M15, M0, M1, M2, M3, M4, M5, M6

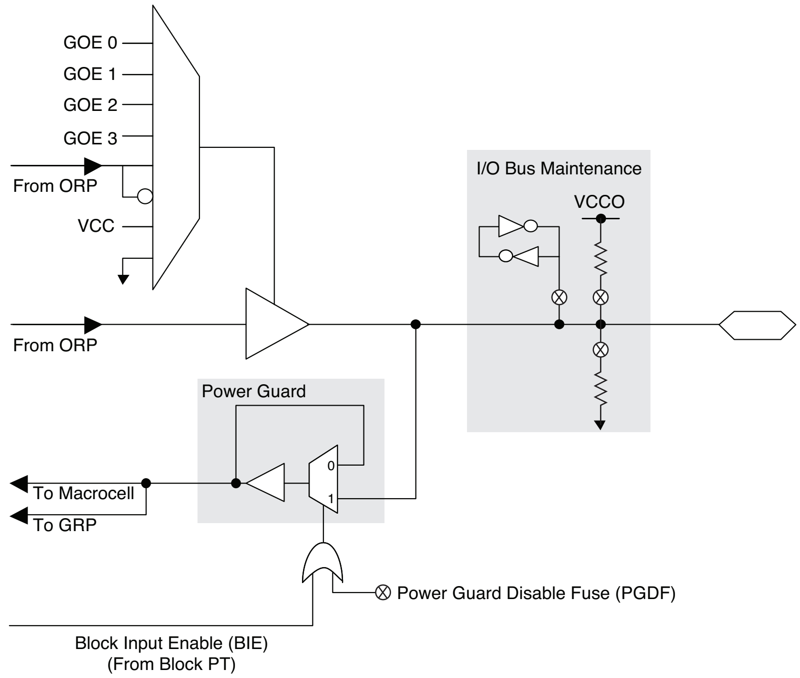
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a “per-pin” basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

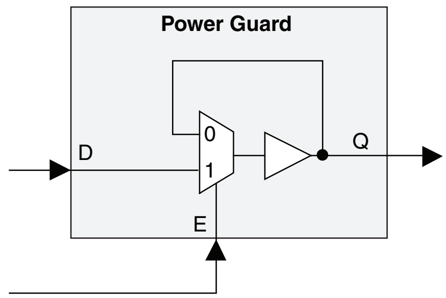
The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

Figure 9. Power Guard

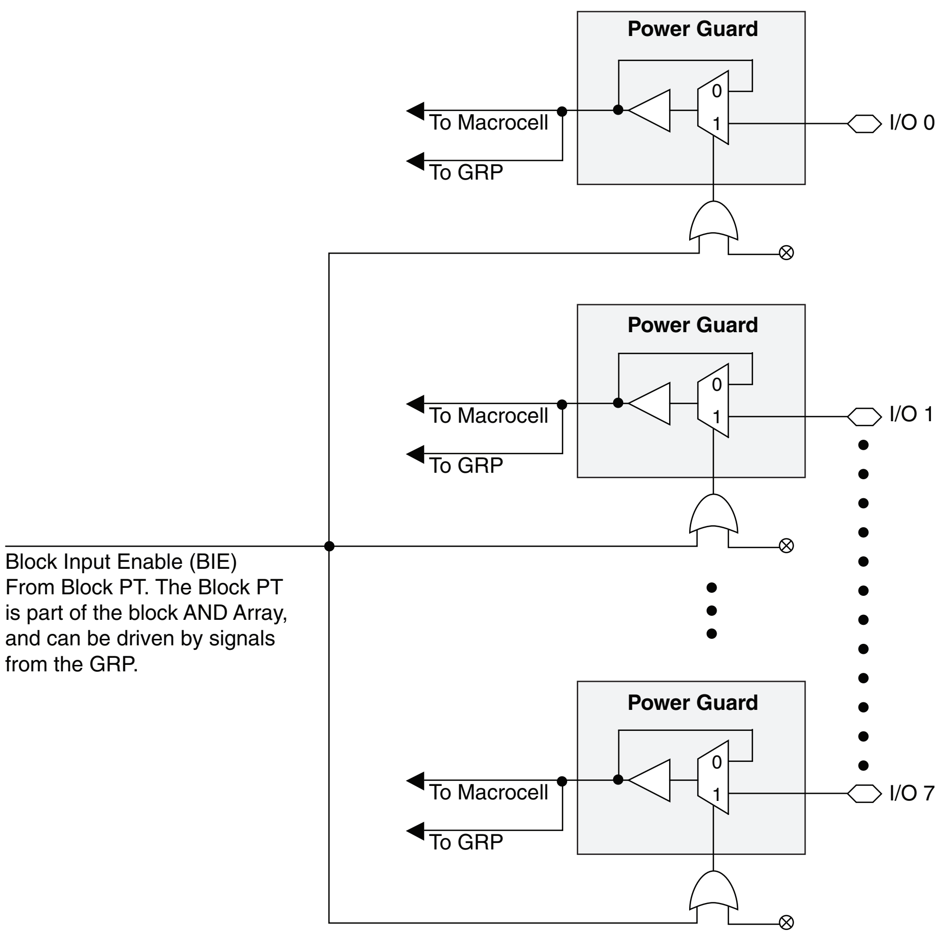


All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os



Some Simple Use Scenarios

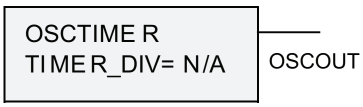
The following diagrams show a few simple examples that omit optional signals for the OSCTIMER block:

A. An oscillator giving 5MHz nominal clock

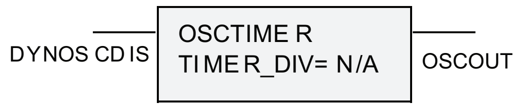
B. An oscillator that can be disabled with an external signal (5MHz nominal clock)

C. An oscillator giving approximately 5 Hz nominal clock (TIMER_DIV = 2^{20} (1,048,576))

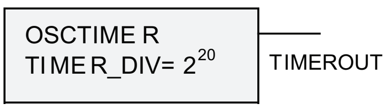
D. An oscillator giving two output clocks: ~5MHz and ~5KHz (TIMER_DIV= 2^{10} (1,024))



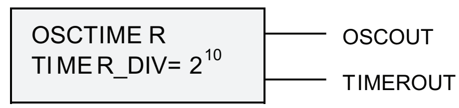
(A) A simple 5MHz oscillator.



(B) An oscillator with dynamic disable.



(C) A simple 5Hz oscillator.



(D) Oscillator with two outputs (5MHz and 5KHz).

OSCTIMER Integration With CPLD Fabric

The OSCTIMER is integrated into the CPLD fabric using the Global Routing Pool (GRP). The macrocell (MC) feedback path for two macrocells is augmented with a programmable multiplexer, as shown in Figure 15. The OSCTIMER outputs (OSCOUT and TIMEROUT) can optionally drive the GRP lines, whereas the macrocell outputs can drive the optional OSCTIMER inputs TIMERRES and DYNOSCDIS.

Figure 15. OSCTIMER Integration With CPLD Fabric

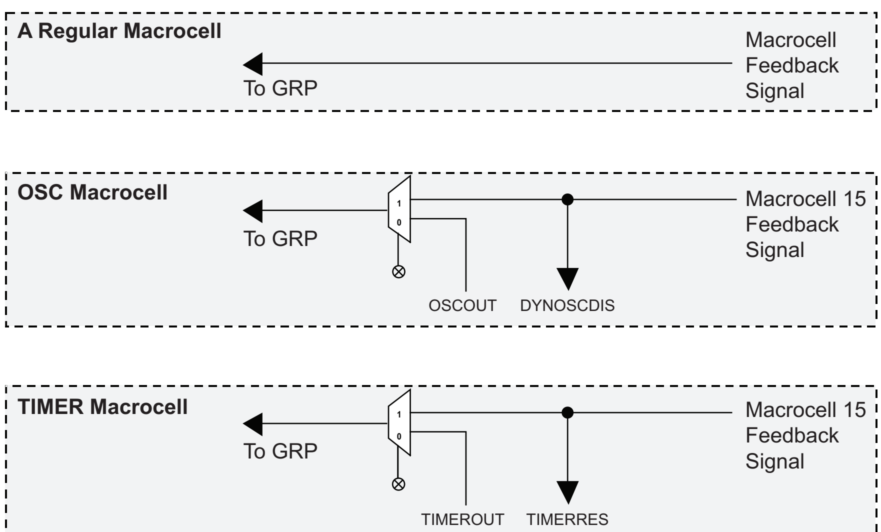


Table 12 shows how these two MCs are designated in each of the ispMACH4000ZE device.

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . -0.5 to 5.5V

Storage Temperature . . . .-65 to 150°C

Junction Temperature (T_j) with Power Applied . . .-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

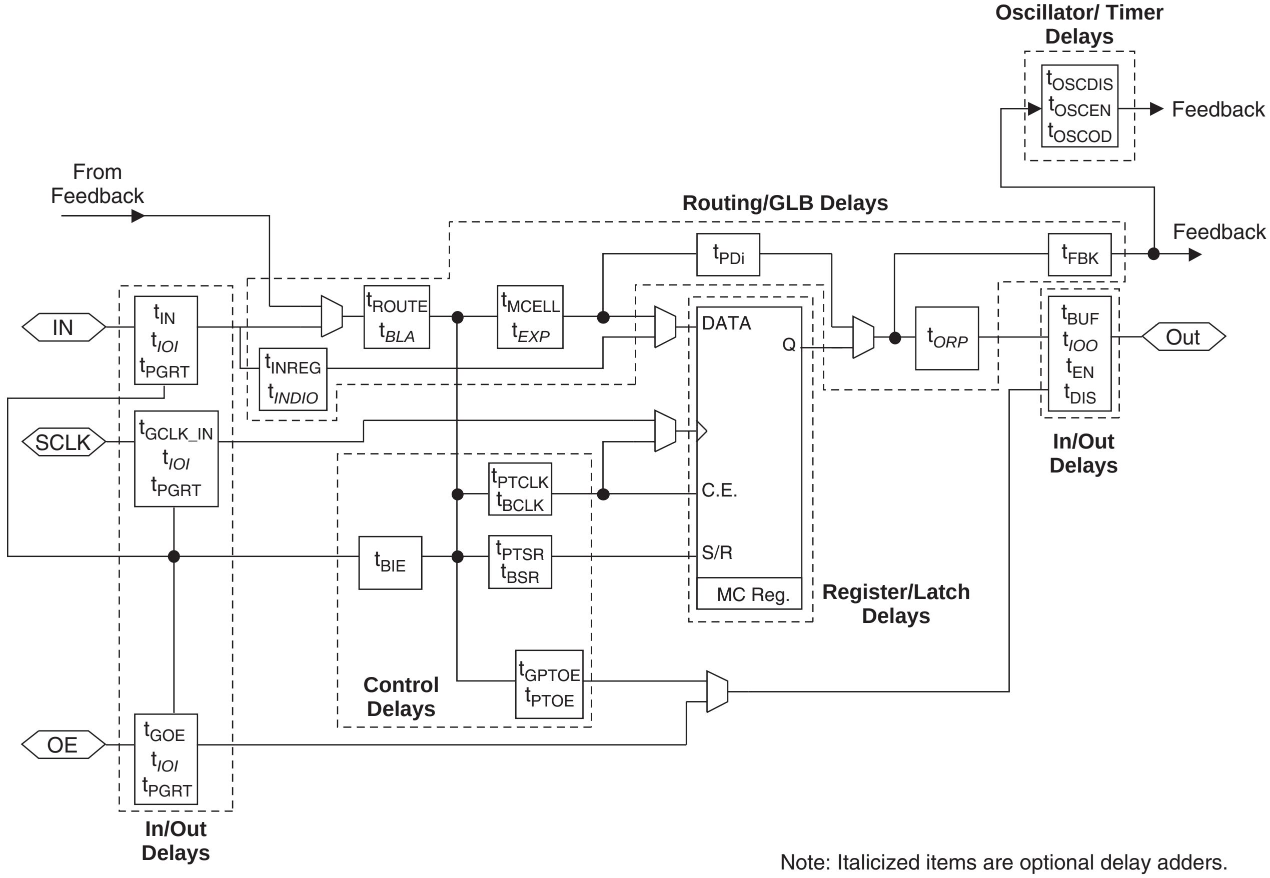
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) $\leq$ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines.

Figure 16. ispMACH 4000ZE Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	2.00	—	1.70	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.20	—	1.30	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.40	—	1.50	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.10	—	1.85	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.20	—	1.90	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.60	—	1.70	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.30	—	3.15	ns
t_{GPTOE}	Global PT OE Delay		—	1.80	—	2.15	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	12.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	7.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	6.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	5.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	4.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	3.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.00	—	1.00	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.40	—	0.40	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.04	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

Figure 17. Output Test Load, LVTTL and LVCMOS Standards

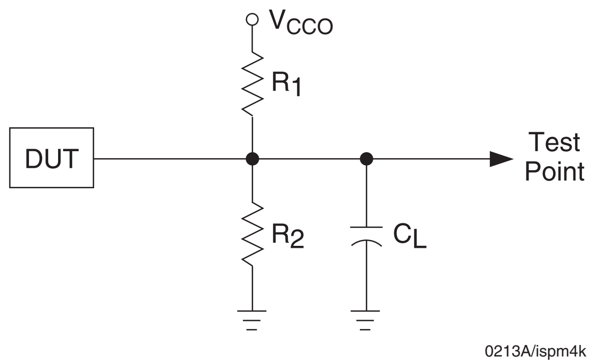


Table 13. Test Fixture Required Components

Test Condition	R_1	R_2	C_L [1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $\frac{V_{CCO}}{2}$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $\frac{V_{CCO}}{2}$	LVCMOS 1.8 = 1.65V
				LVCMOS 1.5 = $\frac{V_{CCO}}{2}$	LVCMOS 1.5 = 1.4V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND	GND
2	-	TDI	TDI	TDI
3	0	A8	B0	C12
4	0	A9	B2	C10
5	0	A10	B4	C6
6	0	A11	B6	C2
7	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
8	0	A12	B8	D12
9	0	A13	B10	D10
10	0	A14	B12	D6
11	0	A15	B13	D4
12*	0	I	I	I
13	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
14	0	B15	C14	E4
15	0	B14	C12	E6
16	0	B13	C10	E10
17	0	B12	C8	E12
18	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
19	0	B11	C6	F2
20	0	B10	C5	F6
21	0	B9	C4	F10
22	0	B8	C2	F12
23*	0	I	I	I
24	-	TCK	TCK	TCK
25	-	VCC	VCC	VCC
26	-	GND	GND	GND
27*	0	I	I	I
28	0	B7	D13	G12
29	0	B6	D12	G10
30	0	B5	D10	G6
31	0	B4	D8	G2
32	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
33	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
34	0	B3	D6	H12
35	0	B2	D4	H10
36	0	B1	D2	H6
37	0	B0	D0	H2
38	0	CLK1/I	CLK1/I	CLK1/I
39	1	CLK2/I	CLK2/I	CLK2/I
40	-	VCC	VCC	VCC
41	1	C0	E0	I2

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
GND*	-	GND
A1	-	TDI
B1	0	VCCO (Bank 0)
D3	0	B0
C1	0	B1
D2	0	B2
D1	0	B4
E4	0	B5
F3	0	B6
E2	0	GND (Bank 0)
E1	0	B8
E3	0	B9
F4	0	B10
G4	0	B12
F2	0	B13
G3	0	B14
H4	0	VCCO (Bank 0)
F1	0	C14
G2	0	C13
G1	0	C12
H3	0	C10
J4	0	C9
H1	0	C8
H2	0	GND (Bank 0)
J3	0	C6
J1	0	C5
J2	0	C4
K3	0	C2
K2	0	C1
K1	0	C0
L2	0	VCCO (Bank 0)
L1	-	TCK
M1	-	VCC
GND*	-	GND
L3	0	D14
M2	0	D13
K4	0	D12
M3	0	D10
K5	0	D9
L4	0	D8
M4	0	GND (Bank 0)
J5	0	VCCO (Bank 0)
L5	0	D6

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
A2	0	A14

* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

Part Number Description

LC XXXX XX – XX XX XXX X XX

Device Family

Device Number
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells

Power
ZE = Zero Power, Enhanced

Speed
4 = 4.4ns (4032ZE Only)
4 = 4.7ns (4064ZE Only)
5 = 5.8ns (All Devices)
7 = 7.5ns (All Devices)

Production Status
Blank = Final production device
ES = Engineering samples

Operating Temperature Range
C = Commercial
I = Industrial

Pin/Ball Count
48 (1.0 mm thickness)
64
100
132
144

Package
TN = Lead-free TQFP
MN = Lead-free csBGA (0.5 mm pitch)
UMN = Lead-free ucBGA (0.4 mm pitch)

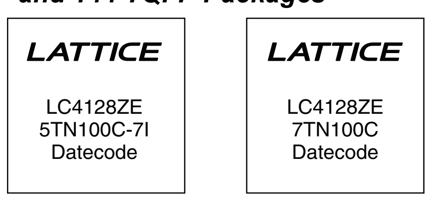
ispMACH 4000ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

Ordering Information

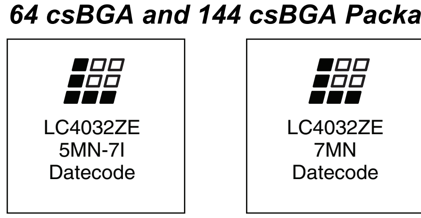
Note: ispMACH 4000ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages



Dual Mark **Single Mark**

Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages



Dual Mark **Single Mark**

Industrial

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
	LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

Technical Support Assistance

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