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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

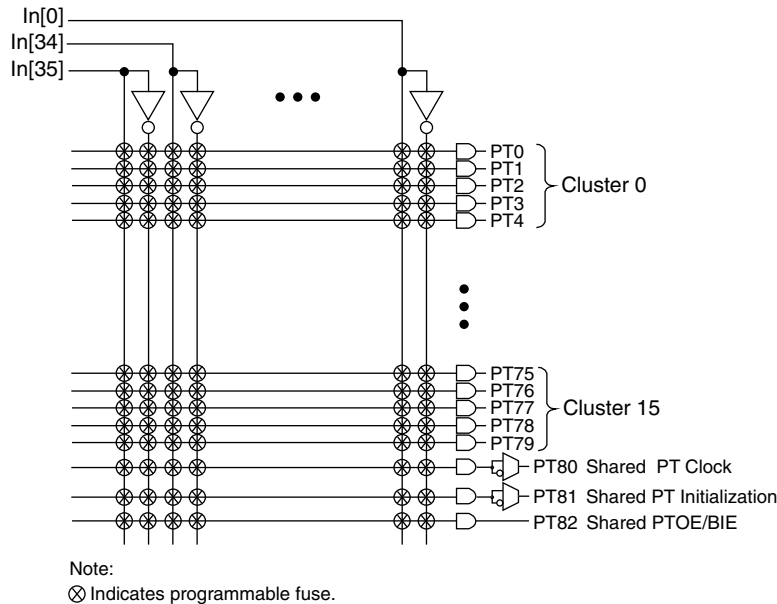
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TFBGA, CSPBGA
Supplier Device Package	64-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032ze-5mn64c

Figure 3. AND Array



Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice

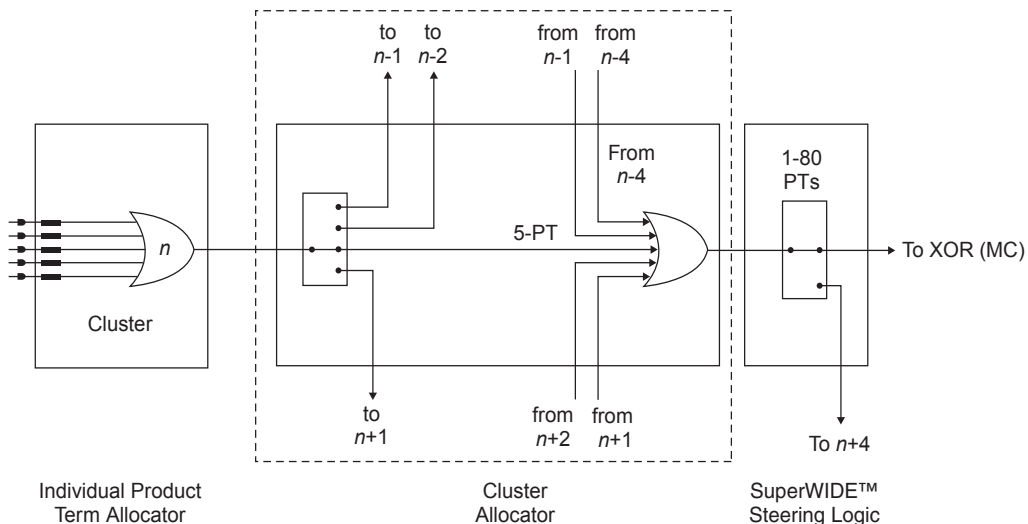


Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 4]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 5]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 6]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 7]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 8]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 9]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 10]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 11]	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M3, M4, M5, M6, M7, M8, M9, M10
[GLB] [MC 4]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 5]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 6]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 7]	M7, M8, M9, M10, M11, M12, M13, M14
[GLB] [MC 8]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 9]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 10]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 11]	M11, M12, M13, M14, M15, M0, M1, M2
[GLB] [MC 12]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 13]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 14]	M14, M15, M0, M1, M2, M3, M4, M5
[GLB] [MC 15]	M15, M0, M1, M2, M3, M4, M5, M6

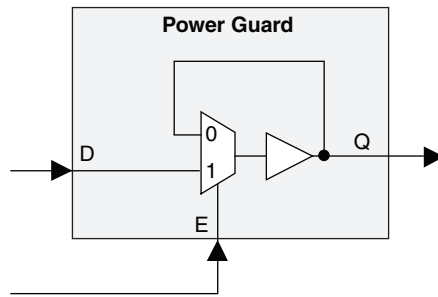
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 9. Power Guard

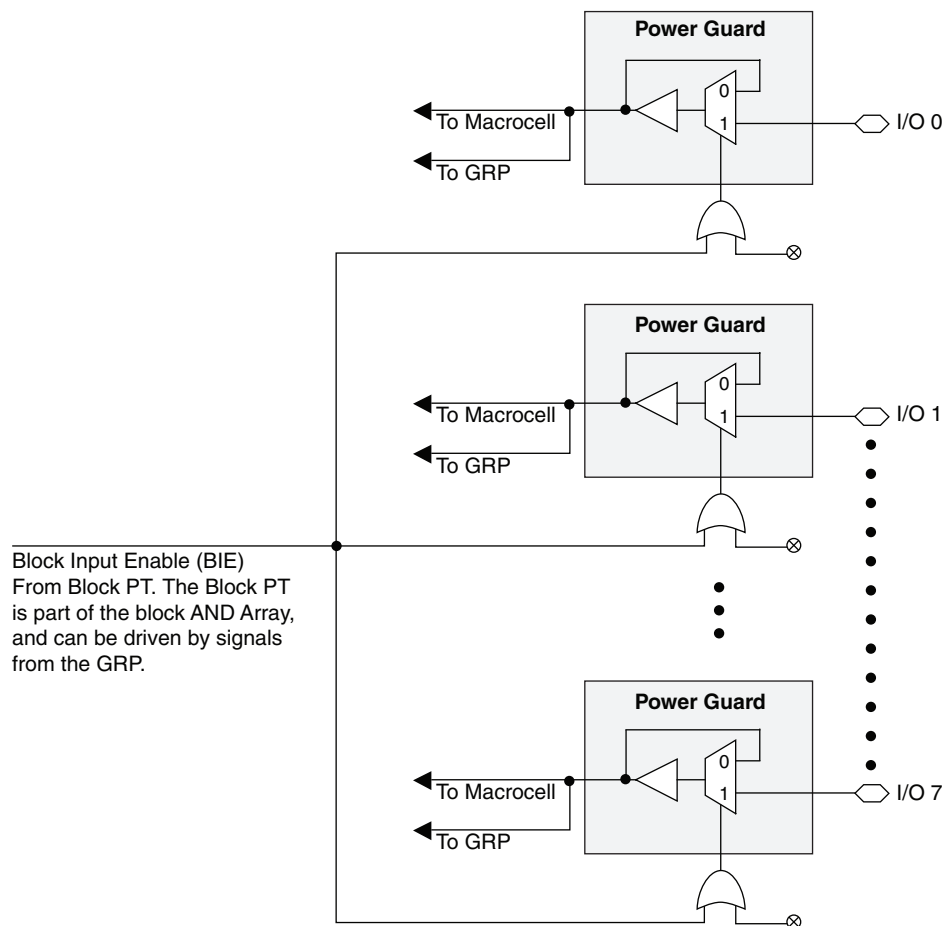


All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os



The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, ..., H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, ..., P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, [Advanced Features of the ispMACH 4000ZE Family](#).

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macro-cell device (with 16 blocks), each block's BIE signal is driven by block-level OE PT from each block.

Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE

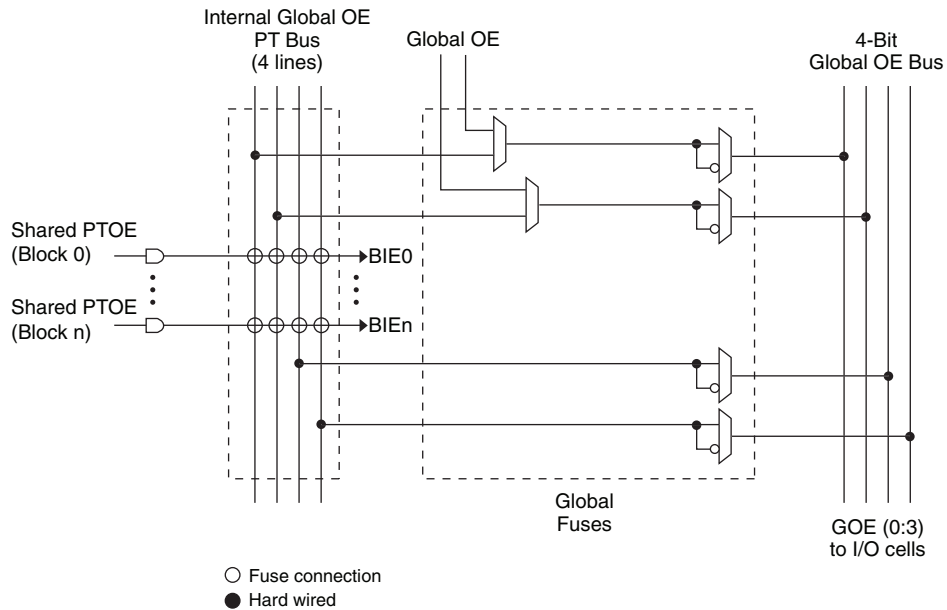
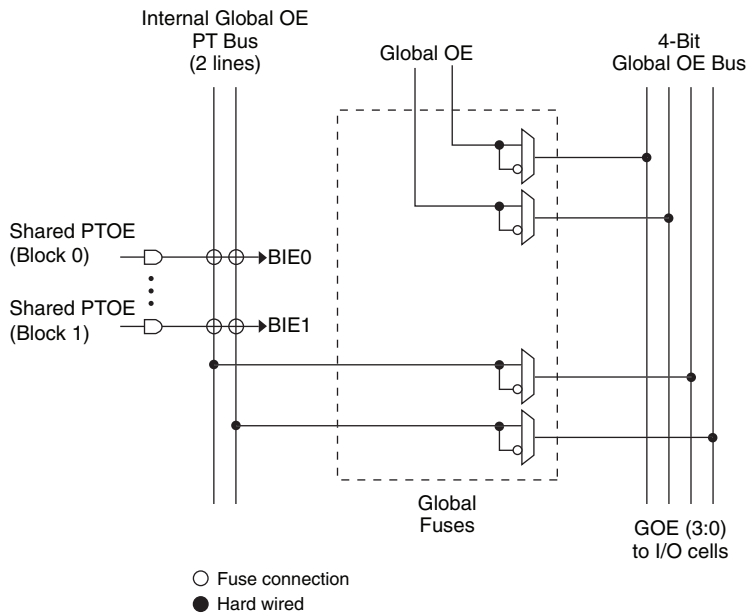


Figure 12. Global OE Generation for ispMACH 4032ZE



On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

Table 12. OSC and TIMER MC Designation

Device	Macrocell	Block Number	MC Number
ispMACH 4032ZE	OSC MC	A	15
	TIMER MC	B	15
ispMACH 4064ZE	OSC MC	A	15
	TIMER MC	D	15
ispMACH 4128ZE	OSC MC	A	15
	TIMER MC	G	15
ispMACH 4256ZE	OSC MC	C	15
	TIMER MC	F	15

Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E² low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

ispMACH 400ZE External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1,2}	LC4032ZE		LC4064ZE		All Devices				Units
		-4		-4		-5		-7		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	20-PT combinatorial propagation delay	—	4.4	—	4.7	—	5.8	—	7.5	ns
t _S	GLB register setup time before clock	2.2	—	2.5	—	2.9	—	4.5	—	ns
t _{ST}	GLB register setup time before clock with T-type register	2.4	—	2.7	—	3.1	—	4.7	—	ns
t _{SIR}	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	1.4	—	ns
t _{SIRZ}	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.9	—	4.0	—	ns
t _H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	1.3	—	ns
t _{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t _{CO}	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.8	—	4.5	ns
t _R	External reset pin to output delay	—	5.0	—	6.0	—	7.5	—	9.0	ns
t _{RW}	External reset pulse duration	1.5	—	1.7	—	2.0	—	4.0	—	ns
t _{P_{TOE/DIS}}	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.2	—	9.0	ns
t _{G_{P_{TOE/DIS}}}	Input to output global product term output enable/disable	—	6.5	—	7.0	—	10.0	—	10.5	ns
t _{GOE/DIS}	Global OE input to output enable/disable	—	4.5	—	4.5	—	5.5	—	7.0	ns
t _{CW}	Global clock width, high or low	1.0	—	1.5	—	1.8	—	2.8	—	ns
t _{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	2.8	—	ns
t _{WIR}	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	2.8	—	ns
f _{MAX (Int.)} ³	Clock frequency with internal feedback	—	260	—	241	—	200	—	172	MHz
f _{MAX (Ext.)}	clock frequency with external feedback, [1 / (t _S + t _{CO})]	—	192	—	175	—	149	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

2. Measured using standard switching GRP loading of 1 and 1 output switching.

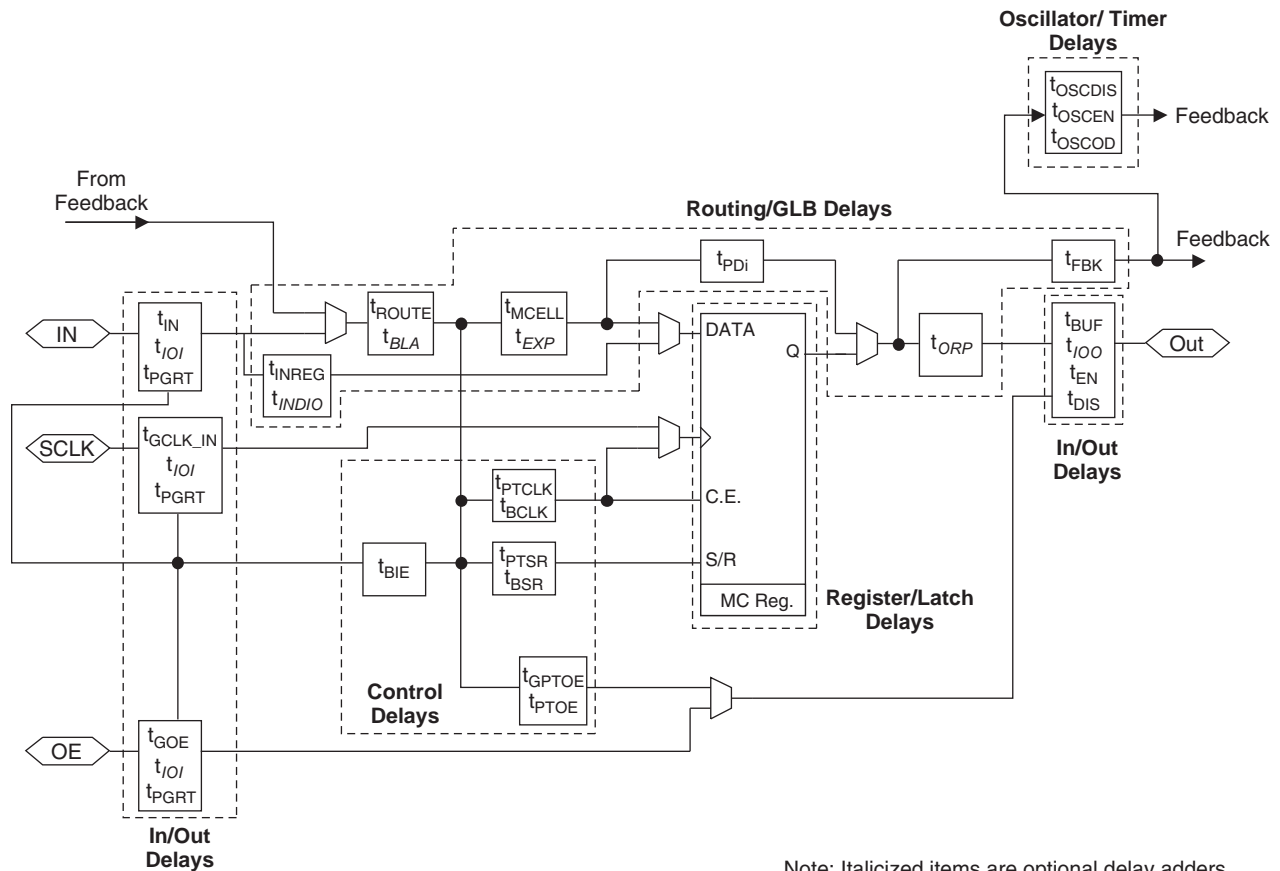
3. Standard 16-bit counter using GRP feedback.

Timing v.0.8

Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, [ispMACH 4000ZE Timing Model Design and Usage Guidelines](#).

Figure 16. ispMACH 4000ZE Timing Model

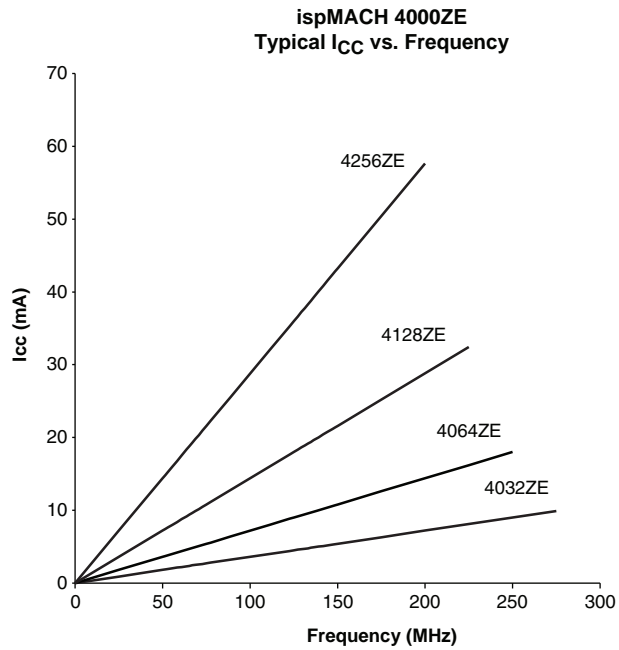


ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LC4032ZE		LC4064ZE		Units	
		-4		-4			
		Min.	Max.	Min.	Max.		
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.70	ns	
Control Delays							
t _{BCLK}	GLB PT Clock Delay	—	1.20	—	1.30	ns	
t _{PTCLK}	Macrocell PT Clock Delay	—	1.40	—	1.50	ns	
t _{BSR}	Block PT Set/Reset Delay	—	1.10	—	1.85	ns	
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.20	—	1.90	ns	
t _{BIE}	Power Guard Block Input Enable Delay	—	1.60	—	1.70	ns	
t _{P_{TOE}}	Macrocell PT OE Delay	—	2.30	—	3.15	ns	
t _{GPTOE}	Global PT OE Delay	—	1.80	—	2.15	ns	
Internal Oscillator							
t _{O_{SCSU}}	Oscillator DYNOSCDIS Setup Time	5.00	—	5.00	—	ns	
t _{O_{SCH}}	Oscillator DYNOSCDIS Hold Time	5.00	—	5.00	—	ns	
t _{O_{SCEN}}	Oscillator OSCOUT Enable Time (To Stable)	—	5.00	—	5.00	ns	
t _{O_{SCOD}}	Oscillator Output Delay	—	4.00	—	4.00	ns	
t _{O_{SCNOM}}	Oscillator OSCOUT Nominal Frequency	—	5.00	—	5.00	MHz	
t _{O_{SCvar}}	Oscillator Variation of Nominal Frequency	—	30	—	30	%	
t _{T_{MRCO20}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)	—	12.50	—	12.50	ns	
t _{T_{MRCO10}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)	—	7.50	—	7.50	ns	
t _{T_{MRCO7}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)	—	6.00	—	6.00	ns	
t _{T_{MRRSTO}}	Oscillator TIMEROUT Reset to Out (Going Low)	—	5.00	—	5.00	ns	
t _{T_{MRRR}}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay	—	4.00	—	4.00	ns	
t _{T_{MRRSTPW}}	Oscillator TIMEROUT Reset Minimum Pulse Width	3.00	—	3.00	—	ns	
Optional Delay Adjusters		Base Parameter					
t _{I_{NDIO}}	Input Register Delay	t _{I_{NREG}}	—	1.00	—	1.00	ns
t _{E_{XP}}	Product Term Expander Delay	t _{M_{CELL}}	—	0.40	—	0.40	ns
t _{B_{LA}}	Additional Block Loading Adders	t _{R_{ROUTE}}	—	0.04	—	0.05	ns
t_{I_{OI}} Input Buffer Delays							
LVTTTL_in	Using LVTTTL Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.60	—	0.60	ns
LVC _{MOS15_in}	Using LVC _{MOS} 1.5 Standard	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.20	—	0.20	ns
LVC _{MOS18_in}	Using LVC _{MOS} 1.8 Standard	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.00	—	0.00	ns
LVC _{MOS25_in}	Using LVC _{MOS} 2.5 Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
LVC _{MOS33_in}	Using LVC _{MOS} 3.3 Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
t_{I_{OO}} Output Buffer Delays							
LVTTTL_out	Output Configured as TTL Buffer	t _{E_N} , t _{D_{IS}} , t _{B_{UF}}	—	0.20	—	0.20	ns

Power Consumption



Power Estimation Coefficients¹

Device	A	B
ispMACH 4032ZE	0.010	0.009
ispMACH 4064ZE	0.011	0.009
ispMACH 4128ZE	0.012	0.009
ispMACH 4256ZE	0.013	0.009

1. For further information about the use of these coefficients, refer to TN1187, [Power Estimation in ispMACH 4000ZE Devices](#).

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
B2	-	TDI	TDI
B1	0	A5	A8
C2	0	A6	A10
C1	0	A7	A11
GND*	0	GND (Bank 0)	GND (Bank 0)
C3	0	NC	A12
E3	0	VCCO (Bank 0)	VCCO (Bank 0)
D1	0	A8	B15
D2	0	NC	B14
E1	0	A9	B13
D3	0	A10	B12
F1	0	A11	B11
E2	0	NC	B10
G1	0	NC	B9
F2	0	NC	B8
H1	-	TCK	TCK
E4	-	VCC	VCC
GND*	-	GND	GND
G2	0	A12	B6
H2	0	NC	B5
H3	0	A13	B4
GND*	0	NC	GND (Bank 0)
F4	0	NC	VCCO (Bank 0)
G3	0	A14	B3
F3	0	NC	B2
H4	0	A15	B0
G4	0	CLK1/I	CLK1/I
H5	1	CLK2/I	CLK2/I
F5	1	B0	C0
G5	1	B1	C1
G6	1	B2	C2
H6	1	B3	C4
F6	1	B4	C5
H7	1	NC	C6
H8	-	TMS	TMS
G7	1	B5	C8
F7	1	B6	C10
G8	1	B7	C11
GND*	1	GND (Bank 0)	GND (Bank 1)
F8	1	NC	C12
D6	1	VCCO (Bank 1)	VCCO (Bank 1)
E8	1	B8	D15

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
A1	-	TDI
B1	0	A8
B2	0	A10
B3	0	A11
GND*	0	GND (Bank 0)
C1	0	A12
C3	0	VCCO (Bank 0)
C2	0	B15
D1	0	B14
D2	0	B13
D3	0	B12
E1	0	B11
E2	0	B10
E3	0	B9
F1	0	B8
F2	-	TCK
E4	-	VCC
GND*	-	GND
H2	0	B6
H1	0	B5
G1	0	B4
GND*	0	GND (Bank 0)
F3	0	VCCO (Bank 0)
G2	0	B3
G3	0	B2
H3	0	B0
G4	0	CLK1/I
F4	1	CLK2/I
H4	1	C0
H5	1	C1
G5	1	C2
H6	1	C4
H7	1	C5
H8	1	C6
G8	-	TMS
G7	1	C8
G6	1	C10
F8	1	C11
GND*	1	GND (Bank 1)
F7	1	C12
F6	1	VCCO (Bank 1)
F5	1	D15
E8	1	D14

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP (Cont.)**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
83	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
84	1	D3	H6	P12
85	1	D2	H4	P10
86	1	D1	H2	P6
87	1	D0/GOE1	H0/GOE1	P2/GOE1
88	1	CLK3/I	CLK3/I	CLK3/I
89	0	CLK0/I	CLK0/I	CLK0/I
90	-	VCC	VCC	VCC
91	0	A0/GOE0	A0/GOE0	A2/GOE0
92	0	A1	A2	A6
93	0	A2	A4	A10
94	0	A3	A6	A12
95	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
96	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
97	0	A4	A8	B2
98	0	A5	A10	B6
99	0	A6	A12	B10
100	0	A7	A14	B12

* This pin is input only.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
GND*	-	GND
A1	-	TDI
B1	0	VCCO (Bank 0)
D3	0	B0
C1	0	B1
D2	0	B2
D1	0	B4
E4	0	B5
F3	0	B6
E2	0	GND (Bank 0)
E1	0	B8
E3	0	B9
F4	0	B10
G4	0	B12
F2	0	B13
G3	0	B14
H4	0	VCCO (Bank 0)
F1	0	C14
G2	0	C13
G1	0	C12
H3	0	C10
J4	0	C9
H1	0	C8
H2	0	GND (Bank 0)
J3	0	C6
J1	0	C5
J2	0	C4
K3	0	C2
K2	0	C1
K1	0	C0
L2	0	VCCO (Bank 0)
L1	-	TCK
M1	-	VCC
GND*	-	GND
L3	0	D14
M2	0	D13
K4	0	D12
M3	0	D10
K5	0	D9
L4	0	D8
M4	0	GND (Bank 0)
J5	0	VCCO (Bank 0)
L5	0	D6

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

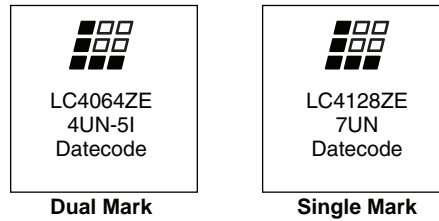
Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND
2	-	TDI	TDI
3	0	VCCO (Bank 0)	VCCO (Bank 0)
4	0	B0	C12
5	0	B1	C10
6	0	B2	C8
7	0	B4	C6
8	0	B5	C4
9	0	B6	C2
10	0	GND (Bank 0)	GND (Bank 0)
11	0	B8	D14
12	0	B9	D12
13	0	B10	D10
14	0	B12	D8
15	0	B13	D6
16	0	B14	D4
17*	0	NC	I
18	0	GND (Bank 0)	NC
19	0	VCCO (Bank 0)	VCCO (Bank 0)
20*	0	NC	I
21	0	C14	E2
22	0	C13	E4
23	0	C12	E6
24	0	C10	E8
25	0	C9	E10
26	0	C8	E12
27	0	GND (Bank 0)	GND (Bank 0)
28	0	C6	F2
29	0	C5	F4
30	0	C4	F6
31	0	C2	F8
32	0	C1	F10
33	0	C0	F12
34	0	VCCO (Bank 0)	VCCO (Bank 0)
35	-	TCK	TCK
36	-	VCC	VCC
37	-	GND	GND
38*	0	NC	I
39	0	D14	G12
40	0	D13	G10
41	0	D12	G8
42	0	D10	G6

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
86	1	F12	L8
87	1	F13	L6
88	1	F14	L4
89*	1	NC	I
90	1	GND (Bank 1)	NC
91	1	VCCO (Bank 1)	VCCO (Bank 1)
92*	1	NC	I
93	1	G14	M2
94	1	G13	M4
95	1	G12	M6
96	1	G10	M8
97	1	G9	M10
98	1	G8	M12
99	1	GND (Bank 1)	GND (Bank 1)
100	1	G6	N2
101	1	G5	N4
102	1	G4	N6
103	1	G2	N8
104	1	G1	N10
105	1	G0	N12
106	1	VCCO (Bank 1)	VCCO (Bank 1)
107	-	TDO	TDO
108	-	VCC	VCC
109	-	GND	GND
110*	1	NC	I
111	1	H14	O12
112	1	H13	O10
113	1	H12	O8
114	1	H10	O6
115	1	H9	O4
116	1	H8	O2
117*	1	NC	I
118	1	GND (Bank 1)	GND (Bank 1)
119	1	VCCO (Bank 1)	VCCO (Bank 1)
120	1	H6	P12
121	1	H5	P10
122	1	H4	P8
123	1	H2	P6
124	1	H1	P4
125	1	H0/GOE1	P2/GOE1
126	1	CLK3/I	CLK3/I
127	0	GND (Bank 0)	GND (Bank 0)
128	0	CLK0/I	CLK0/I

Figure 20. Mark Format for 64 ucBGA and 132 ucBGA Packages

Lead-Free Packaging
Commercial

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-4TN48C	32	1.8	4.4	Lead-Free TQFP	48	32	C
	LC4032ZE-5TN48C	32	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4032ZE-7TN48C	32	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4032ZE-4MN64C	32	1.8	4.4	Lead-Free csBGA	64	32	C
	LC4032ZE-5MN64C	32	1.8	5.8	Lead-Free csBGA	64	32	C
	LC4032ZE-7MN64C	32	1.8	7.5	Lead-Free csBGA	64	32	C
LC4064ZE	LC4064ZE-4TN48C	64	1.8	4.7	Lead-Free TQFP	48	32	C
	LC4064ZE-5TN48C	64	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4064ZE-7TN48C	64	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4064ZE-4TN100C	64	1.8	4.7	Lead-Free TQFP	100	64	C
	LC4064ZE-5TN100C	64	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4064ZE-7TN100C	64	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4064ZE-4MN64C	64	1.8	4.7	Lead-Free csBGA	64	48	C
	LC4064ZE-5MN64C	64	1.8	5.8	Lead-Free csBGA	64	48	C
	LC4064ZE-7MN64C	64	1.8	7.5	Lead-Free csBGA	64	48	C
	LC4064ZE-4MN144C	64	1.8	4.7	Lead-Free csBGA	144	64	C
LC4128ZE	LC4128ZE-5TN100C	128	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4128ZE-7TN100C	128	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4128ZE-5TN144C	128	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4128ZE-7TN144C	128	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4128ZE-5UMN132C	128	1.8	5.8	Lead-Free ucBGA	132	96	C
	LC4128ZE-7UMN132C	128	1.8	7.5	Lead-Free ucBGA	132	96	C
	LC4128ZE-5MN144C	128	1.8	5.8	Lead-Free csBGA	144	96	C
	LC4128ZE-7MN144C	128	1.8	7.5	Lead-Free csBGA	144	96	C
LC4256ZE	LC4256ZE-5TN100C	256	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4256ZE-7TN100C	256	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4256ZE-5TN144C	256	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4256ZE-7TN144C	256	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4256ZE-5MN144C	256	1.8	5.8	Lead-Free csBGA	144	108	C
	LC4256ZE-7MN144C	256	1.8	7.5	Lead-Free csBGA	144	108	C

Industrial

Device	Part Number	Macrocells	Voltage	t _{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I	
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, [ispMACH 4000ZE Timing Model Design and Usage Guidelines](#)
- TN1174, [Advanced Features of the ispMACH 4000ZE Family](#)
- TN1187, [Power Estimation in ispMACH 4000ZE Devices](#)
- [Package Diagrams](#)

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