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### **Understanding Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### **Applications of Embedded - CPLDs**

#### **Details**

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TFBGA, CSPBGA
Supplier Device Package	64-CSBGA (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032ze-5mn64i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032ze-5mn64i</a>

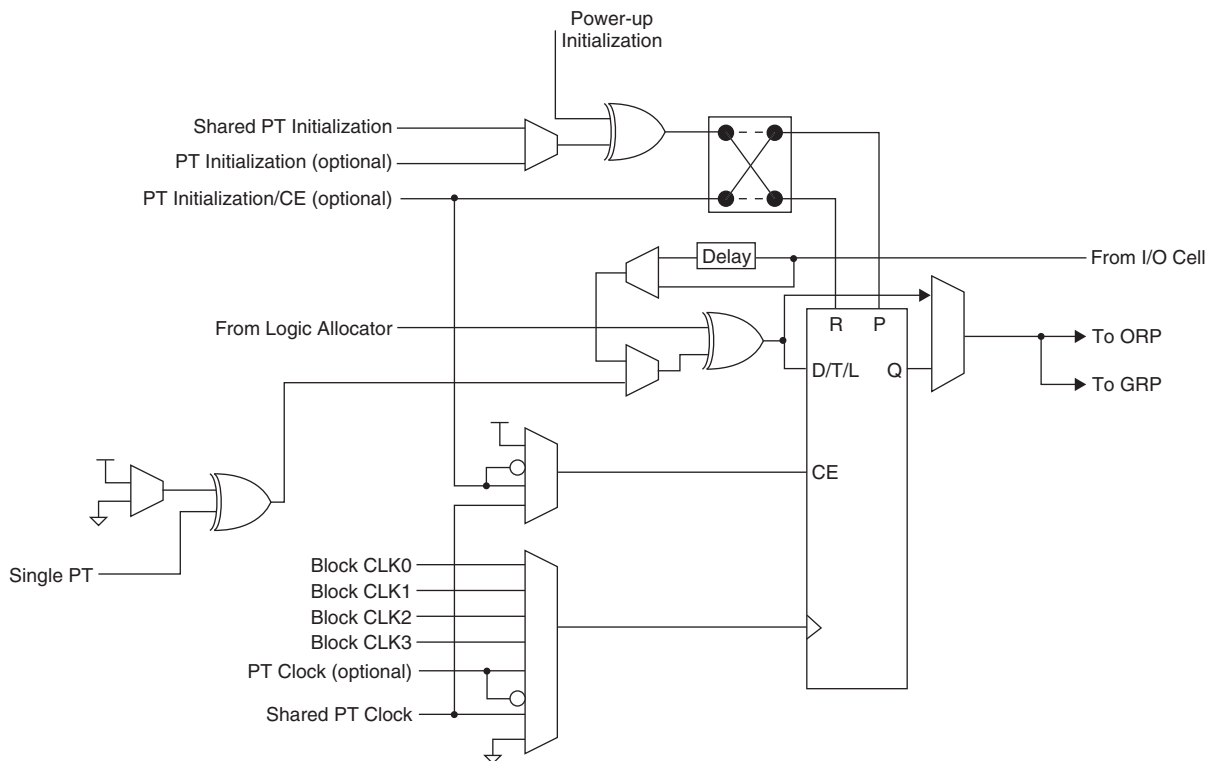
**Table 4. Product Term Expansion Capability**

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 $\tilde{\circ}$ M4 $\tilde{\circ}$ M8 $\tilde{\circ}$ M12 $\tilde{\circ}$ M0	75
Chain-1	M1 $\tilde{\circ}$ M5 $\tilde{\circ}$ M9 $\tilde{\circ}$ M13 $\tilde{\circ}$ M1	80
Chain-2	M2 $\tilde{\circ}$ M6 $\tilde{\circ}$ M10 $\tilde{\circ}$ M14 $\tilde{\circ}$ M2	75
Chain-3	M3 $\tilde{\circ}$ M7 $\tilde{\circ}$ M11 $\tilde{\circ}$ M15 $\tilde{\circ}$ M3	70

Every time the super cluster allocator is used, there is an incremental delay of  $t_{EXP}$ . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

## Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

**Figure 5. Macrocell**


## Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

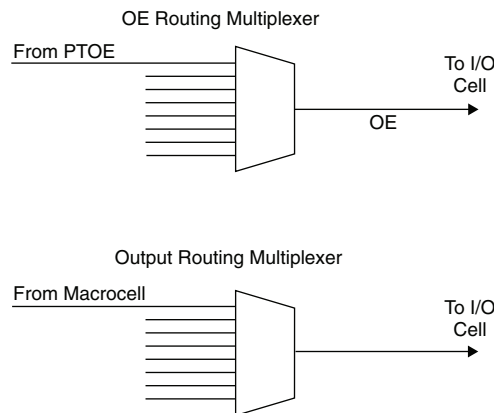
### Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. The enhanced ORP of the ispMACH 400ZE family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

**Figure 7. ORP Slice**



### Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-7 provide the connection details.

**Table 5. GLB/MC/ORP Combinations for ispMACH 4256ZE**

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 2]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 3]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 4]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 5]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 6]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 7]	M14, M15, M0, M1, M2, M3, M4, M5

**Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE**

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 4]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 5]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 6]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 7]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 8]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 9]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 10]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 11]	M14, M15, M0, M1, M2, M3, M4, M5

**Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE**

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M3, M4, M5, M6, M7, M8, M9, M10
[GLB] [MC 4]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 5]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 6]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 7]	M7, M8, M9, M10, M11, M12, M13, M14
[GLB] [MC 8]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 9]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 10]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 11]	M11, M12, M13, M14, M15, M0, M1, M2
[GLB] [MC 12]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 13]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 14]	M14, M15, M0, M1, M2, M3, M4, M5
[GLB] [MC 15]	M15, M0, M1, M2, M3, M4, M5, M6

## Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

## I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

## I/O Recommended Operating Conditions

Standard	V <sub>CCO</sub> (V) <sup>1</sup>	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
LVC MOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V<sub>CCO</sub> are the average of the min. and max. values.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>IL</sub> , I <sub>IH</sub> <sup>1,2</sup>	Input Leakage Current	0 ≤ V <sub>IN</sub> < V <sub>CCO</sub>	—	0.5	1	μA
I <sub>IH</sub> <sup>1</sup>	Input High Leakage Current	V <sub>CCO</sub> < V <sub>IN</sub> ≤ 5.5V	—	—	10	μA
I <sub>PU</sub>	I/O Weak Pull-up Resistor Current	0 ≤ V <sub>IN</sub> ≤ 0.7V <sub>CCO</sub>	-20	—	-150	μA
I <sub>PD</sub>	I/O Weak Pull-down Resistor Current	V <sub>IL</sub> (MAX) ≤ V <sub>IN</sub> ≤ V <sub>IH</sub> (MAX)	30	—	150	μA
I <sub>BHLS</sub>	Bus Hold Low Sustaining Current	V <sub>IN</sub> = V <sub>IL</sub> (MAX)	30	—	—	μA
I <sub>BHHS</sub>	Bus Hold High Sustaining Current	V <sub>IN</sub> = 0.7 V <sub>CCO</sub>	-20	—	—	μA
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	0V ≤ V <sub>IN</sub> ≤ V <sub>BHT</sub>	—	—	150	μA
I <sub>BHHO</sub>	Bus Hold High Overdrive Current	V <sub>BHT</sub> ≤ V <sub>IN</sub> ≤ V <sub>CCO</sub>	—	—	-150	μA
V <sub>BHT</sub>	Bus Hold Trip Points	—	V <sub>CCO</sub> * 0.35	—	V <sub>CCO</sub> * 0.65	V
C <sub>1</sub>	I/O Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	
C <sub>2</sub>	Clock Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	
C <sub>3</sub>	Global Input Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	

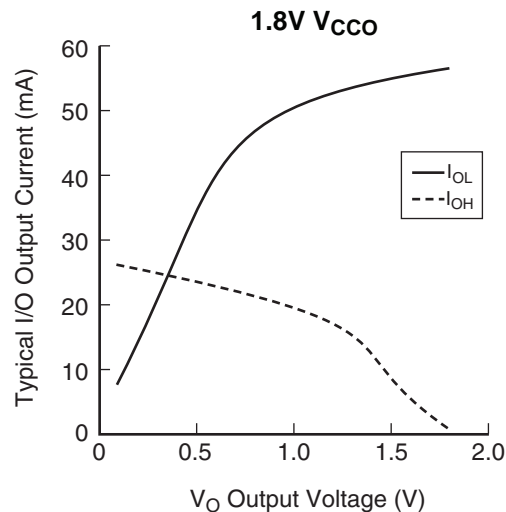
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I<sub>IH</sub> excursions of up to 1.5μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T<sub>A</sub> = 25°C, f = 1.0MHz.

## I/O DC Electrical Characteristics

### Over Recommended Operating Conditions

Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$ Max (V)	$V_{OH}$ Min (V)	$I_{OL}^1$ (mA)	$I_{OH}^1$ (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTTL	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	$V_{CCO} - 0.40$	8.0	-4.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
LVCMOS 1.5 <sup>2</sup>	-0.3	$0.35 * V_{CC}$	$0.65 * V_{CC}$	3.6	0.40	$V_{CCO} - 0.45$	2.0	-2.0
					0.20	$V_{CCO} - 0.20$	0.1	-0.1
PCI 3.3	-0.3	$0.3 * 3.3 * (V_{CC} / 1.8)$	$0.5 * 3.3 * (V_{CC} / 1.8)$	5.5	$0.1 V_{CCO}$	$0.9 V_{CCO}$	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed  $n * 8\text{mA}$ . Where  $n$  is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from  $V_{CC}$ , if the ispMACH 4000ZE  $V_{CC}$  and the  $V_{CC}$  of the driving device ( $V_{CCd-d}$ ; that determines steady state  $V_{IH}$ ) are in the extreme range of their specifications. Typically, DC current drawn from  $V_{CC}$  will be  $2\mu\text{A}$  per input.



## Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t <sub>BTCP</sub>	TCK [BSCAN test] clock cycle	40	—	ns
t <sub>BTCH</sub>	TCK [BSCAN test] pulse width high	20	—	ns
t <sub>BTCL</sub>	TCK [BSCAN test] pulse width low	20	—	ns
t <sub>BTSU</sub>	TCK [BSCAN test] setup time	8	—	ns
t <sub>BTH</sub>	TCK [BSCAN test] hold time	10	—	ns
t <sub>BRF</sub>	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTOZ</sub>	TAP controller falling edge of clock to data output disable	—	10	ns
t <sub>BTVO</sub>	TAP controller falling edge of clock to data output enable	—	10	ns
t <sub>BTCPsu</sub>	BSCAN test Capture register setup time	8	—	ns
t <sub>BTCPH</sub>	BSCAN test Capture register hold time	10	—	ns
t <sub>BTUCO</sub>	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t <sub>BTUOZ</sub>	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t <sub>BTUOV</sub>	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

## Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V <sub>CC</sub>	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V <sub>CC00</sub> , V <sub>CC01</sub>	The power supply pins for each I/O bank.	
yzz	Input/Output <sup>1</sup> – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

## ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8



**ispMACH 4000ZE Power Supply and NC Connections<sup>1</sup> (Cont.)**

Signal	132 ucBGA <sup>3</sup>	144 csBGA <sup>3</sup>	144 TQFP <sup>2</sup>
VCC	M1, M7, A12, B5	H5, H8, E8, E5	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	B1, H4, L2, J5, A4	E4, F4, G4, J5, D5	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	K9, L12, F12, D9, C7	J8, H9, G9, F9, D8	64, 75, 91, 106, 119
GND	E5, E8, H5, H8	F6, G6, G7, F7	1, 37, 73, 109
GND (Bank 0)	E2, H2, M4, B7, B3	G5, H4, H6, E6, F5	10, 18 <sup>4</sup> , 27, 46, 127, 137
GND (Bank 1)	L7, J9, H12, E9, A9	H7, J9, G8, F8, E7	55, 65, 82, 90 <sup>4</sup> , 99, 118
NC	—	<b>4064ZE:</b> E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 <b>4128ZE:</b> D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2	<b>4128ZE:</b> 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 <b>4256ZE:</b> 18, 90

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

**ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA (Cont.)**

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
E7	1	NC	D14
E6	1	B9	D13
D7	1	B10	D12
D8	1	NC	D11
C5	1	NC	D10
C7	1	B11	D9
C8	1	NC	D8
B8	-	TDO	TDO
D5	-	VCC	VCC
GND*	-	GND	GND
A8	1	B12	D7
A7	1	NC	D6
B7	1	NC	D5
A6	1	B13	D4
GND*	1	NC	GND (Bank 1)
C6	1	NC	VCCO (Bank 1)
B6	1	B14	D3
A5	1	NC	D2
B5	1	B15/GOE1	D0/GOE1
A4	1	CLK3/I	CLK3/I
C4	0	CLK0/I	CLK0/I
B4	0	A0/GOE0	A0/GOE0
B3	0	A1	A1
A3	0	A2	A2
A2	0	A3	A4
A1	0	A4	A6

\* All bonded grounds are connected to the following two balls, D4 and E5.

**ispMACH 4064ZE Logic Signal Connections: 64 ucBGA**

Ball Number	Bank Number	GLB/MC/Pad
A1	-	TDI
B1	0	A8
B2	0	A10
B3	0	A11
GND*	0	GND (Bank 0)
C1	0	A12
C3	0	VCCO (Bank 0)
C2	0	B15
D1	0	B14
D2	0	B13
D3	0	B12
E1	0	B11
E2	0	B10
E3	0	B9
F1	0	B8
F2	-	TCK
E4	-	VCC
GND*	-	GND
H2	0	B6
H1	0	B5
G1	0	B4
GND*	0	GND (Bank 0)
F3	0	VCCO (Bank 0)
G2	0	B3
G3	0	B2
H3	0	B0
G4	0	CLK1/I
F4	1	CLK2/I
H4	1	C0
H5	1	C1
G5	1	C2
H6	1	C4
H7	1	C5
H8	1	C6
G8	-	TMS
G7	1	C8
G6	1	C10
F8	1	C11
GND*	1	GND (Bank 1)
F7	1	C12
F6	1	VCCO (Bank 1)
F5	1	D15
E8	1	D14

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
 100 TQFP**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND	GND
2	-	TDI	TDI	TDI
3	0	A8	B0	C12
4	0	A9	B2	C10
5	0	A10	B4	C6
6	0	A11	B6	C2
7	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
8	0	A12	B8	D12
9	0	A13	B10	D10
10	0	A14	B12	D6
11	0	A15	B13	D4
12*	0	I	I	I
13	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
14	0	B15	C14	E4
15	0	B14	C12	E6
16	0	B13	C10	E10
17	0	B12	C8	E12
18	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
19	0	B11	C6	F2
20	0	B10	C5	F6
21	0	B9	C4	F10
22	0	B8	C2	F12
23*	0	I	I	I
24	-	TCK	TCK	TCK
25	-	VCC	VCC	VCC
26	-	GND	GND	GND
27*	0	I	I	I
28	0	B7	D13	G12
29	0	B6	D12	G10
30	0	B5	D10	G6
31	0	B4	D8	G2
32	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
33	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
34	0	B3	D6	H12
35	0	B2	D4	H10
36	0	B1	D2	H6
37	0	B0	D0	H2
38	0	CLK1/I	CLK1/I	CLK1/I
39	1	CLK2/I	CLK2/I	CLK2/I
40	-	VCC	VCC	VCC
41	1	C0	E0	I2

**ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

**ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

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**ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
A2	0	A14

\* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
144 csBGA (Cont.)**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J12	1	NC Ball	NC Ball	L14
J11	1	NC Ball	NC Ball	L12
H10	1	NC Ball	F8	L10
H12	1	C12	F9	L8
G11	1	C13	F10	L6
H11	1	C14	F12	L4
G12	1	C15	F13	L2
G10*	1	I	F14	L0
G9	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
F12	1	D15	G14	M0
F11	1	D14	G13	M2
E11	1	D13	G12	M4
E12	1	D12	G10	M6
D10	1	NC Ball	G9	M8
F10	1	NC Ball	G8	M10
D12	1	NC Ball	NC Ball	M12
F8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
E10	1	D11	G6	N2
D11	1	D10	G5	N4
E9	1	D9	G4	N6
C12	1	D8	G2	N8
C11*	1	I	G1	N10
B12	1	NC Ball	G0	N12
F9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
B11	-	TDO	TDO	TDO
E8	-	VCC	VCC	VCC
F7	-	GND	GND	GND
A12	1	NC Ball	NC Ball	O14
C10	1	NC Ball	NC Ball	O12
B10	1	NC Ball	H14	O10
A11*	1	I	H13	O8
D9	1	D7	H12	O6
B9	1	D6	H10	O4
C9	1	D5	H9	O2
A10	1	D4	H8	O0
E7	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
D8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
A9	1	NC Ball	H6	P12
B8	1	NC Ball	H5	P10
C8	1	D3	H4	P8
A8	1	D2	H2	P6
D7	1	D1	H1	P4
B7	1	D0/GOE1	H0/GOE1	P2/GOE1



**ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

**ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)**

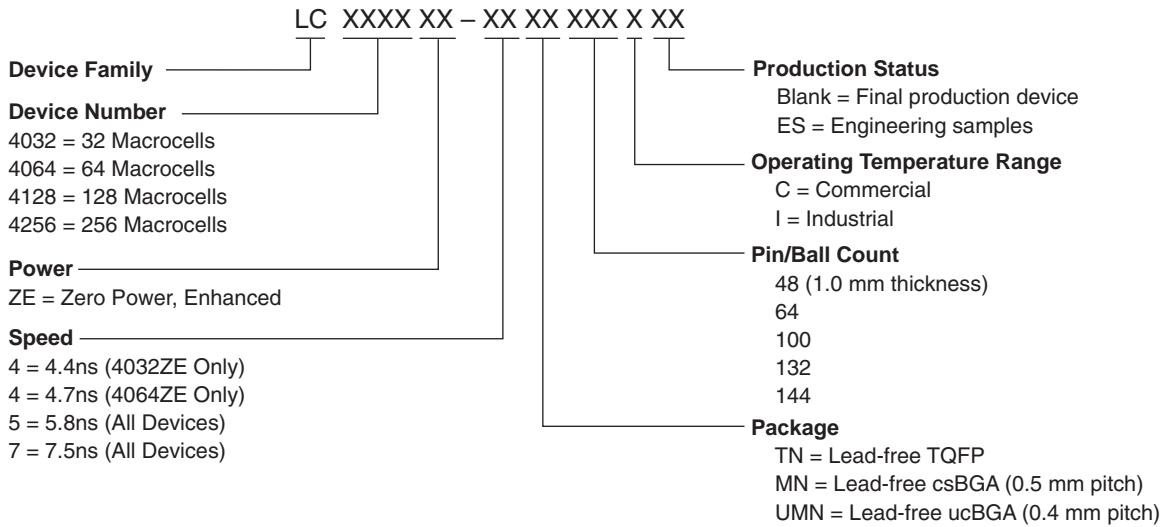
Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
86	1	F12	L8
87	1	F13	L6
88	1	F14	L4
89*	1	NC	I
90	1	GND (Bank 1)	NC
91	1	VCCO (Bank 1)	VCCO (Bank 1)
92*	1	NC	I
93	1	G14	M2
94	1	G13	M4
95	1	G12	M6
96	1	G10	M8
97	1	G9	M10
98	1	G8	M12
99	1	GND (Bank 1)	GND (Bank 1)
100	1	G6	N2
101	1	G5	N4
102	1	G4	N6
103	1	G2	N8
104	1	G1	N10
105	1	G0	N12
106	1	VCCO (Bank 1)	VCCO (Bank 1)
107	-	TDO	TDO
108	-	VCC	VCC
109	-	GND	GND
110*	1	NC	I
111	1	H14	O12
112	1	H13	O10
113	1	H12	O8
114	1	H10	O6
115	1	H9	O4
116	1	H8	O2
117*	1	NC	I
118	1	GND (Bank 1)	GND (Bank 1)
119	1	VCCO (Bank 1)	VCCO (Bank 1)
120	1	H6	P12
121	1	H5	P10
122	1	H4	P8
123	1	H2	P6
124	1	H1	P4
125	1	H0/GOE1	P2/GOE1
126	1	CLK3/I	CLK3/I
127	0	GND (Bank 0)	GND (Bank 0)
128	0	CLK0/I	CLK0/I

**ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

\* This pin is input only for the LC4256ZE.

## Part Number Description



## ispMACH 400ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

## Ordering Information

Note: ispMACH 400ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages

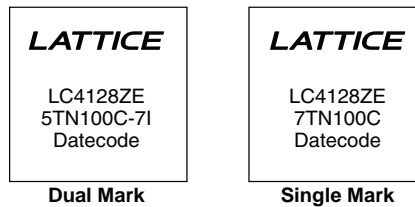
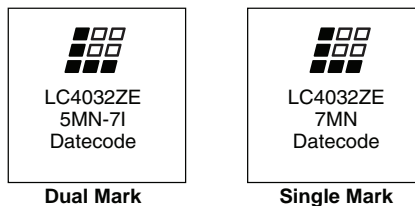
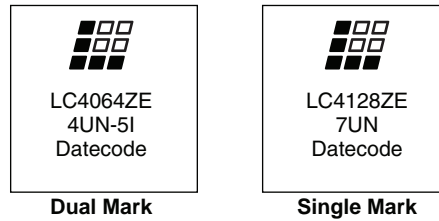


Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages



**Figure 20. Mark Format for 64 ucBGA and 132 ucBGA Packages**


## Lead-Free Packaging

### Commercial

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-4TN48C	32	1.8	4.4	Lead-Free TQFP	48	32	C
	LC4032ZE-5TN48C	32	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4032ZE-7TN48C	32	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4032ZE-4MN64C	32	1.8	4.4	Lead-Free csBGA	64	32	C
	LC4032ZE-5MN64C	32	1.8	5.8	Lead-Free csBGA	64	32	C
	LC4032ZE-7MN64C	32	1.8	7.5	Lead-Free csBGA	64	32	C
LC4064ZE	LC4064ZE-4TN48C	64	1.8	4.7	Lead-Free TQFP	48	32	C
	LC4064ZE-5TN48C	64	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4064ZE-7TN48C	64	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4064ZE-4TN100C	64	1.8	4.7	Lead-Free TQFP	100	64	C
	LC4064ZE-5TN100C	64	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4064ZE-7TN100C	64	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4064ZE-4MN64C	64	1.8	4.7	Lead-Free csBGA	64	48	C
	LC4064ZE-5MN64C	64	1.8	5.8	Lead-Free csBGA	64	48	C
	LC4064ZE-7MN64C	64	1.8	7.5	Lead-Free csBGA	64	48	C
	LC4064ZE-4MN144C	64	1.8	4.7	Lead-Free csBGA	144	64	C
LC4064ZE-5MN144C	64	1.8	5.8	Lead-Free csBGA	144	64	C	
LC4064ZE-7MN144C	64	1.8	7.5	Lead-Free csBGA	144	64	C	
LC4128ZE	LC4128ZE-5TN100C	128	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4128ZE-7TN100C	128	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4128ZE-5TN144C	128	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4128ZE-7TN144C	128	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4128ZE-5UMN132C	128	1.8	5.8	Lead-Free ucBGA	132	96	C
	LC4128ZE-7UMN132C	128	1.8	7.5	Lead-Free ucBGA	132	96	C
	LC4128ZE-5MN144C	128	1.8	5.8	Lead-Free csBGA	144	96	C
	LC4128ZE-7MN144C	128	1.8	7.5	Lead-Free csBGA	144	96	C
LC4256ZE	LC4256ZE-5TN100C	256	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4256ZE-7TN100C	256	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4256ZE-5TN144C	256	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4256ZE-7TN144C	256	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4256ZE-5MN144C	256	1.8	5.8	Lead-Free csBGA	144	108	C
	LC4256ZE-7MN144C	256	1.8	7.5	Lead-Free csBGA	144	108	C