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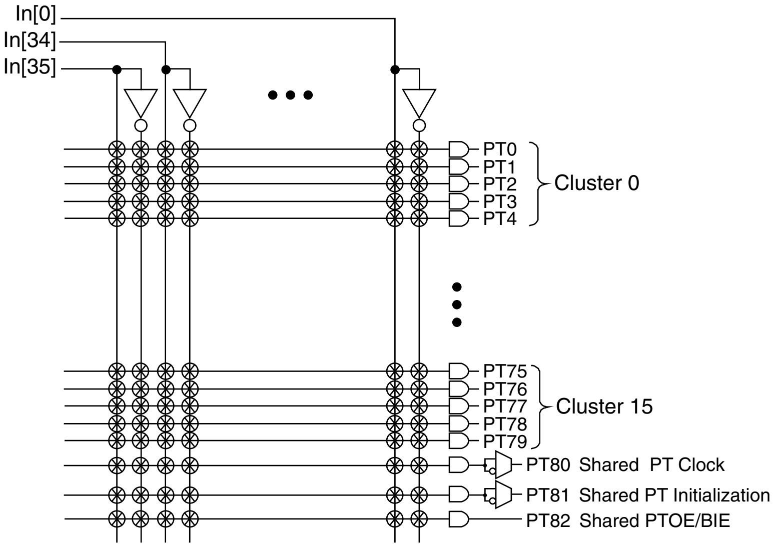
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TFBGA, CSPBGA
Supplier Device Package	64-CSBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4032ze-7mn64i

Figure 3. AND Array



Note:
⊗ Indicates programmable fuse.

Enhanced Logic Allocator

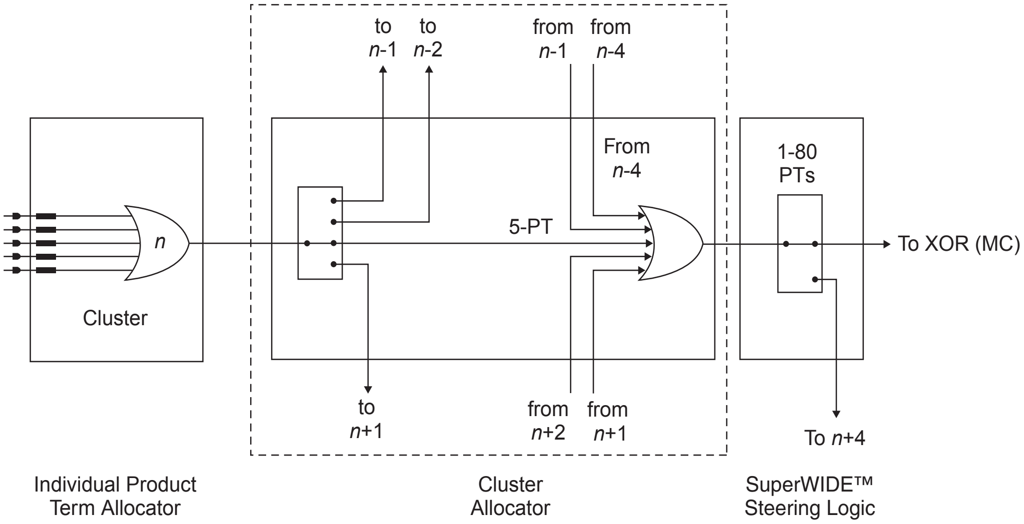
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

Table 2. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 3. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000ZE family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be "stolen" from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000ZE device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator

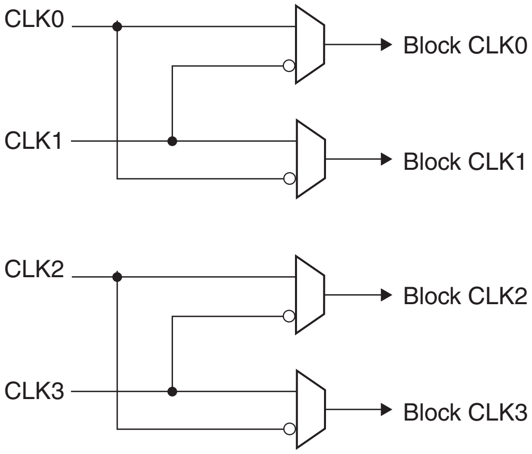


Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 4]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 5]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 6]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 7]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 8]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 9]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 10]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 11]	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M3, M4, M5, M6, M7, M8, M9, M10
[GLB] [MC 4]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 5]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 6]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 7]	M7, M8, M9, M10, M11, M12, M13, M14
[GLB] [MC 8]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 9]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 10]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 11]	M11, M12, M13, M14, M15, M0, M1, M2
[GLB] [MC 12]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 13]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 14]	M14, M15, M0, M1, M2, M3, M4, M5
[GLB] [MC 15]	M15, M0, M1, M2, M3, M4, M5, M6

Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macrocell device (with 16 blocks), each block's BIE signal is driven by block-level OE PT from each block.

Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE

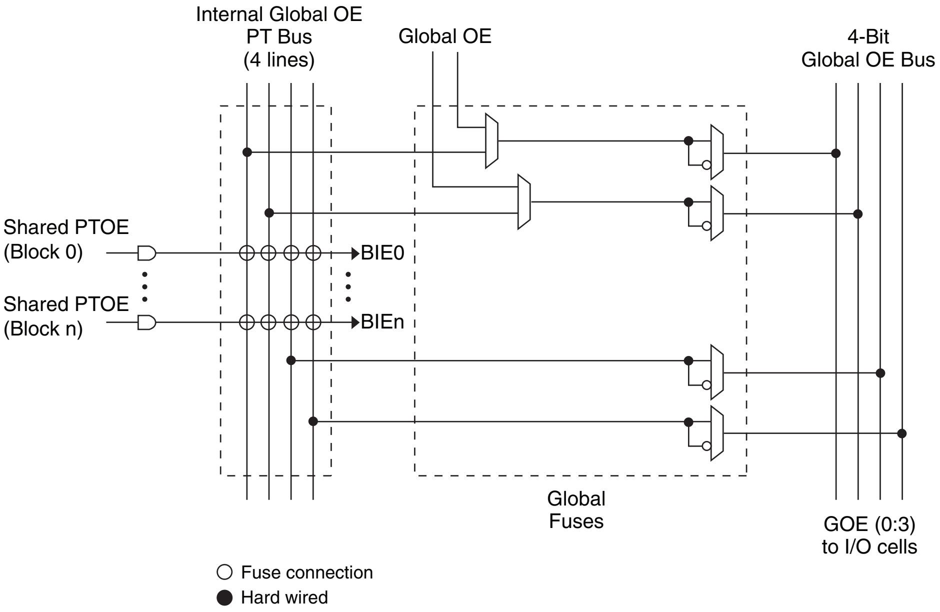
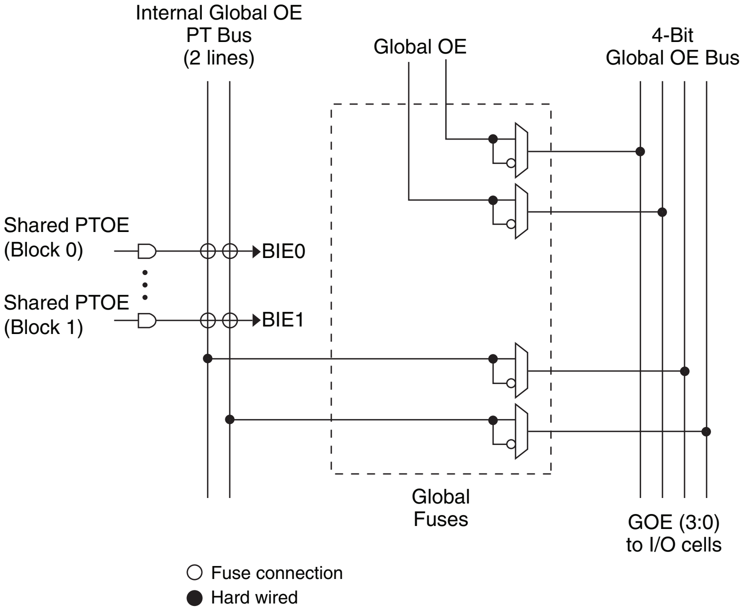


Figure 12. Global OE Generation for ispMACH 4032ZE



On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

Table 12. OSC and TIMER MC Designation

Device	Macrocell	Block Number	MC Number
ispMACH 4032ZE	OSC MC TIMER MC	A B	15 15
ispMACH 4064ZE	OSC MC TIMER MC	A D	15 15
ispMACH 4128ZE	OSC MC TIMER MC	A G	15 15
ispMACH 4256ZE	OSC MC TIMER MC	C F	15 15

Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . -0.5 to 5.5V

Storage Temperature . . . .-65 to 150°C

Junction Temperature (T_j) with Power Applied . . .-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
LVCMOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input Leakage Current	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-20	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-20	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T_A = 25°C, f = 1.0MHz.

ispMACH 4000ZE Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	LC4032ZE		LC4064ZE		Units
		-4		-4		
		Min.	Max.	Min.	Max.	
In/Out Delays						
t_{IN}	Input Buffer Delay	—	0.85	—	0.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	ns
t_{GOE}	Global OE Pin Delay	—	2.25	—	2.25	ns
t_{BUF}	Delay through Output Buffer	—	0.75	—	0.90	ns
t_{EN}	Output Enable Time	—	2.25	—	2.25	ns
t_{DIS}	Output Disable Time	—	1.35	—	1.35	ns
t_{PGSU}	Input Power Guard Setup Time	—	3.30	—	3.55	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	5.00	—	5.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dissertation	—	5.00	—	5.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	1.60	—	1.70	ns
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.90	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.55	—	0.55	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_{S}	D-Register Setup Time (Global Clock)	0.70	—	0.85	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.25	—	1.85	—	ns
t_{H}	D-Register Hold Time	1.50	—	1.65	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	0.90	—	1.05	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.45	—	1.65	—	ns
t_{HT}	T-Resister Hold Time	1.50	—	1.65	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.85	—	0.80	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.15	—	1.30	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.90	—	1.10	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.35	—	0.40	ns
t_{CES}	Clock Enable Setup Time	1.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.70	—	0.95	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.45	—	1.85	—	ns
t_{HL}	Latch Hold Time	1.40	—	1.80	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.35	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.30	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.30	—	0.30	ns

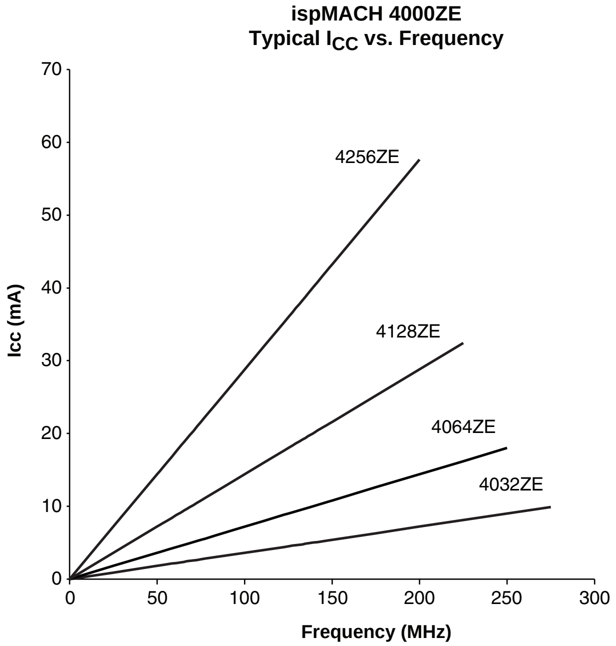
ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		All Devices				Units
			-5		-7		
			Min.	Max.	Min.	Max.	
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

Power Consumption



Power Estimation Coefficients[1]

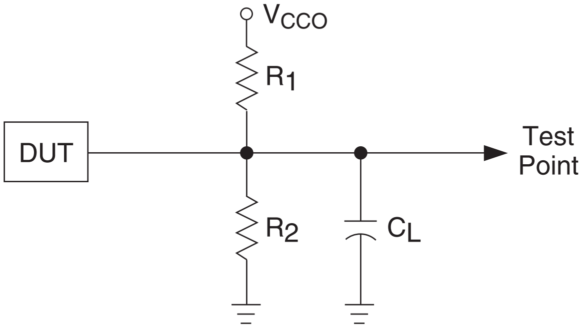
Device	A	B
ispMACH 4032ZE	0.010	0.009
ispMACH 4064ZE	0.011	0.009
ispMACH 4128ZE	0.012	0.009
ispMACH 4256ZE	0.013	0.009

1. For further information about the use of these coefficients, refer to TN1187, Power Estimation in ispMACH 4000ZE Devices.

Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

Figure 17. Output Test Load, LVTTL and LVCMOS Standards



0213A/ispm4k

Table 13. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $\frac{V_{CCO}}{2}$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $\frac{V_{CCO}}{2}$	LVCMOS 1.8 = 1.65V
				LVCMOS 1.5 = $\frac{V_{CCO}}{2}$	LVCMOS 1.5 = 1.4V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
A2	0	A14

* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
F6	-	GND	GND	GND
A1	-	TDI	TDI	TDI
E4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
B2	0	NC Ball	B0	C12
B1	0	NC Ball	B1	C10
C3	0	A8	B2	C8
C2	0	A9	B4	C6
C1	0	A10	B5	C4
D1	0	A11	B6	C2
G5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
D2	0	NC Ball	NC Ball	D14
D3	0	NC Ball	NC Ball	D12
E1	0	NC Ball	B8	D10
E2	0	A12	B9	D8
F2	0	A13	B10	D6
D4	0	A14	B12	D4
F1	0	A15	B13	D2
F3*	0	I	B14	D0
F4	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
G1	0	B15	C14	E0
E3	0	B14	C13	E2
G2	0	B13	C12	E4
G3	0	B12	C10	E6
H1	0	NC Ball	C9	E8
H3	0	NC Ball	C8	E10
H2	0	NC Ball	NC Ball	E12
H4	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J1	0	B11	C6	F2
J3	0	B10	C5	F4
J2	0	B9	C4	F6
K1	0	B8	C2	F8
K2*	0	I	C1	F10
L1	0	NC Ball	C0	F12
G4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
L2	-	TCK	TCK	TCK
H5	-	VCC	VCC	VCC
G6	-	GND	GND	GND
M1	0	NC Ball	NC Ball	G14
K3	0	NC Ball	NC Ball	G12
M2	0	NC Ball	D14	G10
L3*	0	I	D13	G8

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.

Industrial

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
	LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

Technical Support Assistance

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