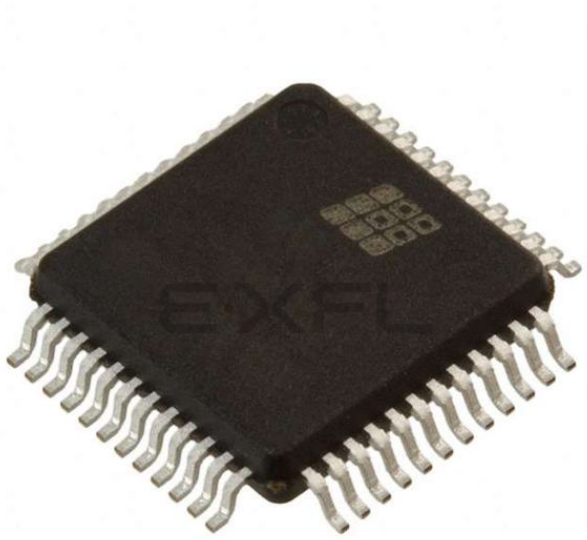


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.7 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-4tn48c

Introduction

The high performance ispMACH 4000ZE family from Lattice offers an ultra low power CPLD solution. The new family is based on Lattice's industry-leading ispMACH 4000 architecture. Retaining the best of the previous generation, the ispMACH 4000ZE architecture focuses on significant innovations to combine high performance with low power in a flexible CPLD family. For example, the family's new Power Guard feature minimizes dynamic power consumption by preventing internal logic toggling due to unnecessary I/O pin activity.

The ispMACH 4000ZE combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000ZE family offers densities ranging from 32 to 256 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA), and Ultra Chip Scale BGA (ucBGA) packages ranging from 32 to 144 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

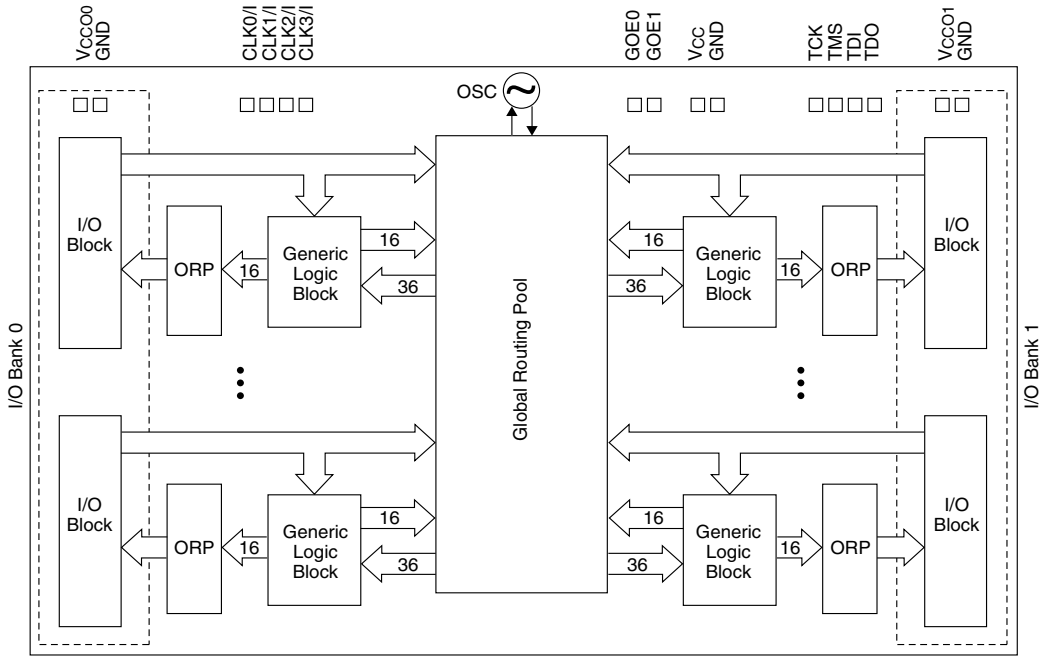
A user programmable internal oscillator and a timer are included in the device for tasks like LED control, keyboard scanner and similar housekeeping type state machines. This feature can be optionally disabled to save power.

The ispMACH 4000ZE family has enhanced system integration capabilities. It supports a 1.8V supply voltage and 3.3V, 2.5V, 1.8V and 1.5V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000ZE also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a "per-pin" basis. The ispMACH 4000ZE family members are 1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000ZE devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

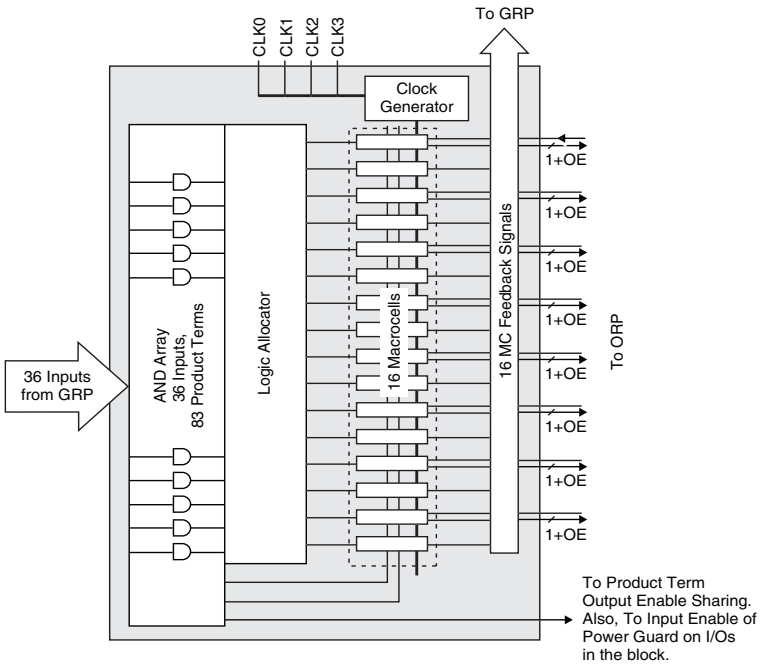
Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

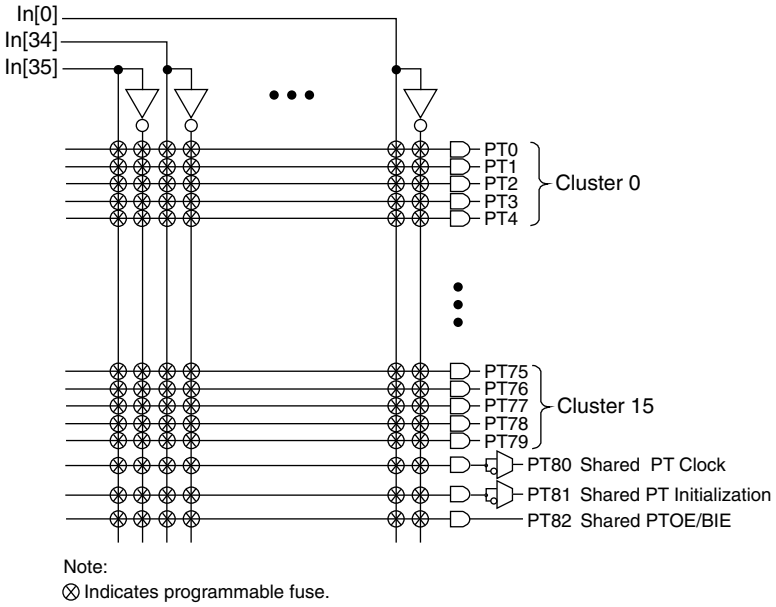


AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array



Enhanced Logic Allocator

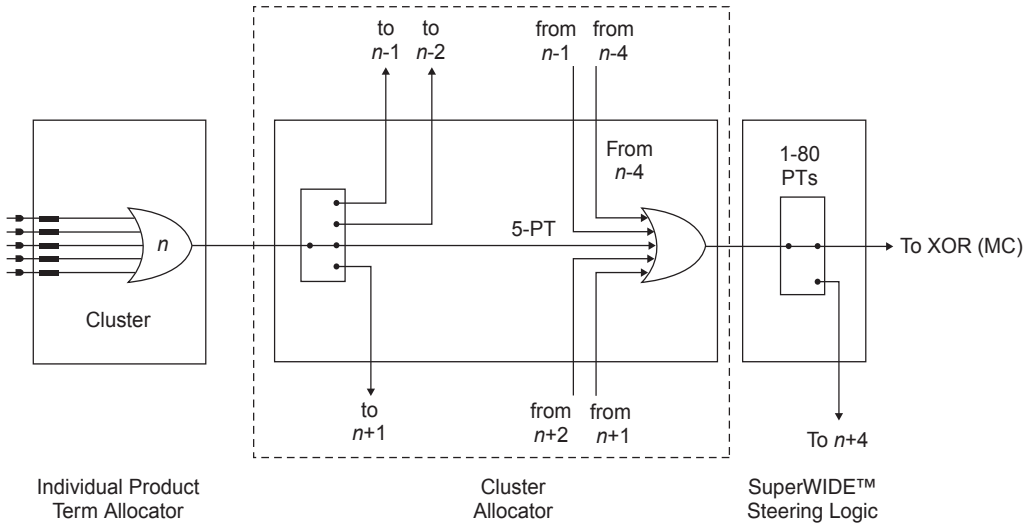
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

Table 2. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 3. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 4]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 5]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 6]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 7]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 8]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 9]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 10]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 11]	M14, M15, M0, M1, M2, M3, M4, M5

Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M1, M2, M3, M4, M5, M6, M7, M8
[GLB] [MC 2]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 3]	M3, M4, M5, M6, M7, M8, M9, M10
[GLB] [MC 4]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 5]	M5, M6, M7, M8, M9, M10, M11, M12
[GLB] [MC 6]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 7]	M7, M8, M9, M10, M11, M12, M13, M14
[GLB] [MC 8]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 9]	M9, M10, M11, M12, M13, M14, M15, M0
[GLB] [MC 10]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 11]	M11, M12, M13, M14, M15, M0, M1, M2
[GLB] [MC 12]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 13]	M13, M14, M15, M0, M1, M2, M3, M4
[GLB] [MC 14]	M14, M15, M0, M1, M2, M3, M4, M5
[GLB] [MC 15]	M15, M0, M1, M2, M3, M4, M5, M6

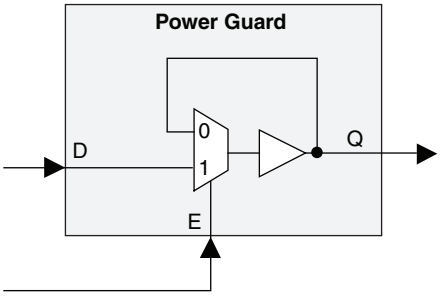
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 9. Power Guard

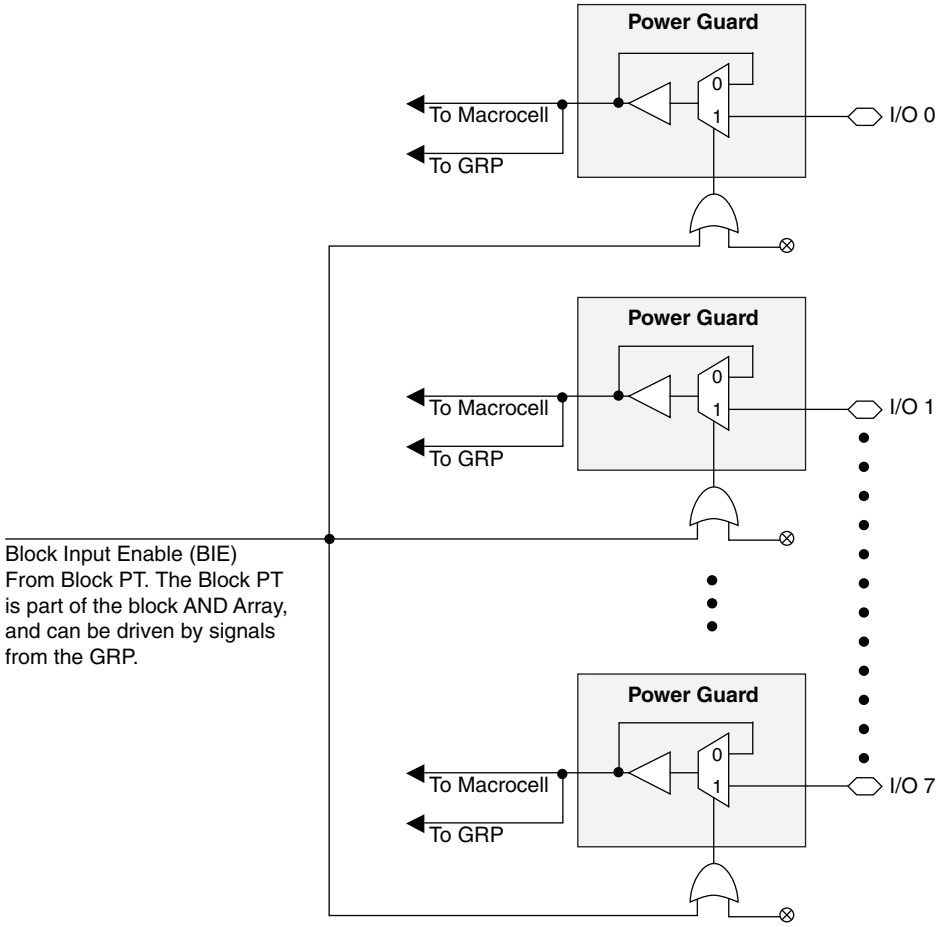


All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os



The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macrocell device (with 16 blocks), each block's BIE signal is driven by block-level OE PT from each block.

Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE

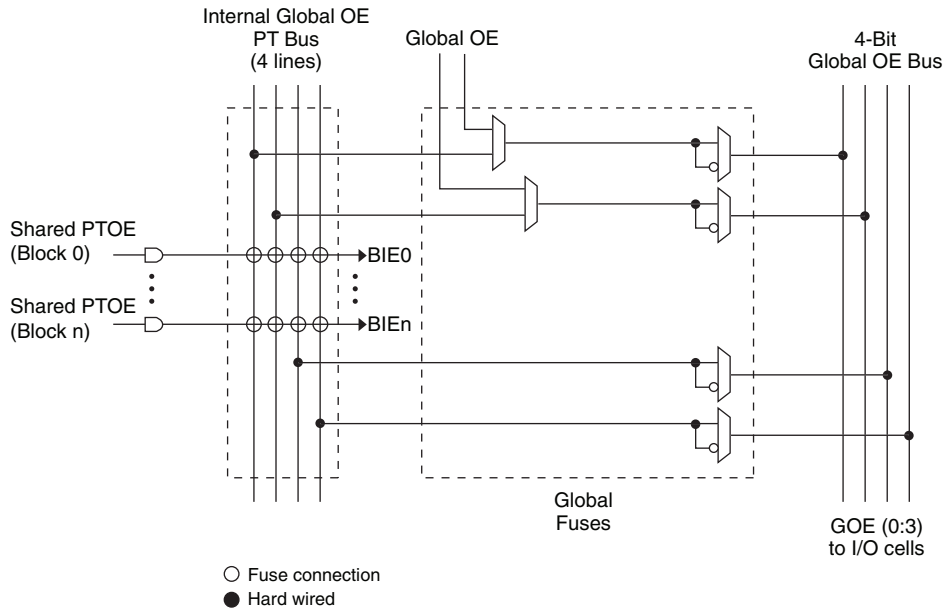
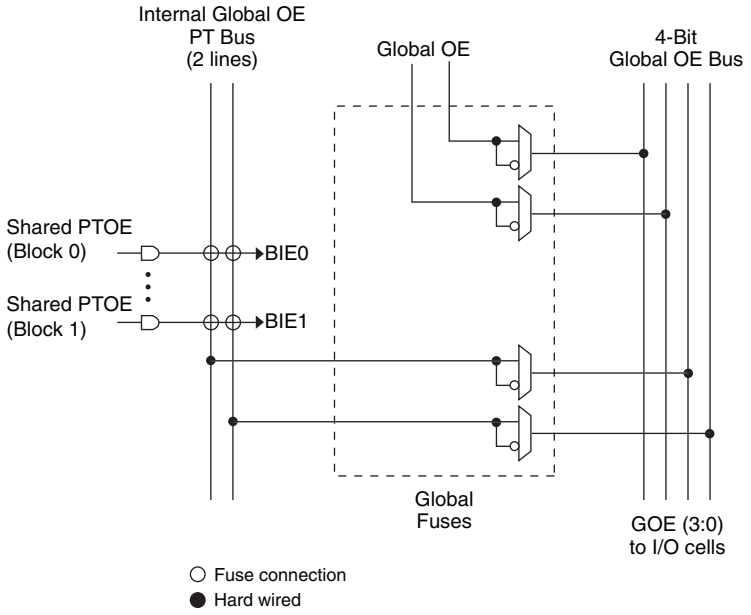


Figure 12. Global OE Generation for ispMACH 4032ZE



On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
LVCMOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input Leakage Current	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-20	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-20	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T_A = 25°C, f = 1.0MHz.

Supply Current

To minimize transient current during power-on, configure CPLD I/Os to a pull-up or float state. If this logic scenario is not possible, then the recommended power sequence should assert VCC and VCCO at the same time or VCC before VCCO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	60	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	13	25	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	15	40	µA
ispMACH 4064ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	92	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	15	30	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	18	50	µA
ispMACH 4128ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	195	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	16	40	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	19	60	µA
ispMACH 4256ZE						
$ICC^{1, 2, 3, 5, 6}$	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	372	—	µA
$ICC^{4, 5, 6}$	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	32	65	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	43	100	µA

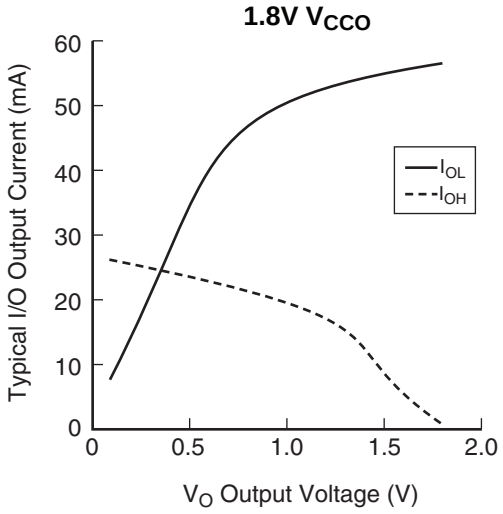
1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15µA typical current plus additional current from any logic it drives.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.5[2]	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from V_{CC}, if the ispMACH 4000ZE V_{CC} and the V_{CC} of the driving device (V_{CC}d-d; that determines steady state V_{IH}) are in the extreme range of their specifications. Typically, DC current drawn from V_{CC} will be 2µA per input.



ispMACH 4000ZE External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1, 2]	LC4032ZE		LC4064ZE		All Devices				Units
		-4		-4		-5		-7		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	20-PT combinatorial propagation delay	—	4.4	—	4.7	—	5.8	—	7.5	ns
t_S	GLB register setup time before clock	2.2	—	2.5	—	2.9	—	4.5	—	ns
t_{ST}	GLB register setup time before clock with T-type register	2.4	—	2.7	—	3.1	—	4.7	—	ns
t_{SIR}	GLB register setup time before clock, input register path	1.0	—	1.1	—	1.3	—	1.4	—	ns
t_{SIRZ}	GLB register setup time before clock with zero hold	2.0	—	2.1	—	2.9	—	4.0	—	ns
t_H	GLB register hold time after clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HT}	GLB register hold time after clock with T-type register	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time after clock, input register path	1.0	—	1.0	—	1.3	—	1.3	—	ns
t_{HIRZ}	GLB register hold time after clock, input register path with zero hold	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.0	—	3.2	—	3.8	—	4.5	ns
t_R	External reset pin to output delay	—	5.0	—	6.0	—	7.5	—	9.0	ns
t_{RW}	External reset pulse duration	1.5	—	1.7	—	2.0	—	4.0	—	ns
$t_{PTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	8.0	—	8.2	—	9.0	ns
$t_{GPTOE/DIS}$	Input to output global product term output enable/disable	—	6.5	—	7.0	—	10.0	—	10.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	4.5	—	5.5	—	7.0	ns
t_{CW}	Global clock width, high or low	1.0	—	1.5	—	1.8	—	2.8	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.0	—	1.5	—	1.8	—	2.8	—	ns
t_{WIR}	Input register clock width, high or low	1.0	—	1.5	—	1.8	—	2.8	—	ns
f_{MAX} (Int.)[3]	Clock frequency with internal feedback	—	260	—	241	—	200	—	172	MHz
f_{MAX} (Ext.)	clock frequency with external feedback, $[1 / (t_S + t_{CO})]$	—	192	—	175	—	149	—	111	MHz

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Standard 16-bit counter using GRP feedback.

Timing v.0.8

ispMACH 4000ZE Internal Timing Parameters

Over Recommended Operating Conditions

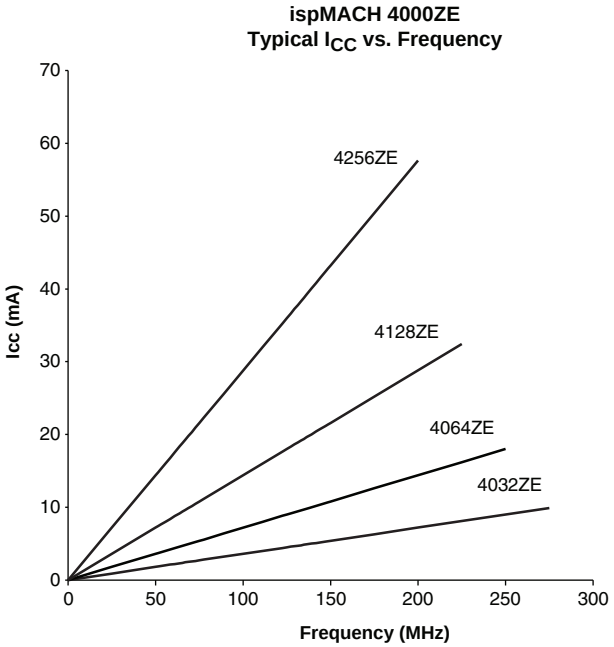
Parameter	Description	LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
In/Out Delays						
t_{IN}	Input Buffer Delay	—	0.85	—	0.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	ns
t_{GOE}	Global OE Pin Delay	—	2.25	—	2.25	ns
t_{BUF}	Delay through Output Buffer	—	0.75	—	0.90	ns
t_{EN}	Output Enable Time	—	2.25	—	2.25	ns
t_{DIS}	Output Disable Time	—	1.35	—	1.35	ns
t_{PGSU}	Input Power Guard Setup Time	—	3.30	—	3.55	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	5.00	—	5.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dissertation	—	5.00	—	5.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	1.60	—	1.70	ns
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.90	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.55	—	0.55	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_{S}	D-Register Setup Time (Global Clock)	0.70	—	0.85	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.25	—	1.85	—	ns
t_{H}	D-Register Hold Time	1.50	—	1.65	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	0.90	—	1.05	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.45	—	1.65	—	ns
t_{HT}	T-Resister Hold Time	1.50	—	1.65	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.85	—	0.80	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.15	—	1.30	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.90	—	1.10	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.35	—	0.40	ns
t_{CES}	Clock Enable Setup Time	1.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.70	—	0.95	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.45	—	1.85	—	ns
t_{HL}	Latch Hold Time	1.40	—	1.80	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.35	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.30	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.30	—	0.30	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	2.00	—	1.70	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.20	—	1.30	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.40	—	1.50	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.10	—	1.85	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.20	—	1.90	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.60	—	1.70	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.30	—	3.15	ns
t_{GPTOE}	Global PT OE Delay		—	1.80	—	2.15	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	12.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	7.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	6.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	5.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	4.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	3.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.00	—	1.00	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.40	—	0.40	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.04	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

Power Consumption



Power Estimation Coefficients[1]

Device	A	B
ispMACH 4032ZE	0.010	0.009
ispMACH 4064ZE	0.011	0.009
ispMACH 4128ZE	0.012	0.009
ispMACH 4256ZE	0.013	0.009

1. For further information about the use of these coefficients, refer to TN1187, Power Estimation in ispMACH 4000ZE Devices.

ispMACH 4000ZE Power Supply and NC Connections[1] (Cont.)

Signal	132 ucBGA[3]	144 csBGA[3]	144 TQFP[2]
VCC	M1, M7, A12, B5	H5, H8, E8, E5	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	B1, H4, L2, J5, A4	E4, F4, G4, J5, D5	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	K9, L12, F12, D9, C7	J8, H9, G9, F9, D8	64, 75, 91, 106, 119
GND	E5, E8, H5, H8	F6, G6, G7, F7	1, 37, 73, 109
GND (Bank 0)	E2, H2, M4, B7, B3	G5, H4, H6, E6, F5	10, 18[4], 27, 46, 127, 137
GND (Bank 1)	L7, J9, H12, E9, A9	H7, J9, G8, F8, E7	55, 65, 82, 90[4], 99, 118
NC	—	**4064ZE:** E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 **4128ZE:** D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2	**4128ZE:** 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 **4256ZE:** 18, 90

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
GND*	-	GND
A1	-	TDI
B1	0	VCCO (Bank 0)
D3	0	B0
C1	0	B1
D2	0	B2
D1	0	B4
E4	0	B5
F3	0	B6
E2	0	GND (Bank 0)
E1	0	B8
E3	0	B9
F4	0	B10
G4	0	B12
F2	0	B13
G3	0	B14
H4	0	VCCO (Bank 0)
F1	0	C14
G2	0	C13
G1	0	C12
H3	0	C10
J4	0	C9
H1	0	C8
H2	0	GND (Bank 0)
J3	0	C6
J1	0	C5
J2	0	C4
K3	0	C2
K2	0	C1
K1	0	C0
L2	0	VCCO (Bank 0)
L1	-	TCK
M1	-	VCC
GND*	-	GND
L3	0	D14
M2	0	D13
K4	0	D12
M3	0	D10
K5	0	D9
L4	0	D8
M4	0	GND (Bank 0)
J5	0	VCCO (Bank 0)
L5	0	D6

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J12	1	NC Ball	NC Ball	L14
J11	1	NC Ball	NC Ball	L12
H10	1	NC Ball	F8	L10
H12	1	C12	F9	L8
G11	1	C13	F10	L6
H11	1	C14	F12	L4
G12	1	C15	F13	L2
G10*	1	I	F14	L0
G9	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
F12	1	D15	G14	M0
F11	1	D14	G13	M2
E11	1	D13	G12	M4
E12	1	D12	G10	M6
D10	1	NC Ball	G9	M8
F10	1	NC Ball	G8	M10
D12	1	NC Ball	NC Ball	M12
F8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
E10	1	D11	G6	N2
D11	1	D10	G5	N4
E9	1	D9	G4	N6
C12	1	D8	G2	N8
C11*	1	I	G1	N10
B12	1	NC Ball	G0	N12
F9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
B11	-	TDO	TDO	TDO
E8	-	VCC	VCC	VCC
F7	-	GND	GND	GND
A12	1	NC Ball	NC Ball	O14
C10	1	NC Ball	NC Ball	O12
B10	1	NC Ball	H14	O10
A11*	1	I	H13	O8
D9	1	D7	H12	O6
B9	1	D6	H10	O4
C9	1	D5	H9	O2
A10	1	D4	H8	O0
E7	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
D8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
A9	1	NC Ball	H6	P12
B8	1	NC Ball	H5	P10
C8	1	D3	H4	P8
A8	1	D2	H2	P6
D7	1	D1	H1	P4
B7	1	D0/GOE1	H0/GOE1	P2/GOE1

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
C7	1	CLK3/I	CLK3/I	CLK3/I
E6	0	NC Ball	GND (Bank 0)	GND (Bank 0)
A7	0	CLK0/I	CLK0/I	CLK0/I
E5	-	VCC	VCC	VCC
D6	0	A0/GOE0	A0/GOE0	A2/GOE0
B6	0	A1	A1	A4
A6	0	A2	A2	A6
C6	0	A3	A4	A8
B5	0	NC Ball	A5	A10
A5	0	NC Ball	A6	A12
D5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
F5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
A4	0	A4	A8	B2
B4	0	A5	A9	B4
C5	0	A6	A10	B6
A3	0	A7	A12	B8
C4	0	NC Ball	A13	B10
B3	0	NC Ball	A14	B12
A2	0	NC Ball	NC Ball	B14

* This pin is input only for the LC4064ZE.

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.