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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5.8 ns |
| Voltage Supply - Internal | 1.7V ~ 1.9V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 48 |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TFBGA, CSPBGA |
| Supplier Device Package | 64-CSBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-5mn64i |

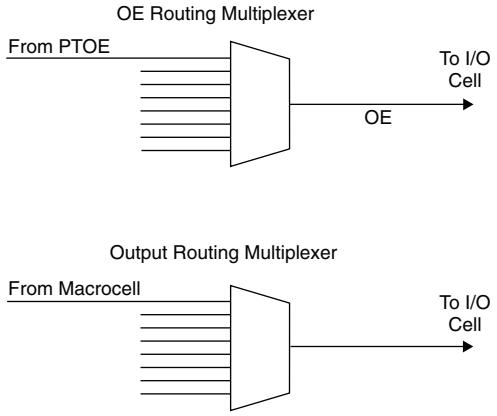
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. The enhanced ORP of the ispMACH 4000ZE family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

***Figure 7. ORP Slice***




## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-7 provide the connection details.

***Table 5. GLB/MC/ORP Combinations for ispMACH 4256ZE***

| GLB/MC | ORP Mux Input Macrocells |
|---|---|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 2] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 3] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 4] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 5] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 6] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 7] | M14, M15, M0, M1, M2, M3, M4, M5 |

*Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE*

| GLB/MC | ORP Mux Input Macrocells |
|---|---|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M1, M2, M3, M4, M5, M6, M7, M8 |
| [GLB] [MC 2] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 3] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 4] | M5, M6, M7, M8, M9, M10, M11, M12 |
| [GLB] [MC 5] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 6] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 7] | M9, M10, M11, M12, M13, M14, M15, M0 |
| [GLB] [MC 8] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 9] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 10] | M13, M14, M15, M0, M1, M2, M3, M4 |
| [GLB] [MC 11] | M14, M15, M0, M1, M2, M3, M4, M5 |

*Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE*

| GLB/MC | ORP Mux Input Macrocells |
|---|---|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M1, M2, M3, M4, M5, M6, M7, M8 |
| [GLB] [MC 2] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 3] | M3, M4, M5, M6, M7, M8, M9, M10 |
| [GLB] [MC 4] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 5] | M5, M6, M7, M8, M9, M10, M11, M12 |
| [GLB] [MC 6] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 7] | M7, M8, M9, M10, M11, M12, M13, M14 |
| [GLB] [MC 8] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 9] | M9, M10, M11, M12, M13, M14, M15, M0 |
| [GLB] [MC 10] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 11] | M11, M12, M13, M14, M15, M0, M1, M2 |
| [GLB] [MC 12] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 13] | M13, M14, M15, M0, M1, M2, M3, M4 |
| [GLB] [MC 14] | M14, M15, M0, M1, M2, M3, M4, M5 |
| [GLB] [MC 15] | M15, M0, M1, M2, M3, M4, M5, M6 |

### Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

## I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

*Figure 13. On-Chip Oscillator and Timer*


*Table 11. On-Chip Oscillator and Timer Signal Names*

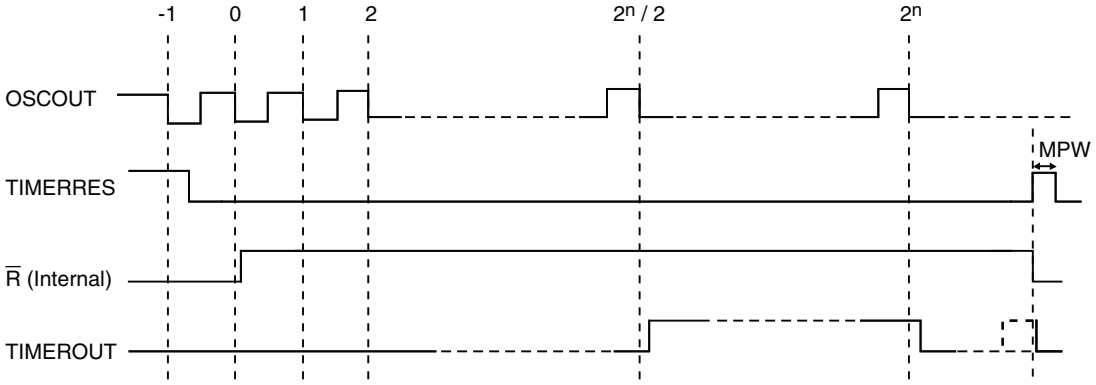
| Signal Name | Input or Output | Optional / Required | Description |
|---|---|---|---|
| OSCOUT | Output | Optional | Oscillator Output (Nominal Frequency: 5MHz) |
| TIMEROUT | Output | Optional | Oscillator Frequency Divided by an integer TIMER_DIV (Default 128) |
| TIMERRES | Input | Optional | Reset the Timer |
| DYNOSCDIS | Input | Optional | Disables the Oscillator, resets the Timer and saves the power. |

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER_DIV.

The attribute TIMER_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal "$\overline{R}$" is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

*Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT*



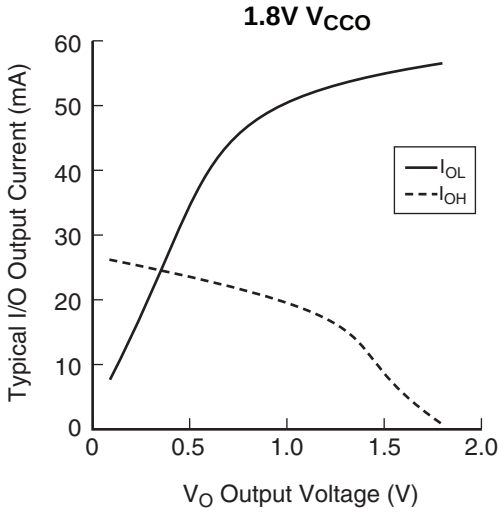

Note: n = Number of bits in the divider (7, 10 or 20)
Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

# I/O DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVTTL | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 3.3 | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.70 | 1.70 | 3.6 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.5[2] | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| PCI 3.3 | -0.3 | 0.3 * 3.3 * ($V_{CC}$ / 1.8) | 0.5 * 3.3 * ($V_{CC}$ / 1.8) | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from $V_{CC}$, if the ispMACH 4000ZE $V_{CC}$ and the $V_{CC}$ of the driving device ($V_{CC}$d-d; that determines steady state $V_{IH}$) are in the extreme range of their specifications. Typically, DC current drawn from $V_{CC}$ will be 2µA per input.



# ispMACH 4000ZE External Switching Characteristics

**Over Recommended Operating Conditions**

| Parameter | Description[1, 2] | LC4032ZE | | LC4064ZE | | All Devices | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -4 | | -4 | | -5 | | -7 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | 20-PT combinatorial propagation delay | — | 4.4 | — | 4.7 | — | 5.8 | — | 7.5 | ns |
| $t_S$ | GLB register setup time before clock | 2.2 | — | 2.5 | — | 2.9 | — | 4.5 | — | ns |
| $t_{ST}$ | GLB register setup time before clock with T-type register | 2.4 | — | 2.7 | — | 3.1 | — | 4.7 | — | ns |
| $t_{SIR}$ | GLB register setup time before clock, input register path | 1.0 | — | 1.1 | — | 1.3 | — | 1.4 | — | ns |
| $t_{SIRZ}$ | GLB register setup time before clock with zero hold | 2.0 | — | 2.1 | — | 2.9 | — | 4.0 | — | ns |
| $t_H$ | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HT}$ | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{HIR}$ | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.3 | — | 1.3 | — | ns |
| $t_{HIRZ}$ | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| $t_{CO}$ | GLB register clock-to-output delay | — | 3.0 | — | 3.2 | — | 3.8 | — | 4.5 | ns |
| $t_R$ | External reset pin to output delay | — | 5.0 | — | 6.0 | — | 7.5 | — | 9.0 | ns |
| $t_{RW}$ | External reset pulse duration | 1.5 | — | 1.7 | — | 2.0 | — | 4.0 | — | ns |
| $t_{PTOE/DIS}$ | Input to output local product term output enable/disable | — | 7.0 | — | 8.0 | — | 8.2 | — | 9.0 | ns |
| $t_{GPTOE/DIS}$ | Input to output global product term output enable/disable | — | 6.5 | — | 7.0 | — | 10.0 | — | 10.5 | ns |
| $t_{GOE/DIS}$ | Global OE input to output enable/disable | — | 4.5 | — | 4.5 | — | 5.5 | — | 7.0 | ns |
| $t_{CW}$ | Global clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | 2.8 | — | ns |
| $t_{GW}$ | Global gate width low (for low transparent) or high (for high transparent) | 1.0 | — | 1.5 | — | 1.8 | — | 2.8 | — | ns |
| $t_{WIR}$ | Input register clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | 2.8 | — | ns |
| $f_{MAX}$ (Int.)[3] | Clock frequency with internal feedback | — | 260 | — | 241 | — | 200 | — | 172 | MHz |
| $f_{MAX}$ (Ext.) | clock frequency with external feedback, $[1 / (t_S + t_{CO})]$ | — | 192 | — | 175 | — | 149 | — | 111 | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.
2. Measured using standard switching GRP loading of 1 and 1 output switching.
3. Standard 16-bit counter using GRP feedback.

Timing v.0.8

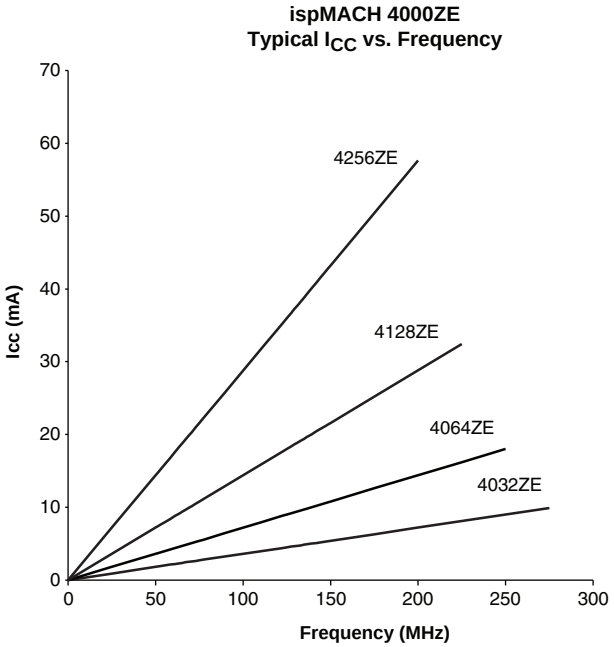
# ispMACH 4000ZE Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | | LC4032ZE -4 Min. | LC4032ZE -4 Max. | LC4064ZE -4 Min. | LC4064ZE -4 Max. | Units |
|---|---|---|---|---|---|---|---|
| LVCMOS15_out | Output Configured as 1.5V Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.20 | — | 0.20 | ns |
| LVCMOS18_out | Output Configured as 1.8V Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.00 | — | 0.00 | ns |
| LVCMOS25_out | Output Configured as 2.5V Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.10 | — | 0.10 | ns |
| LVCMOS33_out | Output Configured as 3.3V Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.20 | — | 0.20 | ns |
| PCI_out | Output Configured as PCI Compatible Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.20 | — | 0.20 | ns |
| Slow Slew | Output Configured for Slow Slew Rate | $t_{EN}$, $t_{BUF}$ | — | 1.00 | — | 1.00 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

## Power Consumption




## Power Estimation Coefficients[1]

| Device | A | B |
|---|---|---|
| ispMACH 4032ZE | 0.010 | 0.009 |
| ispMACH 4064ZE | 0.011 | 0.009 |
| ispMACH 4128ZE | 0.012 | 0.009 |
| ispMACH 4256ZE | 0.013 | 0.009 |

1. For further information about the use of these coefficients, refer to TN1187, Power Estimation in ispMACH 4000ZE Devices.

## Signal Descriptions

| Signal Names | Description | |
|---|---|---|
| TMS | Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine. | |
| TCK | Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine. | |
| TDI | Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data. | |
| TDO | Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out. | |
| GOE0/IO, GOE1/IO | These pins are configured to be either Global Output Enable Input or as general I/O pins. | |
| GND | Ground | |
| NC | Not Connected | |
| $V_{CC}$ | The power supply pins for logic core and JTAG port. | |
| CLK0/I, CLK1/I, CLK2/I, CLK3/I | These pins are configured to be either CLK input or as an input. | |
| $V_{CCO0}$, $V_{CCO1}$ | The power supply pins for each I/O bank. | |
| yzz | Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15. | |
| | ispMACH 4032ZE | y: A-B |
| | ispMACH 4064ZE | y: A-D |
| | ispMACH 4128ZE | y: A-H |
| | ispMACH 4256ZE | y: A-P |

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

## ORP Reference Table

| | 4032ZE | 4064ZE | | | 4128ZE | | 4256ZE | | |
|---|---|---|---|---|---|---|---|---|---|
| Number of I/Os | 32 | 32 | 48 | 64 | 64 | 96 | 64 | 96 | 108 |
| Number of GLBs | 2 | 4 | 4 | 4 | 8 | 8 | 16 | 16 | 16 |
| Number of I/Os per GLB | 16 | 8 | Mixture of 9, 10, 14, 15 | 16 | 8 | 12 | 4 | 6 | Mixture of 6, 7, 8 |
| Reference ORP Table (I/Os per GLB) | 16 | 8 | 9, 10, 14, 15 | 16 | 8 | 12 | 4 | 6 | 6, 7, 8 |

## ispMACH 4000ZE Power Supply and NC Connections[1]

| Signal | 48 TQFP[2] | 64 csBGA[3, 4] | 64 ucBGA[3, 4] | 100 TQFP[2] |
|---|---|---|---|---|
| VCC | 12, 36 | E4, D5 | E4, D5 | 25, 40, 75, 90 |
| VCCO0<br>VCCO (Bank 0) | 6 | **4032ZE:** E3<br>**4064ZE:** E3, F4 | C3, F3 | 13, 33, 95 |
| VCCO1<br>VCCO (Bank 1) | 30 | **4032ZE:** D6<br>**4064ZE:** D6, C6 | F6, A6 | 45, 63, 83 |
| GND | 13, 37 | D4, E5 | D4, D5 | 1, 26, 51, 76 |
| GND (Bank 0) | 5 | D4, E5 | D4, D5 | 7, 18, 32, 96 |
| GND (Bank 1) | 29 | D4, E5 | D4, D5 | 46, 57, 68, 82 |
| NC | — | — | — | — |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

## ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

| Pin Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | TDI | TDI |
| 2 | 0 | A5 | A8 |
| 3 | 0 | A6 | A10 |
| 4 | 0 | A7 | A11 |
| 5 | 0 | GND (Bank 0) | GND (Bank 0) |
| 6 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 7 | 0 | A8 | B15 |
| 8 | 0 | A9 | B12 |
| 9 | 0 | A10 | B10 |
| 10 | 0 | A11 | B8 |
| 11 | - | TCK | TCK |
| 12 | - | VCC | VCC |
| 13 | - | GND | GND |
| 14 | 0 | A12 | B6 |
| 15 | 0 | A13 | B4 |
| 16 | 0 | A14 | B2 |
| 17 | 0 | A15 | B0 |
| 18 | 0 | CLK1/I | CLK1/I |
| 19 | 1 | CLK2/I | CLK2/I |
| 20 | 1 | B0 | C0 |
| 21 | 1 | B1 | C1 |
| 22 | 1 | B2 | C2 |
| 23 | 1 | B3 | C4 |
| 24 | 1 | B4 | C6 |
| 25 | - | TMS | TMS |
| 26 | 1 | B5 | C8 |
| 27 | 1 | B6 | C10 |
| 28 | 1 | B7 | C11 |
| 29 | 1 | GND (Bank 1) | GND (Bank 1) |
| 30 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 31 | 1 | B8 | D15 |
| 32 | 1 | B9 | D12 |
| 33 | 1 | B10 | D10 |
| 34 | 1 | B11 | D8 |
| 35 | - | TDO | TDO |
| 36 | - | VCC | VCC |
| 37 | - | GND | GND |
| 38 | 1 | B12 | D6 |
| 39 | 1 | B13 | D4 |
| 40 | 1 | B14 | D2 |
| 41 | 1 | B15/GOE1 | D0/GOE1 |
| 42 | 1 | CLK3/I | CLK3/I |

## ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA

| Ball Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| B2 | - | TDI | TDI |
| B1 | 0 | A5 | A8 |
| C2 | 0 | A6 | A10 |
| C1 | 0 | A7 | A11 |
| GND* | 0 | GND (Bank 0) | GND (Bank 0) |
| C3 | 0 | NC | A12 |
| E3 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| D1 | 0 | A8 | B15 |
| D2 | 0 | NC | B14 |
| E1 | 0 | A9 | B13 |
| D3 | 0 | A10 | B12 |
| F1 | 0 | A11 | B11 |
| E2 | 0 | NC | B10 |
| G1 | 0 | NC | B9 |
| F2 | 0 | NC | B8 |
| H1 | - | TCK | TCK |
| E4 | - | VCC | VCC |
| GND* | - | GND | GND |
| G2 | 0 | A12 | B6 |
| H2 | 0 | NC | B5 |
| H3 | 0 | A13 | B4 |
| GND* | 0 | NC | GND (Bank 0) |
| F4 | 0 | NC | VCCO (Bank 0) |
| G3 | 0 | A14 | B3 |
| F3 | 0 | NC | B2 |
| H4 | 0 | A15 | B0 |
| G4 | 0 | CLK1/I | CLK1/I |
| H5 | 1 | CLK2/I | CLK2/I |
| F5 | 1 | B0 | C0 |
| G5 | 1 | B1 | C1 |
| G6 | 1 | B2 | C2 |
| H6 | 1 | B3 | C4 |
| F6 | 1 | B4 | C5 |
| H7 | 1 | NC | C6 |
| H8 | - | TMS | TMS |
| G7 | 1 | B5 | C8 |
| F7 | 1 | B6 | C10 |
| G8 | 1 | B7 | C11 |
| GND* | 1 | GND (Bank 0) | GND (Bank 1) |
| F8 | 1 | NC | C12 |
| D6 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| E8 | 1 | B8 | D15 |

## ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| E7 | 1 | D13 |
| E6 | 1 | D12 |
| D8 | 1 | D11 |
| D7 | 1 | D10 |
| D6 | 1 | D9 |
| C8 | 1 | D8 |
| C7 | - | TDO |
| D5 | - | VCC |
| GND* | - | GND |
| B8 | 1 | D7 |
| A8 | 1 | D6 |
| B7 | 1 | D5 |
| A7 | 1 | D4 |
| GND* | 1 | GND (Bank 1) |
| A6 | 1 | VCCO (Bank 1) |
| B6 | 1 | D3 |
| C6 | 1 | D2 |
| A5 | 1 | D0/GOE1 |
| B5 | 1 | CLK3/I |
| C5 | 0 | CLK0/I |
| A4 | 0 | A0/GOE0 |
| B4 | 0 | A1 |
| C4 | 0 | A2 |
| A3 | 0 | A4 |
| A2 | 0 | A6 |

* All bonded grounds are connected to the following two balls, D4 and E5.

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | GND | GND | GND |
| 2 | - | TDI | TDI | TDI |
| 3 | 0 | A8 | B0 | C12 |
| 4 | 0 | A9 | B2 | C10 |
| 5 | 0 | A10 | B4 | C6 |
| 6 | 0 | A11 | B6 | C2 |
| 7 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 8 | 0 | A12 | B8 | D12 |
| 9 | 0 | A13 | B10 | D10 |
| 10 | 0 | A14 | B12 | D6 |
| 11 | 0 | A15 | B13 | D4 |
| 12* | 0 | I | I | I |
| 13 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 14 | 0 | B15 | C14 | E4 |
| 15 | 0 | B14 | C12 | E6 |
| 16 | 0 | B13 | C10 | E10 |
| 17 | 0 | B12 | C8 | E12 |
| 18 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 19 | 0 | B11 | C6 | F2 |
| 20 | 0 | B10 | C5 | F6 |
| 21 | 0 | B9 | C4 | F10 |
| 22 | 0 | B8 | C2 | F12 |
| 23* | 0 | I | I | I |
| 24 | - | TCK | TCK | TCK |
| 25 | - | VCC | VCC | VCC |
| 26 | - | GND | GND | GND |
| 27* | 0 | I | I | I |
| 28 | 0 | B7 | D13 | G12 |
| 29 | 0 | B6 | D12 | G10 |
| 30 | 0 | B5 | D10 | G6 |
| 31 | 0 | B4 | D8 | G2 |
| 32 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 33 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 34 | 0 | B3 | D6 | H12 |
| 35 | 0 | B2 | D4 | H10 |
| 36 | 0 | B1 | D2 | H6 |
| 37 | 0 | B0 | D0 | H2 |
| 38 | 0 | CLK1/I | CLK1/I | CLK1/I |
| 39 | 1 | CLK2/I | CLK2/I | CLK2/I |
| 40 | - | VCC | VCC | VCC |
| 41 | 1 | C0 | E0 | I2 |

## ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| A2 | 0 | A14 |

* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| J12 | 1 | NC Ball | NC Ball | L14 |
| J11 | 1 | NC Ball | NC Ball | L12 |
| H10 | 1 | NC Ball | F8 | L10 |
| H12 | 1 | C12 | F9 | L8 |
| G11 | 1 | C13 | F10 | L6 |
| H11 | 1 | C14 | F12 | L4 |
| G12 | 1 | C15 | F13 | L2 |
| G10* | 1 | I | F14 | L0 |
| G9 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| F12 | 1 | D15 | G14 | M0 |
| F11 | 1 | D14 | G13 | M2 |
| E11 | 1 | D13 | G12 | M4 |
| E12 | 1 | D12 | G10 | M6 |
| D10 | 1 | NC Ball | G9 | M8 |
| F10 | 1 | NC Ball | G8 | M10 |
| D12 | 1 | NC Ball | NC Ball | M12 |
| F8 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| E10 | 1 | D11 | G6 | N2 |
| D11 | 1 | D10 | G5 | N4 |
| E9 | 1 | D9 | G4 | N6 |
| C12 | 1 | D8 | G2 | N8 |
| C11* | 1 | I | G1 | N10 |
| B12 | 1 | NC Ball | G0 | N12 |
| F9 | 1 | NC Ball | VCCO (Bank 1) | VCCO (Bank 1) |
| B11 | - | TDO | TDO | TDO |
| E8 | - | VCC | VCC | VCC |
| F7 | - | GND | GND | GND |
| A12 | 1 | NC Ball | NC Ball | O14 |
| C10 | 1 | NC Ball | NC Ball | O12 |
| B10 | 1 | NC Ball | H14 | O10 |
| A11* | 1 | I | H13 | O8 |
| D9 | 1 | D7 | H12 | O6 |
| B9 | 1 | D6 | H10 | O4 |
| C9 | 1 | D5 | H9 | O2 |
| A10 | 1 | D4 | H8 | O0 |
| E7 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| D8 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| A9 | 1 | NC Ball | H6 | P12 |
| B8 | 1 | NC Ball | H5 | P10 |
| C8 | 1 | D3 | H4 | P8 |
| A8 | 1 | D2 | H2 | P6 |
| D7 | 1 | D1 | H1 | P4 |
| B7 | 1 | D0/GOE1 | H0/GOE1 | P2/GOE1 |

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| C7 | 1 | CLK3/I | CLK3/I | CLK3/I |
| E6 | 0 | NC Ball | GND (Bank 0) | GND (Bank 0) |
| A7 | 0 | CLK0/I | CLK0/I | CLK0/I |
| E5 | - | VCC | VCC | VCC |
| D6 | 0 | A0/GOE0 | A0/GOE0 | A2/GOE0 |
| B6 | 0 | A1 | A1 | A4 |
| A6 | 0 | A2 | A2 | A6 |
| C6 | 0 | A3 | A4 | A8 |
| B5 | 0 | NC Ball | A5 | A10 |
| A5 | 0 | NC Ball | A6 | A12 |
| D5 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| F5 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| A4 | 0 | A4 | A8 | B2 |
| B4 | 0 | A5 | A9 | B4 |
| C5 | 0 | A6 | A10 | B6 |
| A3 | 0 | A7 | A12 | B8 |
| C4 | 0 | NC Ball | A13 | B10 |
| B3 | 0 | NC Ball | A14 | B12 |
| A2 | 0 | NC Ball | NC Ball | B14 |

* This pin is input only for the LC4064ZE.

## ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | GND | GND |
| 2 | - | TDI | TDI |
| 3 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 4 | 0 | B0 | C12 |
| 5 | 0 | B1 | C10 |
| 6 | 0 | B2 | C8 |
| 7 | 0 | B4 | C6 |
| 8 | 0 | B5 | C4 |
| 9 | 0 | B6 | C2 |
| 10 | 0 | GND (Bank 0) | GND (Bank 0) |
| 11 | 0 | B8 | D14 |
| 12 | 0 | B9 | D12 |
| 13 | 0 | B10 | D10 |
| 14 | 0 | B12 | D8 |
| 15 | 0 | B13 | D6 |
| 16 | 0 | B14 | D4 |
| 17* | 0 | NC | I |
| 18 | 0 | GND (Bank 0) | NC |
| 19 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 20* | 0 | NC | I |
| 21 | 0 | C14 | E2 |
| 22 | 0 | C13 | E4 |
| 23 | 0 | C12 | E6 |
| 24 | 0 | C10 | E8 |
| 25 | 0 | C9 | E10 |
| 26 | 0 | C8 | E12 |
| 27 | 0 | GND (Bank 0) | GND (Bank 0) |
| 28 | 0 | C6 | F2 |
| 29 | 0 | C5 | F4 |
| 30 | 0 | C4 | F6 |
| 31 | 0 | C2 | F8 |
| 32 | 0 | C1 | F10 |
| 33 | 0 | C0 | F12 |
| 34 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 35 | - | TCK | TCK |
| 36 | - | VCC | VCC |
| 37 | - | GND | GND |
| 38* | 0 | NC | I |
| 39 | 0 | D14 | G12 |
| 40 | 0 | D13 | G10 |
| 41 | 0 | D12 | G8 |
| 42 | 0 | D10 | G6 |

## ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 43 | 0 | D9 | G4 |
| 44 | 0 | D8 | G2 |
| 45* | 0 | NC | I |
| 46 | 0 | GND (Bank 0) | GND (Bank 0) |
| 47 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 48 | 0 | D6 | H12 |
| 49 | 0 | D5 | H10 |
| 50 | 0 | D4 | H8 |
| 51 | 0 | D2 | H6 |
| 52 | 0 | D1 | H4 |
| 53 | 0 | D0 | H2 |
| 54 | 0 | CLK1/I | CLK1/I |
| 55 | 1 | GND (Bank 1) | GND (Bank 1) |
| 56 | 1 | CLK2/I | CLK2/I |
| 57 | - | VCC | VCC |
| 58 | 1 | E0 | I2 |
| 59 | 1 | E1 | I4 |
| 60 | 1 | E2 | I6 |
| 61 | 1 | E4 | I8 |
| 62 | 1 | E5 | I10 |
| 63 | 1 | E6 | I12 |
| 64 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 65 | 1 | GND (Bank 1) | GND (Bank 1) |
| 66 | 1 | E8 | J2 |
| 67 | 1 | E9 | J4 |
| 68 | 1 | E10 | J6 |
| 69 | 1 | E12 | J8 |
| 70 | 1 | E13 | J10 |
| 71 | 1 | E14 | J12 |
| 72* | 1 | NC | I |
| 73 | - | GND | GND |
| 74 | - | TMS | TMS |
| 75 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 76 | 1 | F0 | K12 |
| 77 | 1 | F1 | K10 |
| 78 | 1 | F2 | K8 |
| 79 | 1 | F4 | K6 |
| 80 | 1 | F5 | K4 |
| 81 | 1 | F6 | K2 |
| 82 | 1 | GND (Bank 1) | GND (Bank 1) |
| 83 | 1 | F8 | L14 |
| 84 | 1 | F9 | L12 |
| 85 | 1 | F10 | L10 |

**Industrial**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZE | LC4032ZE-5TN48I | 32 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-7TN48I | 32 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-5MN64I | 32 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 32 | I |
| | LC4032ZE-7MN64I | 32 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 32 | I |
| LC4064ZE | LC4064ZE-5TN48I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-7TN48I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-5TN100I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-7TN100I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-5MN64I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-7MN64I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-5UMN64I | 64 | 1.8 | 5.8 | Lead-Free ucBGA | 64 | 48 | I |
| | LC4064ZE-7UMN64I | 64 | 1.8 | 7.5 | Lead-Free ucBGA | 64 | 48 | I |
| | LC4064ZE-5MN144I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 64 | I |
| | LC4064ZE-7MN144I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 64 | I |
| LC4128ZE | LC4128ZE-7TN100I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4128ZE-7UMN132I | 128 | 1.8 | 7.5 | Lead-Free ucBGA | 132 | 96 | I |
| | LC4128ZE-7TN144I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4128ZE-7MN144I | 128 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 96 | I |
| LC4256ZE | LC4256ZE-7TN100I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4256ZE-7TN144I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4256ZE-7MN144I | 256 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 108 | I |

1. Contact factory for product availability.

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

## Technical Support Assistance

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## Revision History

| Date | Version | Change Summary |
|---|---|---|
| April 2008 | 01.0 | Initial release. |
| July 2008 | 01.1 | Updated Features bullets. |
| | | Updated typical Hysteresis voltage. |
| | | Updated Power Guard for Dedicated Inputs section. |
| | | Updated DC Electrical Characteristics table. |
| | | Updated Supply Current table. |
| | | Updated I/O DC Electrical Characteristics table and note 2. |
| | | Updated ispMACH 4000ZE Timing Model. |
| | | Added new parameters for the Internal Oscillator. |
| | | Updated ORP Reference table. |
| | | Updated Power Supply and NC Connections table. |
| | | Updated 100 TQFP Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Updated 144 csBGA Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Added 144 TQFP Logic Signal Connections table. |
| August 2008 | 01.2 | Data sheet status changed from advance to final. |
| | | Updated Supply Current table. |
| | | Updated External Switching Characteristics. |
| | | Updated Internal Timing Parameters. |
| | | Updated Power Consumption graph and Power Estimation Coefficients table. |
| | | Updated Ordering Information mark format example. |
| December 2008 | 01.3 | Updated ispMACH 4000ZE Family Selection Guide table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated ispMACH 4000ZE Power Supply and NC Connections table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Added Logic Signal Connections tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Part Number Description diagram for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Ordering Information tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| May 2009 | 01.4 | Correction to $t_{CW}$, $t_{GW}$, $t_{WIR}$ and $f_{MAX}$ parameters in External Switching Characteristics table. |
| June 2011 | 01.5 | Added copper bond package part numbers. |
| | | Added footnote 4 to Absolute Maximum Ratings. |
| February 2012 | 01.6 | Updated document with new corporate logo. |
| February 2012 | 01.7 | Removed copper bond packaging information. Refer to PCN 04A-12 for further information. |
| | | Updated topside marks with new logos in the Ordering Information section. |