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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-5tn100i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-5tn100i</a>

The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a  $V_{CCO}$  of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

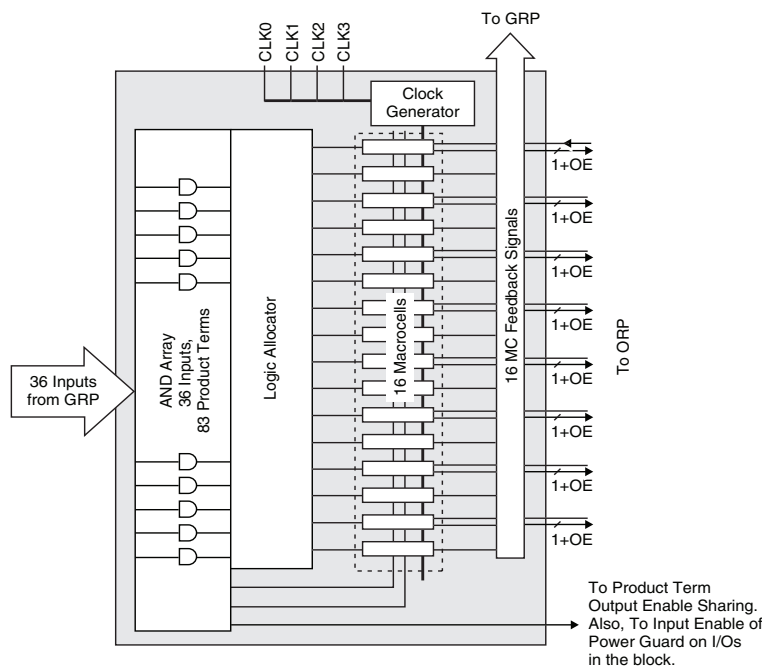
## Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

### Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

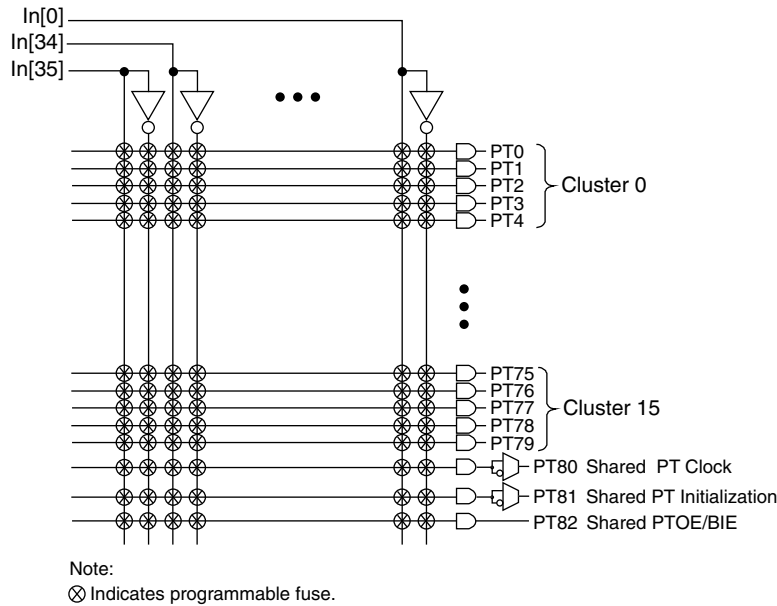


### AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array



### Enhanced Logic Allocator

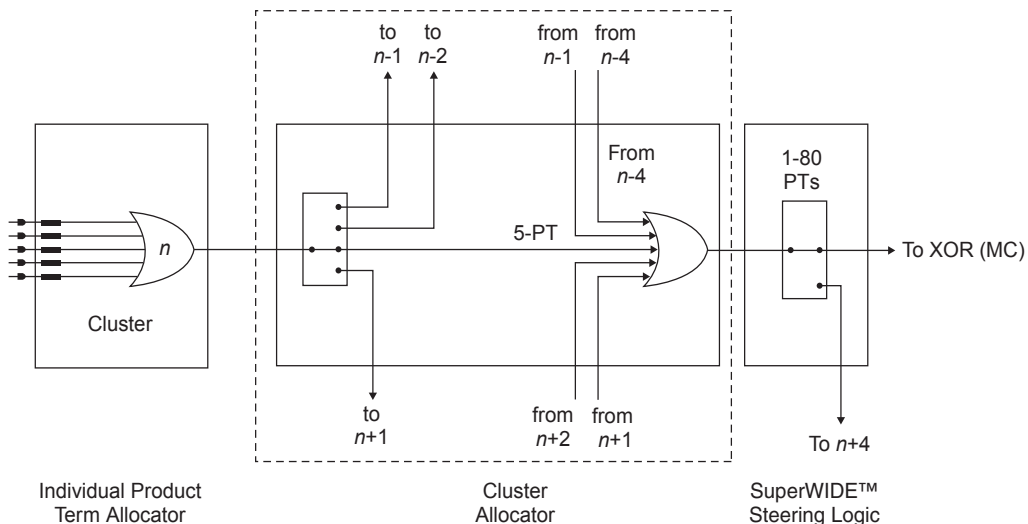
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



**Table 4. Product Term Expansion Capability**

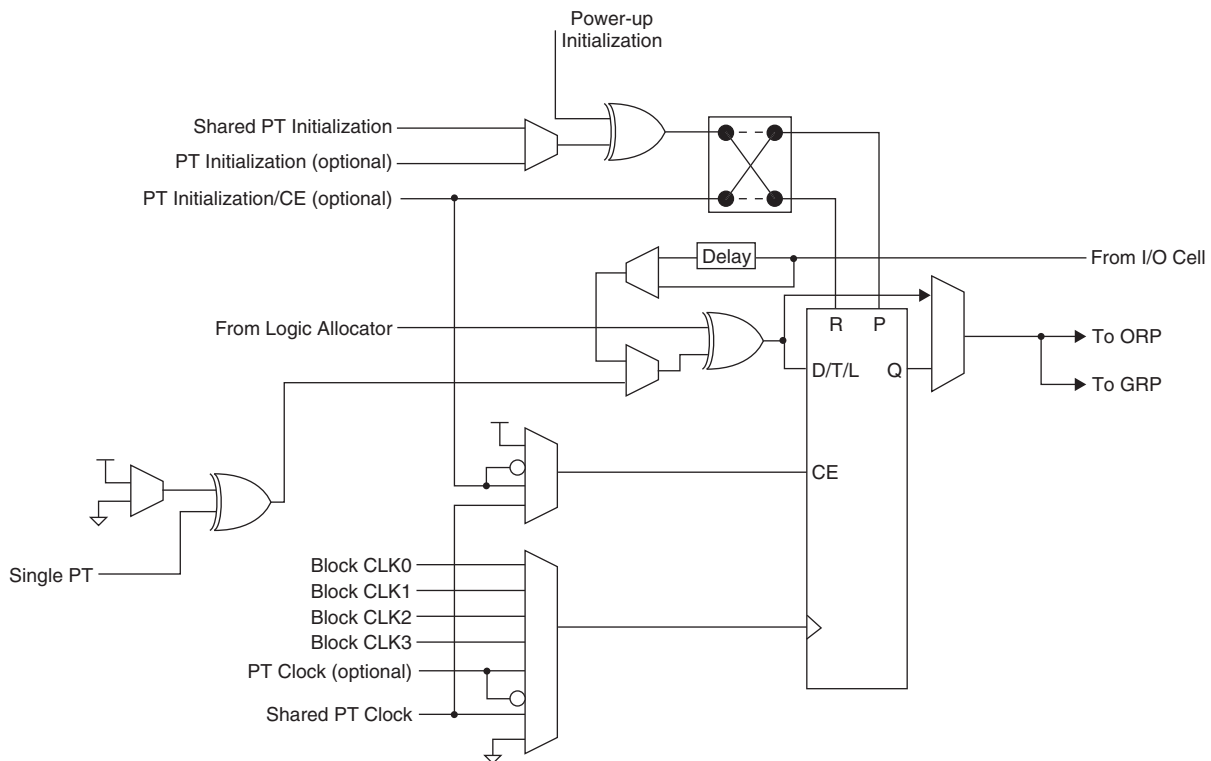
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/Macrocell
Chain-0	M0 Õ M4 Õ M8 Õ M12 Õ M0	75
Chain-1	M1 Õ M5 Õ M9 Õ M13 Õ M1	80
Chain-2	M2 Õ M6 Õ M10 Õ M14 Õ M2	75
Chain-3	M3 Õ M7 Õ M11 Õ M15 Õ M3	70

Every time the super cluster allocator is used, there is an incremental delay of  $t_{EXP}$ . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

### Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

**Figure 5. Macrocell**



### Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

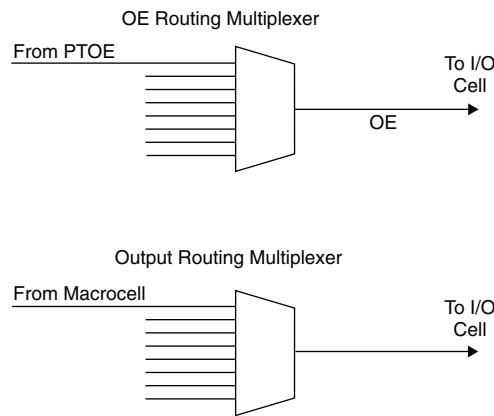
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. The enhanced ORP of the ispMACH 400ZE family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

**Figure 7. ORP Slice**



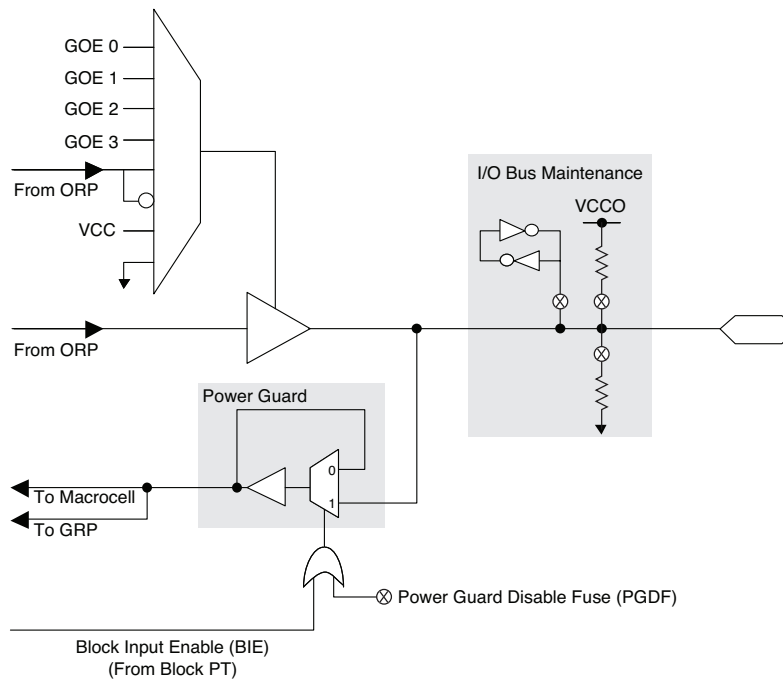
## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-7 provide the connection details.

**Table 5. GLB/MC/ORP Combinations for ispMACH 4256ZE**

GLB/MC	ORP Mux Input Macrocells
[GLB] [MC 0]	M0, M1, M2, M3, M4, M5, M6, M7
[GLB] [MC 1]	M2, M3, M4, M5, M6, M7, M8, M9
[GLB] [MC 2]	M4, M5, M6, M7, M8, M9, M10, M11
[GLB] [MC 3]	M6, M7, M8, M9, M10, M11, M12, M13
[GLB] [MC 4]	M8, M9, M10, M11, M12, M13, M14, M15
[GLB] [MC 5]	M10, M11, M12, M13, M14, M15, M0, M1
[GLB] [MC 6]	M12, M13, M14, M15, M0, M1, M2, M3
[GLB] [MC 7]	M14, M15, M0, M1, M2, M3, M4, M5

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the  $V_{CCO}$  supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the  $V_{CCO}$  supplied to its I/O bank. The I/O standards supported are:

- LVTTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a “per-pin” basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

## Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

**Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices**

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, ..., H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, ..., P)

### Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

**Table 9. Dedicated Clock Inputs to BIE Association**

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

**Table 10. Dedicated Inputs to BIE Association**

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, [Advanced Features of the ispMACH 4000ZE Family](#).

### Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

**Figure 13. On-Chip Oscillator and Timer**

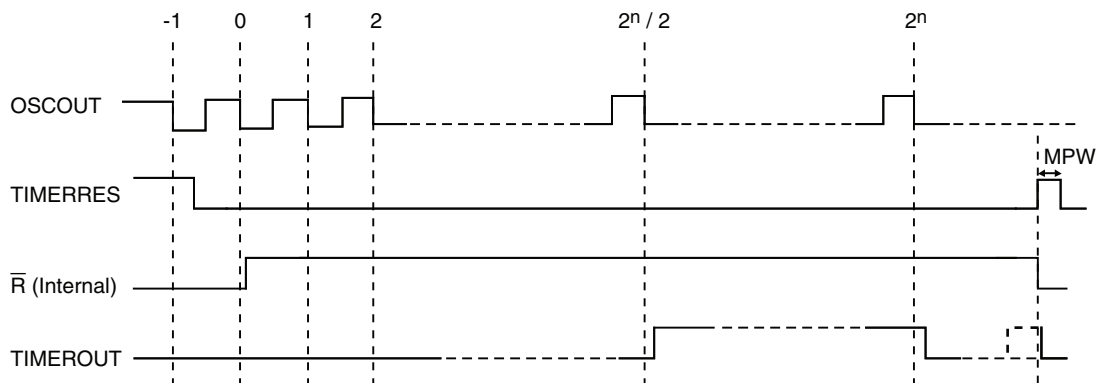
**Table 11. On-Chip Oscillator and Timer Signal Names**

Signal Name	Input or Output	Optional / Required	Description
OSCOUT	Output	Optional	Oscillator Output (Nominal Frequency: 5MHz)
TIMEROUT	Output	Optional	Oscillator Frequency Divided by an integer TIMER_DIV (Default 128)
TIMERRES	Input	Optional	Reset the Timer
DYNOSCDIS	Input	Optional	Disables the Oscillator, resets the Timer and saves the power.

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER\_DIV.

The attribute TIMER\_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal “ $\bar{R}$ ” is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

**Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT**


Note:  $n$  = Number of bits in the divider (7, 10 or 20)

Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.



## I/O Recommended Operating Conditions

Standard	V <sub>CCO</sub> (V) <sup>1</sup>	
	Min.	Max.
LVTTTL	3.0	3.6
LVC MOS 3.3	3.0	3.6
Extended LVC MOS 3.3	2.7	3.6
LVC MOS 2.5	2.3	2.7
LVC MOS 1.8	1.65	1.95
LVC MOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V<sub>CCO</sub> are the average of the min. and max. values.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>IL</sub> , I <sub>IH</sub> <sup>1,2</sup>	Input Leakage Current	0 ≤ V <sub>IN</sub> < V <sub>CCO</sub>	—	0.5	1	μA
I <sub>IH</sub> <sup>1</sup>	Input High Leakage Current	V <sub>CCO</sub> < V <sub>IN</sub> ≤ 5.5V	—	—	10	μA
I <sub>PU</sub>	I/O Weak Pull-up Resistor Current	0 ≤ V <sub>IN</sub> ≤ 0.7V <sub>CCO</sub>	-20	—	-150	μA
I <sub>PD</sub>	I/O Weak Pull-down Resistor Current	V <sub>IL</sub> (MAX) ≤ V <sub>IN</sub> ≤ V <sub>IH</sub> (MAX)	30	—	150	μA
I <sub>BHLS</sub>	Bus Hold Low Sustaining Current	V <sub>IN</sub> = V <sub>IL</sub> (MAX)	30	—	—	μA
I <sub>BHHS</sub>	Bus Hold High Sustaining Current	V <sub>IN</sub> = 0.7 V <sub>CCO</sub>	-20	—	—	μA
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	0V ≤ V <sub>IN</sub> ≤ V <sub>BHT</sub>	—	—	150	μA
I <sub>BHHO</sub>	Bus Hold High Overdrive Current	V <sub>BHT</sub> ≤ V <sub>IN</sub> ≤ V <sub>CCO</sub>	—	—	-150	μA
V <sub>BHT</sub>	Bus Hold Trip Points	—	V <sub>CCO</sub> * 0.35	—	V <sub>CCO</sub> * 0.65	V
C <sub>1</sub>	I/O Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	
C <sub>2</sub>	Clock Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	
C <sub>3</sub>	Global Input Capacitance <sup>3</sup>	V <sub>CCO</sub> = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V <sub>CC</sub> = 1.8V, V <sub>IO</sub> = 0 to V <sub>IH</sub> (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I<sub>IH</sub> excursions of up to 1.5μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T<sub>A</sub> = 25°C, f = 1.0MHz.

**ispMACH 400ZE Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE		LC4064ZE		Units
			-4		-4		
			Min.	Max.	Min.	Max.	
LVC MOS15_out	Output Configured as 1.5V Buffer	$t_{EN}$ , $t_{DIS}$ , $t_{BUF}$	—	0.20	—	0.20	ns
LVC MOS18_out	Output Configured as 1.8V Buffer	$t_{EN}$ , $t_{DIS}$ , $t_{BUF}$	—	0.00	—	0.00	ns
LVC MOS25_out	Output Configured as 2.5V Buffer	$t_{EN}$ , $t_{DIS}$ , $t_{BUF}$	—	0.10	—	0.10	ns
LVC MOS33_out	Output Configured as 3.3V Buffer	$t_{EN}$ , $t_{DIS}$ , $t_{BUF}$	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	$t_{EN}$ , $t_{DIS}$ , $t_{BUF}$	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	$t_{EN}$ , $t_{BUF}$	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.  
 Timing v.0.8

**ispMACH 400ZE Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	All Devices				Units	
		-5		-7			
		Min.	Max.	Min.	Max.		
t <sub>SRR</sub>	Asynchronous Reset or Set Recovery Delay	—	1.80	—	1.67	ns	
<b>Control Delays</b>							
t <sub>BCLK</sub>	GLB PT Clock Delay	—	1.45	—	0.95	ns	
t <sub>PTCLK</sub>	Macrocell PT Clock Delay	—	1.45	—	1.15	ns	
t <sub>BSR</sub>	Block PT Set/Reset Delay	—	1.85	—	1.83	ns	
t <sub>PTSR</sub>	Macrocell PT Set/Reset Delay	—	1.85	—	2.72	ns	
t <sub>BIE</sub>	Power Guard Block Input Enable Delay	—	1.75	—	1.95	ns	
t <sub>P<sub>TOE</sub></sub>	Macrocell PT OE Delay	—	2.40	—	1.90	ns	
t <sub>GPTOE</sub>	Global PT OE Delay	—	4.20	—	3.40	ns	
<b>Internal Oscillator</b>							
t <sub>OSCSU</sub>	Oscillator DYNOSCDIS Setup Time	5.00	—	5.00	—	ns	
t <sub>OSCH</sub>	Oscillator DYNOSCDIS Hold Time	5.00	—	5.00	—	ns	
t <sub>OSCEN</sub>	Oscillator OSCOUT Enable Time (To Stable)	—	5.00	—	5.00	ns	
t <sub>OSCOD</sub>	Oscillator Output Delay	—	4.00	—	4.00	ns	
t <sub>OSCNOM</sub>	Oscillator OSCOUT Nominal Frequency	—	5.00	—	5.00	MHz	
t <sub>OSCvar</sub>	Oscillator Variation of Nominal Frequency	—	30	—	30	%	
t <sub>TMRCO20</sub>	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)	—	12.50	—	14.50	ns	
t <sub>TMRCO10</sub>	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)	—	7.50	—	9.50	ns	
t <sub>TMRCO7</sub>	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)	—	6.00	—	8.00	ns	
t <sub>TMRRSTO</sub>	Oscillator TIMEROUT Reset to Out (Going Low)	—	5.00	—	7.00	ns	
t <sub>TMRRR</sub>	Oscillator TIMEROUT Asynchronous Reset Recovery Delay	—	4.00	—	6.00	ns	
t <sub>TMRRSTPW</sub>	Oscillator TIMEROUT Reset Minimum Pulse Width	3.00	—	5.00	—	ns	
<b>Optional Delay Adjusters</b>		<b>Base Parameter</b>					
t <sub>INDIO</sub>	Input Register Delay	t <sub>INREG</sub>	—	1.60	—	2.60	ns
t <sub>EXP</sub>	Product Term Expander Delay	t <sub>MCELL</sub>	—	0.45	—	0.50	ns
t <sub>BLA</sub>	Additional Block Loading Adders	t <sub>ROUTE</sub>	—	0.05	—	0.05	ns
<b>t<sub>IOI</sub> Input Buffer Delays</b>							
LVTTL_in	Using LVTTTL Standard with Hysteresis	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.60	—	0.60	ns
LVC MOS15_in	Using LVC MOS 1.5 Standard	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.20	—	0.20	ns
LVC MOS18_in	Using LVC MOS 1.8 Standard	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.00	—	0.00	ns
LVC MOS25_in	Using LVC MOS 2.5 Standard with Hysteresis	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.80	—	0.80	ns
LVC MOS33_in	Using LVC MOS 3.3 Standard with Hysteresis	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t <sub>IN</sub> , t <sub>GCLK_IN</sub> , t <sub>GOE</sub>	—	0.80	—	0.80	ns
<b>t<sub>IOO</sub> Output Buffer Delays</b>							
LVTTL_out	Output Configured as TTL Buffer	t <sub>EN</sub> , t <sub>DIS</sub> , t <sub>BUF</sub>	—	0.20	—	0.20	ns

## Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V <sub>CC</sub>	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V <sub>CC00</sub> , V <sub>CC01</sub>	The power supply pins for each I/O bank.	
yzz	Input/Output <sup>1</sup> – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

## ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

**ispMACH 4000ZE Power Supply and NC Connections<sup>1</sup> (Cont.)**

Signal	132 ucBGA <sup>3</sup>	144 csBGA <sup>3</sup>	144 TQFP <sup>2</sup>
VCC	M1, M7, A12, B5	H5, H8, E8, E5	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	B1, H4, L2, J5, A4	E4, F4, G4, J5, D5	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	K9, L12, F12, D9, C7	J8, H9, G9, F9, D8	64, 75, 91, 106, 119
GND	E5, E8, H5, H8	F6, G6, G7, F7	1, 37, 73, 109
GND (Bank 0)	E2, H2, M4, B7, B3	G5, H4, H6, E6, F5	10, 18 <sup>4</sup> , 27, 46, 127, 137
GND (Bank 1)	L7, J9, H12, E9, A9	H7, J9, G8, F8, E7	55, 65, 82, 90 <sup>4</sup> , 99, 118
NC	—	<b>4064ZE:</b> E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 <b>4128ZE:</b> D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2	<b>4128ZE:</b> 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 <b>4256ZE:</b> 18, 90

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

**ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

**ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA**

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
B2	-	TDI	TDI
B1	0	A5	A8
C2	0	A6	A10
C1	0	A7	A11
GND*	0	GND (Bank 0)	GND (Bank 0)
C3	0	NC	A12
E3	0	VCCO (Bank 0)	VCCO (Bank 0)
D1	0	A8	B15
D2	0	NC	B14
E1	0	A9	B13
D3	0	A10	B12
F1	0	A11	B11
E2	0	NC	B10
G1	0	NC	B9
F2	0	NC	B8
H1	-	TCK	TCK
E4	-	VCC	VCC
GND*	-	GND	GND
G2	0	A12	B6
H2	0	NC	B5
H3	0	A13	B4
GND*	0	NC	GND (Bank 0)
F4	0	NC	VCCO (Bank 0)
G3	0	A14	B3
F3	0	NC	B2
H4	0	A15	B0
G4	0	CLK1/I	CLK1/I
H5	1	CLK2/I	CLK2/I
F5	1	B0	C0
G5	1	B1	C1
G6	1	B2	C2
H6	1	B3	C4
F6	1	B4	C5
H7	1	NC	C6
H8	-	TMS	TMS
G7	1	B5	C8
F7	1	B6	C10
G8	1	B7	C11
GND*	1	GND (Bank 0)	GND (Bank 1)
F8	1	NC	C12
D6	1	VCCO (Bank 1)	VCCO (Bank 1)
E8	1	B8	D15

**ispMACH 4064ZE Logic Signal Connections: 64 ucBGA**

Ball Number	Bank Number	GLB/MC/Pad
A1	-	TDI
B1	0	A8
B2	0	A10
B3	0	A11
GND*	0	GND (Bank 0)
C1	0	A12
C3	0	VCCO (Bank 0)
C2	0	B15
D1	0	B14
D2	0	B13
D3	0	B12
E1	0	B11
E2	0	B10
E3	0	B9
F1	0	B8
F2	-	TCK
E4	-	VCC
GND*	-	GND
H2	0	B6
H1	0	B5
G1	0	B4
GND*	0	GND (Bank 0)
F3	0	VCCO (Bank 0)
G2	0	B3
G3	0	B2
H3	0	B0
G4	0	CLK1/I
F4	1	CLK2/I
H4	1	C0
H5	1	C1
G5	1	C2
H6	1	C4
H7	1	C5
H8	1	C6
G8	-	TMS
G7	1	C8
G6	1	C10
F8	1	C11
GND*	1	GND (Bank 1)
F7	1	C12
F6	1	VCCO (Bank 1)
F5	1	D15
E8	1	D14



**ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

\* All bonded grounds are connected to the following two balls, D4 and E5.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
 100 TQFP (Cont.)**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

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**ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
A2	0	A14

\* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
144 csBGA (Cont.)**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
C7	1	CLK3/I	CLK3/I	CLK3/I
E6	0	NC Ball	GND (Bank 0)	GND (Bank 0)
A7	0	CLK0/I	CLK0/I	CLK0/I
E5	-	VCC	VCC	VCC
D6	0	A0/GOE0	A0/GOE0	A2/GOE0
B6	0	A1	A1	A4
A6	0	A2	A2	A6
C6	0	A3	A4	A8
B5	0	NC Ball	A5	A10
A5	0	NC Ball	A6	A12
D5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
F5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
A4	0	A4	A8	B2
B4	0	A5	A9	B4
C5	0	A6	A10	B6
A3	0	A7	A12	B8
C4	0	NC Ball	A13	B10
B3	0	NC Ball	A14	B12
A2	0	NC Ball	NC Ball	B14

\* This pin is input only for the LC4064ZE.

**ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10