Lattice Semiconductor Corporation - LC4064ZE-5UMN64I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	48
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-VFBGA, CSPBGA
Supplier Device Package	64-UCBGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-5umn64i

Introduction

The high performance ispMACH 4000ZE family from Lattice offers an ultra low power CPLD solution. The new family is based on Lattice's industry-leading ispMACH 4000 architecture. Retaining the best of the previous generation, the ispMACH 4000ZE architecture focuses on significant innovations to combine high performance with low power in a flexible CPLD family. For example, the family's new Power Guard feature minimizes dynamic power consumption by preventing internal logic toggling due to unnecessary I/O pin activity.

The ispMACH 4000ZE combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000ZE family offers densities ranging from 32 to 256 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA), and Ultra Chip Scale BGA (ucBGA) packages ranging from 32 to 144 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

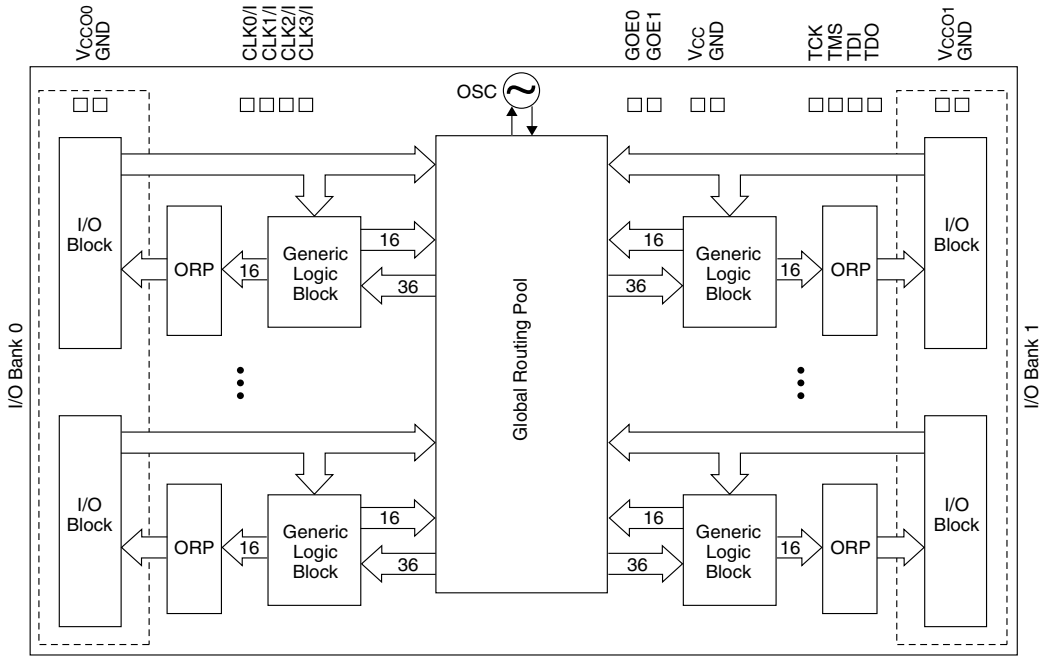
A user programmable internal oscillator and a timer are included in the device for tasks like LED control, keyboard scanner and similar housekeeping type state machines. This feature can be optionally disabled to save power.

The ispMACH 4000ZE family has enhanced system integration capabilities. It supports a 1.8V supply voltage and 3.3V, 2.5V, 1.8V and 1.5V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000ZE also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a "per-pin" basis. The ispMACH 4000ZE family members are 1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000ZE devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

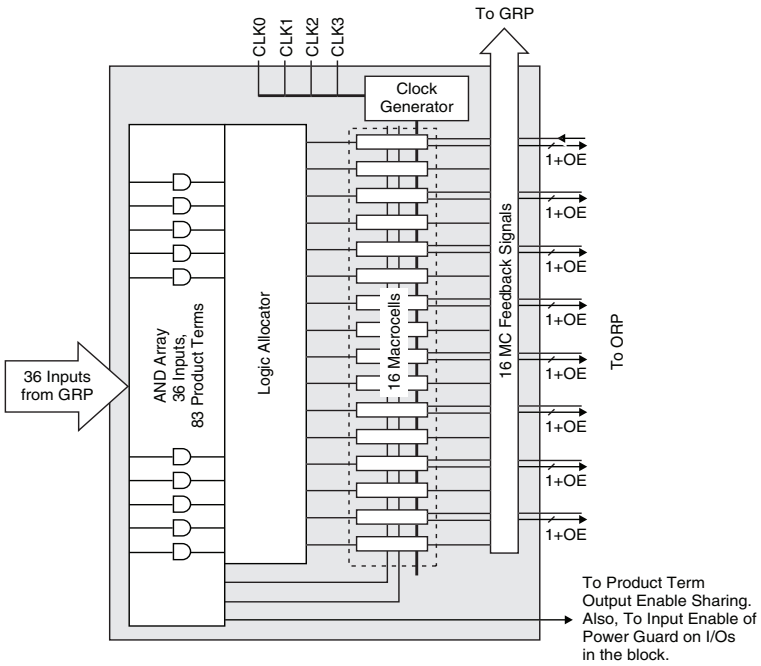
Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Table 4. Product Term Expansion Capability

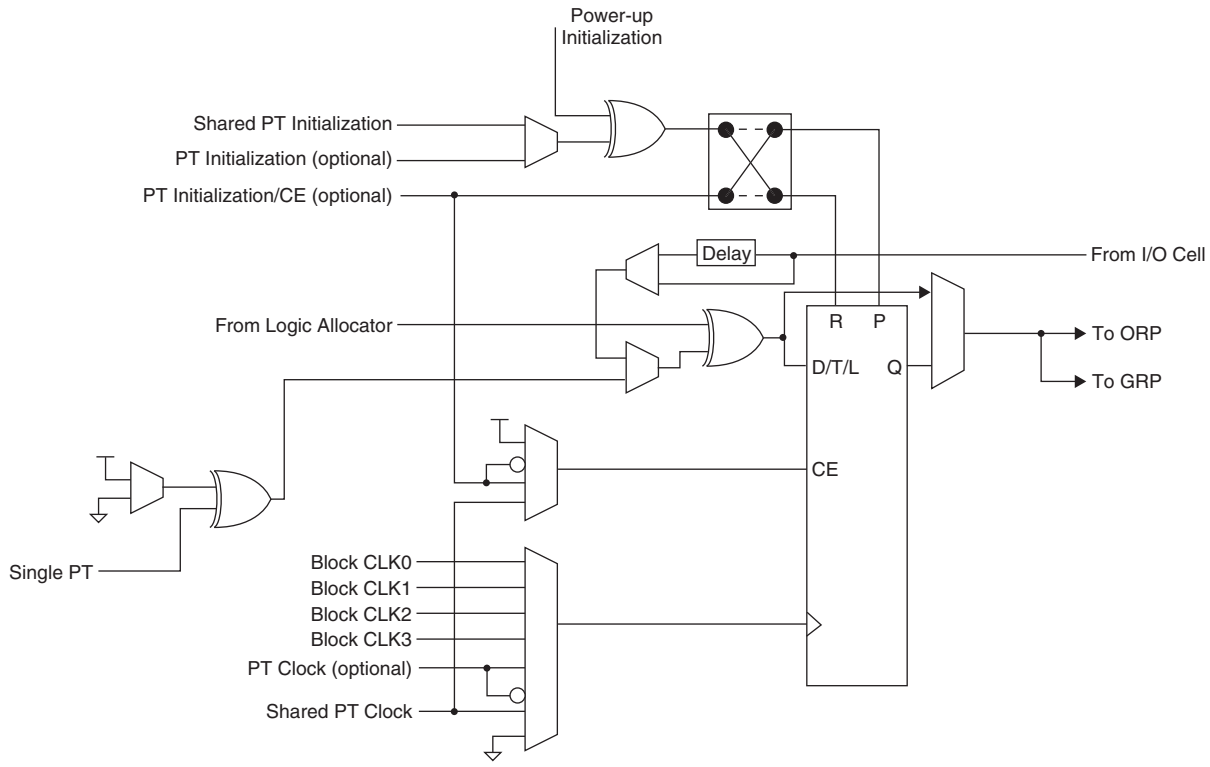
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 Õ M4 Õ M8 Õ M12 Õ M0	75
Chain-1	M1 Õ M5 Õ M9 Õ M13 Õ M1	80
Chain-2	M2 Õ M6 Õ M10 Õ M14 Õ M2	75
Chain-3	M3 Õ M7 Õ M11 Õ M15 Õ M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, …, H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, …, P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, Advanced Features of the ispMACH 4000ZE Family.

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . . -0.5 to 5.5V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (T_j) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
LVCMOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input Leakage Current	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-20	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-20	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

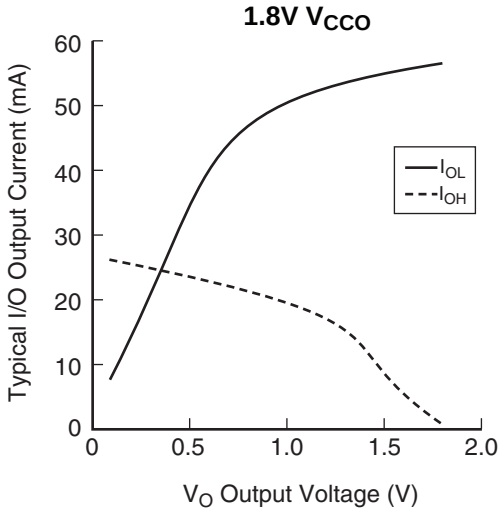
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T_A = 25°C, f = 1.0MHz.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.5[2]	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from V_{CC}, if the ispMACH 4000ZE V_{CC} and the V_{CC} of the driving device (V_{CC}d-d; that determines steady state V_{IH}) are in the extreme range of their specifications. Typically, DC current drawn from V_{CC} will be 2µA per input.

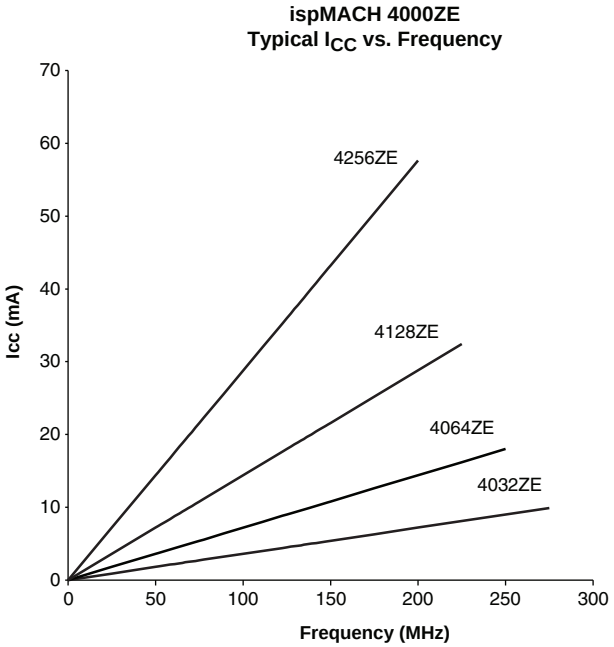


ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	All Devices				Units
		-5		-7		
		Min.	Max.	Min.	Max.	
In/Out Delays						
t_{IN}	Input Buffer Delay	—	1.05	—	1.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.15	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	4.30	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.70	ns
t_{PGSU}	Input Power Guard Setup Time	—	4.30	—	5.60	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	6.00	—	8.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dis-sertation	—	5.00	—	7.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	2.25	—	2.50	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.75	—	0.30	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_S	D-Register Setup Time (Global Clock)	0.90	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.00	—	2.35	—	ns
t_H	D-Register Hold Time	2.00	—	3.25	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.10	—	1.45	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.20	—	2.65	—	ns
t_{HT}	T-Resister Hold Time	2.00	—	3.25	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.20	—	0.65	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.40	—	2.05	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.10	—	1.20	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.45	—	0.75	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.90	—	1.55	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.00	—	2.05	—	ns
t_{HL}	Latch Hold Time	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.35	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.95	—	0.28	ns

Power Consumption



Power Estimation Coefficients[1]

Device	A	B
ispMACH 4032ZE	0.010	0.009
ispMACH 4064ZE	0.011	0.009
ispMACH 4128ZE	0.012	0.009
ispMACH 4256ZE	0.013	0.009

1. For further information about the use of these coefficients, refer to TN1187, Power Estimation in ispMACH 4000ZE Devices.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

ispMACH 4000ZE Power Supply and NC Connections[1]

Signal	48 TQFP[2]	64 csBGA[3, 4]	64 ucBGA[3, 4]	100 TQFP[2]
VCC	12, 36	E4, D5	E4, D5	25, 40, 75, 90
VCCO0 VCCO (Bank 0)	6	**4032ZE:** E3 **4064ZE:** E3, F4	C3, F3	13, 33, 95
VCCO1 VCCO (Bank 1)	30	**4032ZE:** D6 **4064ZE:** D6, C6	F6, A6	45, 63, 83
GND	13, 37	D4, E5	D4, D5	1, 26, 51, 76
GND (Bank 0)	5	D4, E5	D4, D5	7, 18, 32, 96
GND (Bank 1)	29	D4, E5	D4, D5	46, 57, 68, 82
NC	—	—	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
83	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
84	1	D3	H6	P12
85	1	D2	H4	P10
86	1	D1	H2	P6
87	1	D0/GOE1	H0/GOE1	P2/GOE1
88	1	CLK3/I	CLK3/I	CLK3/I
89	0	CLK0/I	CLK0/I	CLK0/I
90	-	VCC	VCC	VCC
91	0	A0/GOE0	A0/GOE0	A2/GOE0
92	0	A1	A2	A6
93	0	A2	A4	A10
94	0	A3	A6	A12
95	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
96	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
97	0	A4	A8	B2
98	0	A5	A10	B6
99	0	A6	A12	B10
100	0	A7	A14	B12

* This pin is input only.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
F6	-	GND	GND	GND
A1	-	TDI	TDI	TDI
E4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
B2	0	NC Ball	B0	C12
B1	0	NC Ball	B1	C10
C3	0	A8	B2	C8
C2	0	A9	B4	C6
C1	0	A10	B5	C4
D1	0	A11	B6	C2
G5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
D2	0	NC Ball	NC Ball	D14
D3	0	NC Ball	NC Ball	D12
E1	0	NC Ball	B8	D10
E2	0	A12	B9	D8
F2	0	A13	B10	D6
D4	0	A14	B12	D4
F1	0	A15	B13	D2
F3*	0	I	B14	D0
F4	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
G1	0	B15	C14	E0
E3	0	B14	C13	E2
G2	0	B13	C12	E4
G3	0	B12	C10	E6
H1	0	NC Ball	C9	E8
H3	0	NC Ball	C8	E10
H2	0	NC Ball	NC Ball	E12
H4	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J1	0	B11	C6	F2
J3	0	B10	C5	F4
J2	0	B9	C4	F6
K1	0	B8	C2	F8
K2*	0	I	C1	F10
L1	0	NC Ball	C0	F12
G4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
L2	-	TCK	TCK	TCK
H5	-	VCC	VCC	VCC
G6	-	GND	GND	GND
M1	0	NC Ball	NC Ball	G14
K3	0	NC Ball	NC Ball	G12
M2	0	NC Ball	D14	G10
L3*	0	I	D13	G8

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J12	1	NC Ball	NC Ball	L14
J11	1	NC Ball	NC Ball	L12
H10	1	NC Ball	F8	L10
H12	1	C12	F9	L8
G11	1	C13	F10	L6
H11	1	C14	F12	L4
G12	1	C15	F13	L2
G10*	1	I	F14	L0
G9	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
F12	1	D15	G14	M0
F11	1	D14	G13	M2
E11	1	D13	G12	M4
E12	1	D12	G10	M6
D10	1	NC Ball	G9	M8
F10	1	NC Ball	G8	M10
D12	1	NC Ball	NC Ball	M12
F8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
E10	1	D11	G6	N2
D11	1	D10	G5	N4
E9	1	D9	G4	N6
C12	1	D8	G2	N8
C11*	1	I	G1	N10
B12	1	NC Ball	G0	N12
F9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
B11	-	TDO	TDO	TDO
E8	-	VCC	VCC	VCC
F7	-	GND	GND	GND
A12	1	NC Ball	NC Ball	O14
C10	1	NC Ball	NC Ball	O12
B10	1	NC Ball	H14	O10
A11*	1	I	H13	O8
D9	1	D7	H12	O6
B9	1	D6	H10	O4
C9	1	D5	H9	O2
A10	1	D4	H8	O0
E7	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
D8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
A9	1	NC Ball	H6	P12
B8	1	NC Ball	H5	P10
C8	1	D3	H4	P8
A8	1	D2	H2	P6
D7	1	D1	H1	P4
B7	1	D0/GOE1	H0/GOE1	P2/GOE1

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND
2	-	TDI	TDI
3	0	VCCO (Bank 0)	VCCO (Bank 0)
4	0	B0	C12
5	0	B1	C10
6	0	B2	C8
7	0	B4	C6
8	0	B5	C4
9	0	B6	C2
10	0	GND (Bank 0)	GND (Bank 0)
11	0	B8	D14
12	0	B9	D12
13	0	B10	D10
14	0	B12	D8
15	0	B13	D6
16	0	B14	D4
17*	0	NC	I
18	0	GND (Bank 0)	NC
19	0	VCCO (Bank 0)	VCCO (Bank 0)
20*	0	NC	I
21	0	C14	E2
22	0	C13	E4
23	0	C12	E6
24	0	C10	E8
25	0	C9	E10
26	0	C8	E12
27	0	GND (Bank 0)	GND (Bank 0)
28	0	C6	F2
29	0	C5	F4
30	0	C4	F6
31	0	C2	F8
32	0	C1	F10
33	0	C0	F12
34	0	VCCO (Bank 0)	VCCO (Bank 0)
35	-	TCK	TCK
36	-	VCC	VCC
37	-	GND	GND
38*	0	NC	I
39	0	D14	G12
40	0	D13	G10
41	0	D12	G8
42	0	D10	G6

Industrial

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
	LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

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Revision History

Date	Version	Change Summary
April 2008	01.0	Initial release.
July 2008	01.1	Updated Features bullets.
		Updated typical Hysteresis voltage.
		Updated Power Guard for Dedicated Inputs section.
		Updated DC Electrical Characteristics table.
		Updated Supply Current table.
		Updated I/O DC Electrical Characteristics table and note 2.
		Updated ispMACH 4000ZE Timing Model.
		Added new parameters for the Internal Oscillator.
		Updated ORP Reference table.
		Updated Power Supply and NC Connections table.
		Updated 100 TQFP Logic Signal Connections table with LC4128ZE and 4256ZE.
		Updated 144 csBGA Logic Signal Connections table with LC4128ZE and 4256ZE.
		Added 144 TQFP Logic Signal Connections table.
August 2008	01.2	Data sheet status changed from advance to final.
		Updated Supply Current table.
		Updated External Switching Characteristics.
		Updated Internal Timing Parameters.
		Updated Power Consumption graph and Power Estimation Coefficients table.
		Updated Ordering Information mark format example.
December 2008	01.3	Updated ispMACH 4000ZE Family Selection Guide table to include 64-ball ucBGA and 132-ball ucBGA packages.
		Updated ispMACH 4000ZE Power Supply and NC Connections table to include 64-ball ucBGA and 132-ball ucBGA packages.
		Added Logic Signal Connections tables for 64-ball ucBGA and 132-ball ucBGA packages.
		Updated Part Number Description diagram for 64-ball ucBGA and 132-ball ucBGA packages.
		Updated Ordering Information tables for 64-ball ucBGA and 132-ball ucBGA packages.
May 2009	01.4	Correction to t_{CW}, t_{GW}, t_{WIR} and f_{MAX} parameters in External Switching Characteristics table.
June 2011	01.5	Added copper bond package part numbers.
		Added footnote 4 to Absolute Maximum Ratings.
February 2012	01.6	Updated document with new corporate logo.
February 2012	01.7	Removed copper bond packaging information. Refer to PCN 04A-12 for further information.
		Updated topside marks with new logos in the Ordering Information section.