Lattice Semiconductor Corporation - LC4064ZE-7TCN100C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-7tcn100c

The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

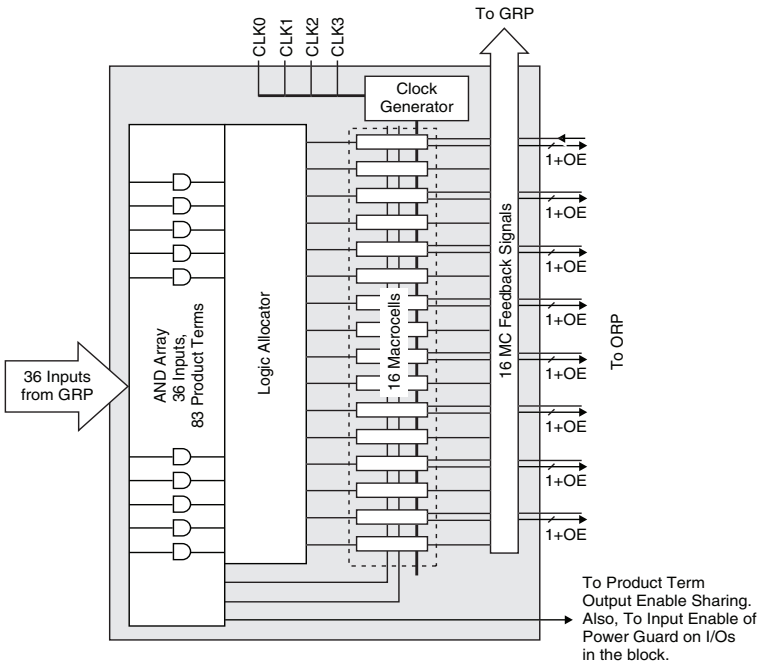
Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block



AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Table 4. Product Term Expansion Capability

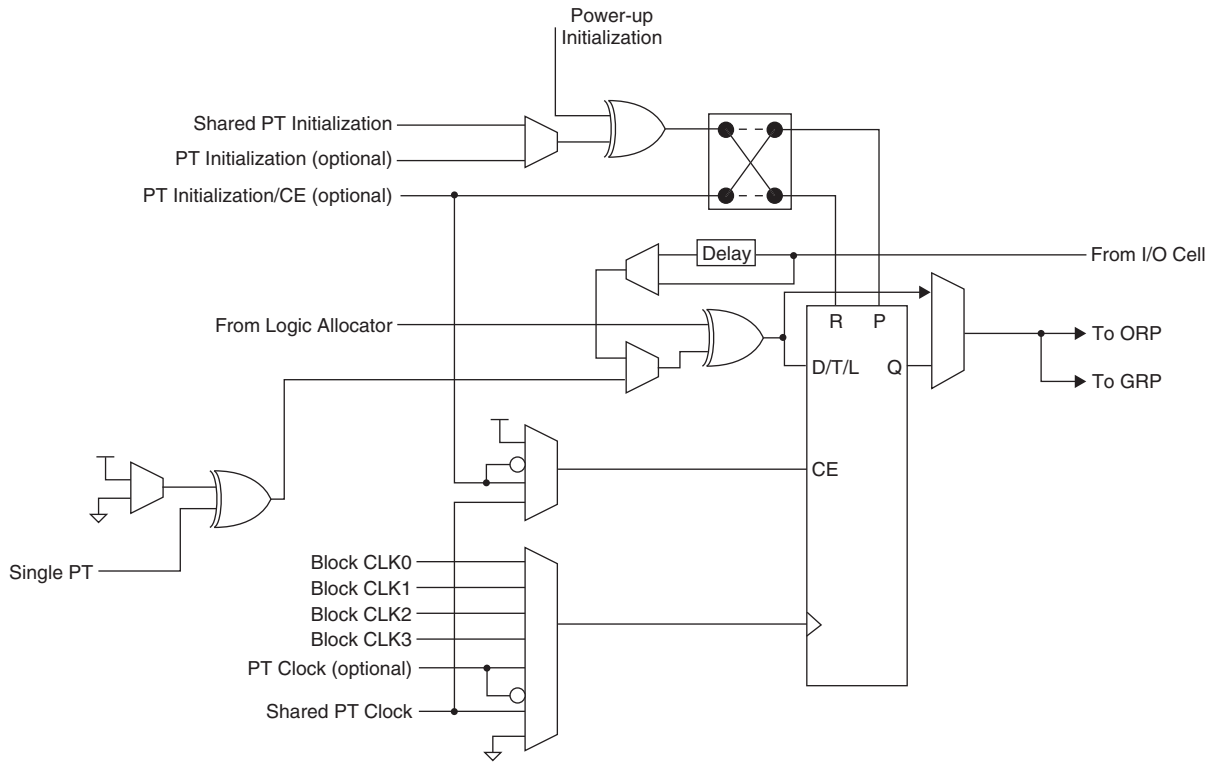
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 Õ M4 Õ M8 Õ M12 Õ M0	75
Chain-1	M1 Õ M5 Õ M9 Õ M13 Õ M1	80
Chain-2	M2 Õ M6 Õ M10 Õ M14 Õ M2	75
Chain-3	M3 Õ M7 Õ M11 Õ M15 Õ M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, …, H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, …, P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, Advanced Features of the ispMACH 4000ZE Family.

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
LVCMOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

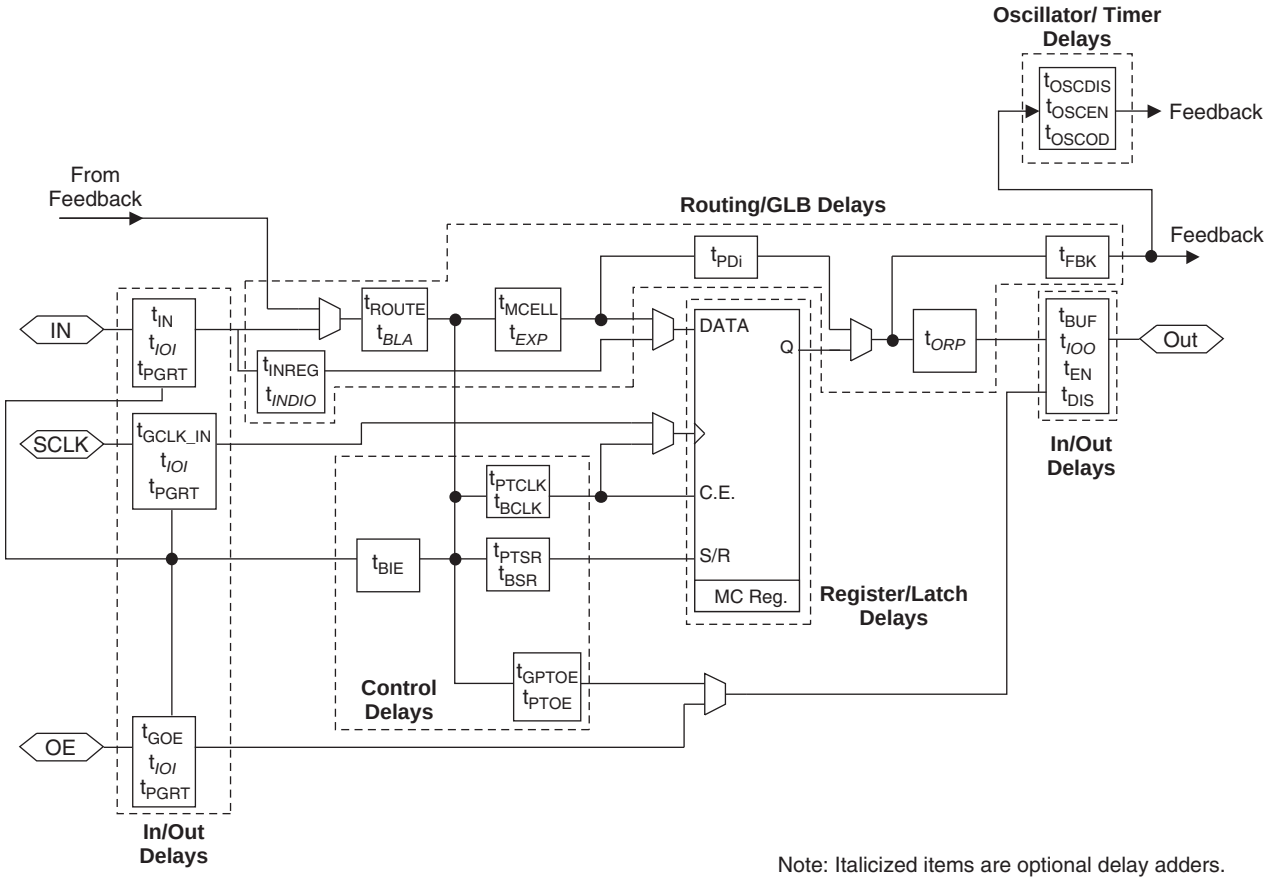
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input Leakage Current	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-20	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-20	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T_A = 25°C, f = 1.0MHz.

Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines.

Figure 16. ispMACH 4000ZE Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	All Devices				Units
		-5		-7		
		Min.	Max.	Min.	Max.	
In/Out Delays						
t_{IN}	Input Buffer Delay	—	1.05	—	1.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.15	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	4.30	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.70	ns
t_{PGSU}	Input Power Guard Setup Time	—	4.30	—	5.60	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	6.00	—	8.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dis-sertation	—	5.00	—	7.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	2.25	—	2.50	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.75	—	0.30	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_S	D-Register Setup Time (Global Clock)	0.90	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.00	—	2.35	—	ns
t_H	D-Register Hold Time	2.00	—	3.25	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.10	—	1.45	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.20	—	2.65	—	ns
t_{HT}	T-Resister Hold Time	2.00	—	3.25	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.20	—	0.65	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.40	—	2.05	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.10	—	1.20	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.45	—	0.75	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.90	—	1.55	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.00	—	2.05	—	ns
t_{HL}	Latch Hold Time	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.35	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.95	—	0.28	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		All Devices				Units
			-5		-7		
			Min.	Max.	Min.	Max.	
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	1.80	—	1.67	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.45	—	0.95	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.45	—	1.15	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.85	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.85	—	2.72	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.75	—	1.95	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.40	—	1.90	ns
t_{GPTOE}	Global PT OE Delay		—	4.20	—	3.40	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	14.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	9.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	8.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	7.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	6.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	5.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.60	—	2.60	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.45	—	0.50	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.05	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

Figure 17. Output Test Load, LVTTL and LVCMOS Standards

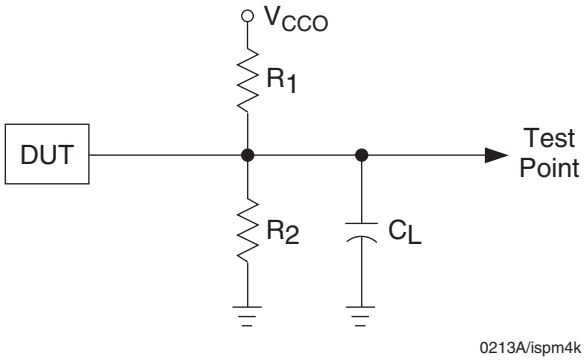


Table 13. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $\frac{V_{CCO}}{2}$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $\frac{V_{CCO}}{2}$	LVCMOS 1.8 = 1.65V
				LVCMOS 1.5 = $\frac{V_{CCO}}{2}$	LVCMOS 1.5 = 1.4V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

ispMACH 4000ZE Power Supply and NC Connections[1]

Signal	48 TQFP[2]	64 csBGA[3, 4]	64 ucBGA[3, 4]	100 TQFP[2]
VCC	12, 36	E4, D5	E4, D5	25, 40, 75, 90
VCCO0 VCCO (Bank 0)	6	**4032ZE:** E3 **4064ZE:** E3, F4	C3, F3	13, 33, 95
VCCO1 VCCO (Bank 1)	30	**4032ZE:** D6 **4064ZE:** D6, C6	F6, A6	45, 63, 83
GND	13, 37	D4, E5	D4, D5	1, 26, 51, 76
GND (Bank 0)	5	D4, E5	D4, D5	7, 18, 32, 96
GND (Bank 1)	29	D4, E5	D4, D5	46, 57, 68, 82
NC	—	—	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
E7	1	NC	D14
E6	1	B9	D13
D7	1	B10	D12
D8	1	NC	D11
C5	1	NC	D10
C7	1	B11	D9
C8	1	NC	D8
B8	-	TDO	TDO
D5	-	VCC	VCC
GND*	-	GND	GND
A8	1	B12	D7
A7	1	NC	D6
B7	1	NC	D5
A6	1	B13	D4
GND*	1	NC	GND (Bank 1)
C6	1	NC	VCCO (Bank 1)
B6	1	B14	D3
A5	1	NC	D2
B5	1	B15/GOE1	D0/GOE1
A4	1	CLK3/I	CLK3/I
C4	0	CLK0/I	CLK0/I
B4	0	A0/GOE0	A0/GOE0
B3	0	A1	A1
A3	0	A2	A2
A2	0	A3	A4
A1	0	A4	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
GND*	-	GND
A1	-	TDI
B1	0	VCCO (Bank 0)
D3	0	B0
C1	0	B1
D2	0	B2
D1	0	B4
E4	0	B5
F3	0	B6
E2	0	GND (Bank 0)
E1	0	B8
E3	0	B9
F4	0	B10
G4	0	B12
F2	0	B13
G3	0	B14
H4	0	VCCO (Bank 0)
F1	0	C14
G2	0	C13
G1	0	C12
H3	0	C10
J4	0	C9
H1	0	C8
H2	0	GND (Bank 0)
J3	0	C6
J1	0	C5
J2	0	C4
K3	0	C2
K2	0	C1
K1	0	C0
L2	0	VCCO (Bank 0)
L1	-	TCK
M1	-	VCC
GND*	-	GND
L3	0	D14
M2	0	D13
K4	0	D12
M3	0	D10
K5	0	D9
L4	0	D8
M4	0	GND (Bank 0)
J5	0	VCCO (Bank 0)
L5	0	D6

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
C7	1	CLK3/I	CLK3/I	CLK3/I
E6	0	NC Ball	GND (Bank 0)	GND (Bank 0)
A7	0	CLK0/I	CLK0/I	CLK0/I
E5	-	VCC	VCC	VCC
D6	0	A0/GOE0	A0/GOE0	A2/GOE0
B6	0	A1	A1	A4
A6	0	A2	A2	A6
C6	0	A3	A4	A8
B5	0	NC Ball	A5	A10
A5	0	NC Ball	A6	A12
D5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
F5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
A4	0	A4	A8	B2
B4	0	A5	A9	B4
C5	0	A6	A10	B6
A3	0	A7	A12	B8
C4	0	NC Ball	A13	B10
B3	0	NC Ball	A14	B12
A2	0	NC Ball	NC Ball	B14

* This pin is input only for the LC4064ZE.

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
86	1	F12	L8
87	1	F13	L6
88	1	F14	L4
89*	1	NC	I
90	1	GND (Bank 1)	NC
91	1	VCCO (Bank 1)	VCCO (Bank 1)
92*	1	NC	I
93	1	G14	M2
94	1	G13	M4
95	1	G12	M6
96	1	G10	M8
97	1	G9	M10
98	1	G8	M12
99	1	GND (Bank 1)	GND (Bank 1)
100	1	G6	N2
101	1	G5	N4
102	1	G4	N6
103	1	G2	N8
104	1	G1	N10
105	1	G0	N12
106	1	VCCO (Bank 1)	VCCO (Bank 1)
107	-	TDO	TDO
108	-	VCC	VCC
109	-	GND	GND
110*	1	NC	I
111	1	H14	O12
112	1	H13	O10
113	1	H12	O8
114	1	H10	O6
115	1	H9	O4
116	1	H8	O2
117*	1	NC	I
118	1	GND (Bank 1)	GND (Bank 1)
119	1	VCCO (Bank 1)	VCCO (Bank 1)
120	1	H6	P12
121	1	H5	P10
122	1	H4	P8
123	1	H2	P6
124	1	H1	P4
125	1	H0/GOE1	P2/GOE1
126	1	CLK3/I	CLK3/I
127	0	GND (Bank 0)	GND (Bank 0)
128	0	CLK0/I	CLK0/I

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.

Part Number Description

LC XXXX XX – XX XX XXX X XX

Device Family

Device Number
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells

Power
ZE = Zero Power, Enhanced

Speed
4 = 4.4ns (4032ZE Only)
4 = 4.7ns (4064ZE Only)
5 = 5.8ns (All Devices)
7 = 7.5ns (All Devices)

Production Status
Blank = Final production device
ES = Engineering samples

Operating Temperature Range
C = Commercial
I = Industrial

Pin/Ball Count
48 (1.0 mm thickness)
64
100
132
144

Package
TN = Lead-free TQFP
MN = Lead-free csBGA (0.5 mm pitch)
UMN = Lead-free ucBGA (0.4 mm pitch)

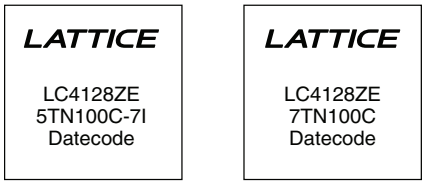
ispMACH 4000ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

Ordering Information

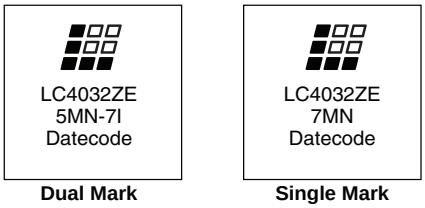
Note: ispMACH 4000ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages



Dual Mark **Single Mark**

Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages



Dual Mark **Single Mark**