Lattice Semiconductor Corporation - LC4064ZE-7TCN100I Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-7tcn100i

Table 4. Product Term Expansion Capability

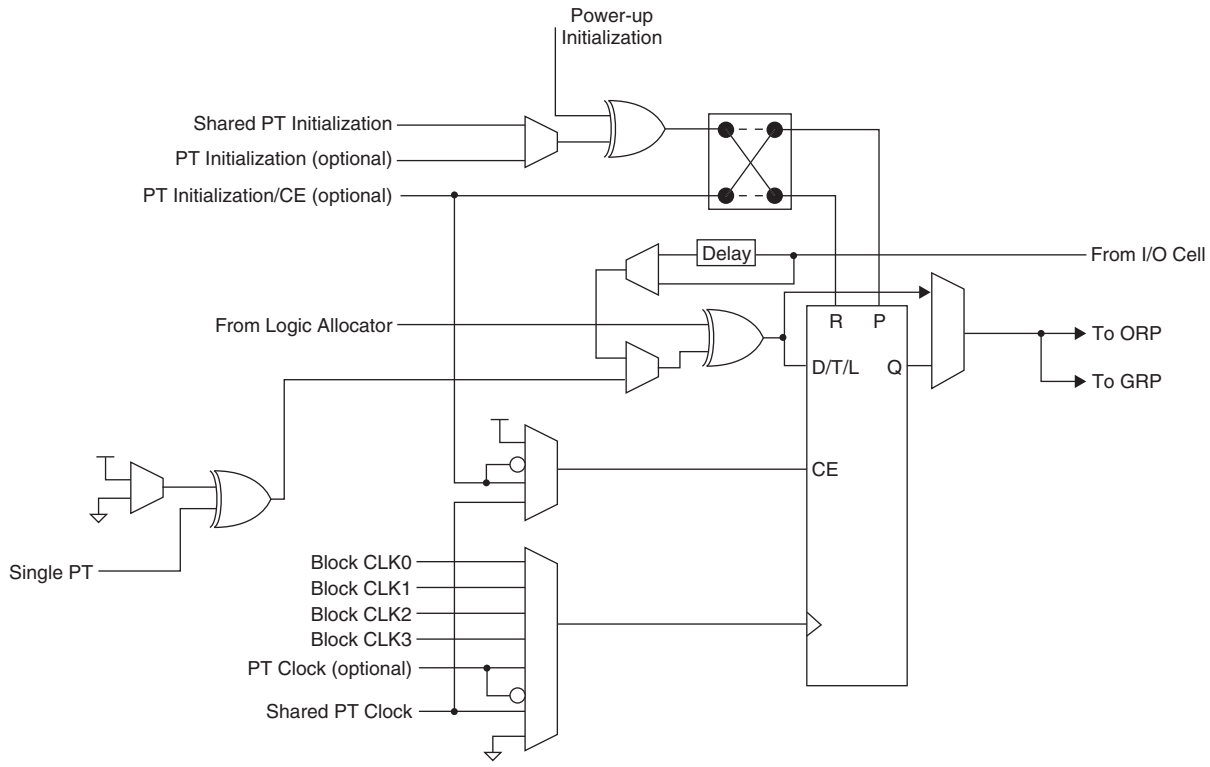
Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 Õ M4 Õ M8 Õ M12 Õ M0	75
Chain-1	M1 Õ M5 Õ M9 Õ M13 Õ M1	80
Chain-2	M2 Õ M6 Õ M10 Õ M14 Õ M2	75
Chain-3	M3 Õ M7 Õ M11 Õ M15 Õ M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

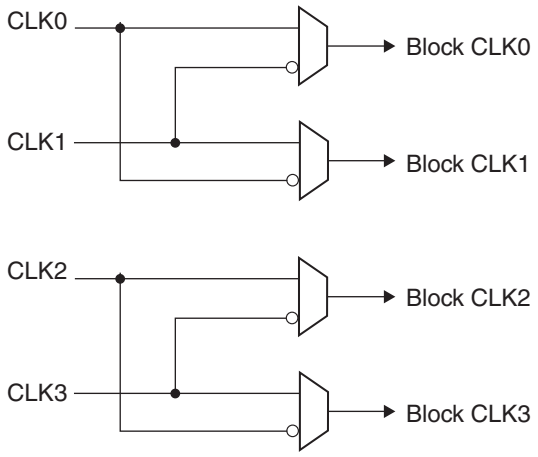
The ispMACH 4000ZE family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000ZE device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, …, H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, …, P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, Advanced Features of the ispMACH 4000ZE Family.

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Figure 13. On-Chip Oscillator and Timer

Table 11. On-Chip Oscillator and Timer Signal Names

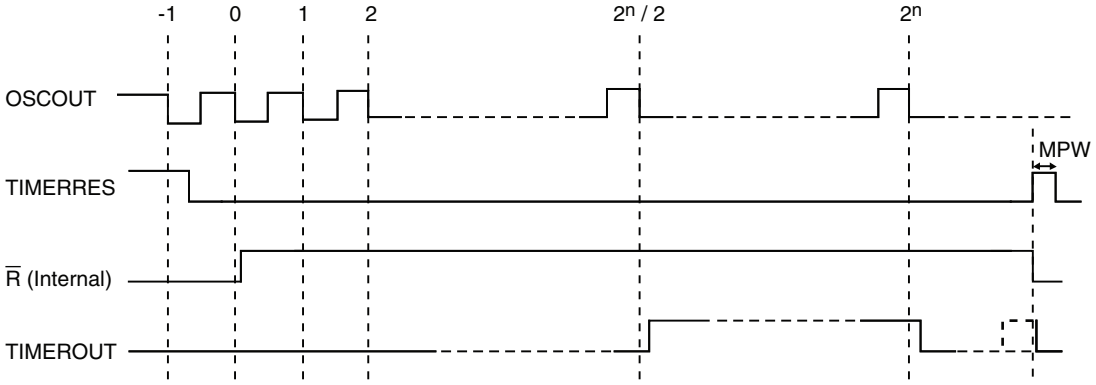
Signal Name	Input or Output	Optional / Required	Description
OSCOUT	Output	Optional	Oscillator Output (Nominal Frequency: 5MHz)
TIMEROUT	Output	Optional	Oscillator Frequency Divided by an integer TIMER_DIV (Default 128)
TIMERRES	Input	Optional	Reset the Timer
DYNOSCDIS	Input	Optional	Disables the Oscillator, resets the Timer and saves the power.

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER_DIV.

The attribute TIMER_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal "$\overline{R}$" is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT



Note: n = Number of bits in the divider (7, 10 or 20)
Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . . -0.5 to 5.5V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (T_j) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \le V_{IN} \le 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

Standard	V_{CCO} (V)[1]	
	Min.	Max.
LVTTL	3.0	3.6
LVCMOS 3.3	3.0	3.6
Extended LVCMOS 3.3	2.7	3.6
LVCMOS 2.5	2.3	2.7
LVCMOS 1.8	1.65	1.95
LVCMOS 1.5	1.4	1.6
PCI 3.3	3.0	3.6

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 2]	Input Leakage Current	$0 \le V_{IN} < V_{CCO}$	—	0.5	1	µA
I_{IH}[1]	Input High Leakage Current	$V_{CCO} < V_{IN} \le 5.5V$	—	—	10	µA
I_{PU}	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7V_{CCO}$	-20	—	-150	µA
I_{PD}	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	-20	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{BHT}$	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$V_{BHT} \le V_{IN} \le V_{CCO}$	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points	—	V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured T_A = 25°C, f = 1.0MHz.

ispMACH 4000ZE Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
In/Out Delays						
t_{IN}	Input Buffer Delay	—	0.85	—	0.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.60	—	1.60	ns
t_{GOE}	Global OE Pin Delay	—	2.25	—	2.25	ns
t_{BUF}	Delay through Output Buffer	—	0.75	—	0.90	ns
t_{EN}	Output Enable Time	—	2.25	—	2.25	ns
t_{DIS}	Output Disable Time	—	1.35	—	1.35	ns
t_{PGSU}	Input Power Guard Setup Time	—	3.30	—	3.55	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	5.00	—	5.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dissertation	—	5.00	—	5.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	1.60	—	1.70	ns
t_{PDi}	Macrocell Propagation Delay	—	0.25	—	0.25	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	0.65	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	0.90	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.55	—	0.55	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_{S}	D-Register Setup Time (Global Clock)	0.70	—	0.85	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	1.25	—	1.85	—	ns
t_{H}	D-Register Hold Time	1.50	—	1.65	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	0.90	—	1.05	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	1.45	—	1.65	—	ns
t_{HT}	T-Resister Hold Time	1.50	—	1.65	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	0.85	—	0.80	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.15	—	1.30	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	0.90	—	1.10	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.35	—	0.40	ns
t_{CES}	Clock Enable Setup Time	1.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.70	—	0.95	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	1.45	—	1.85	—	ns
t_{HL}	Latch Hold Time	1.40	—	1.80	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.40	—	0.35	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.30	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.30	—	0.30	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		All Devices				Units
			-5		-7		
			Min.	Max.	Min.	Max.	
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	1.80	—	1.67	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.45	—	0.95	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.45	—	1.15	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.85	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.85	—	2.72	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.75	—	1.95	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.40	—	1.90	ns
t_{GPTOE}	Global PT OE Delay		—	4.20	—	3.40	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	14.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	9.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	8.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	7.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	6.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	5.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.60	—	2.60	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.45	—	0.50	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.05	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

ispMACH 4000ZE Power Supply and NC Connections[1]

Signal	48 TQFP[2]	64 csBGA[3, 4]	64 ucBGA[3, 4]	100 TQFP[2]
VCC	12, 36	E4, D5	E4, D5	25, 40, 75, 90
VCCO0 VCCO (Bank 0)	6	**4032ZE:** E3 **4064ZE:** E3, F4	C3, F3	13, 33, 95
VCCO1 VCCO (Bank 1)	30	**4032ZE:** D6 **4064ZE:** D6, C6	F6, A6	45, 63, 83
GND	13, 37	D4, E5	D4, D5	1, 26, 51, 76
GND (Bank 0)	5	D4, E5	D4, D5	7, 18, 32, 96
GND (Bank 1)	29	D4, E5	D4, D5	46, 57, 68, 82
NC	—	—	—	—

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	TDI	TDI
2	0	A5	A8
3	0	A6	A10
4	0	A7	A11
5	0	GND (Bank 0)	GND (Bank 0)
6	0	VCCO (Bank 0)	VCCO (Bank 0)
7	0	A8	B15
8	0	A9	B12
9	0	A10	B10
10	0	A11	B8
11	-	TCK	TCK
12	-	VCC	VCC
13	-	GND	GND
14	0	A12	B6
15	0	A13	B4
16	0	A14	B2
17	0	A15	B0
18	0	CLK1/I	CLK1/I
19	1	CLK2/I	CLK2/I
20	1	B0	C0
21	1	B1	C1
22	1	B2	C2
23	1	B3	C4
24	1	B4	C6
25	-	TMS	TMS
26	1	B5	C8
27	1	B6	C10
28	1	B7	C11
29	1	GND (Bank 1)	GND (Bank 1)
30	1	VCCO (Bank 1)	VCCO (Bank 1)
31	1	B8	D15
32	1	B9	D12
33	1	B10	D10
34	1	B11	D8
35	-	TDO	TDO
36	-	VCC	VCC
37	-	GND	GND
38	1	B12	D6
39	1	B13	D4
40	1	B14	D2
41	1	B15/GOE1	D0/GOE1
42	1	CLK3/I	CLK3/I

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
B2	-	TDI	TDI
B1	0	A5	A8
C2	0	A6	A10
C1	0	A7	A11
GND*	0	GND (Bank 0)	GND (Bank 0)
C3	0	NC	A12
E3	0	VCCO (Bank 0)	VCCO (Bank 0)
D1	0	A8	B15
D2	0	NC	B14
E1	0	A9	B13
D3	0	A10	B12
F1	0	A11	B11
E2	0	NC	B10
G1	0	NC	B9
F2	0	NC	B8
H1	-	TCK	TCK
E4	-	VCC	VCC
GND*	-	GND	GND
G2	0	A12	B6
H2	0	NC	B5
H3	0	A13	B4
GND*	0	NC	GND (Bank 0)
F4	0	NC	VCCO (Bank 0)
G3	0	A14	B3
F3	0	NC	B2
H4	0	A15	B0
G4	0	CLK1/I	CLK1/I
H5	1	CLK2/I	CLK2/I
F5	1	B0	C0
G5	1	B1	C1
G6	1	B2	C2
H6	1	B3	C4
F6	1	B4	C5
H7	1	NC	C6
H8	-	TMS	TMS
G7	1	B5	C8
F7	1	B6	C10
G8	1	B7	C11
GND*	1	GND (Bank 0)	GND (Bank 1)
F8	1	NC	C12
D6	1	VCCO (Bank 1)	VCCO (Bank 1)
E8	1	B8	D15

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
83	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
84	1	D3	H6	P12
85	1	D2	H4	P10
86	1	D1	H2	P6
87	1	D0/GOE1	H0/GOE1	P2/GOE1
88	1	CLK3/I	CLK3/I	CLK3/I
89	0	CLK0/I	CLK0/I	CLK0/I
90	-	VCC	VCC	VCC
91	0	A0/GOE0	A0/GOE0	A2/GOE0
92	0	A1	A2	A6
93	0	A2	A4	A10
94	0	A3	A6	A12
95	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
96	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
97	0	A4	A8	B2
98	0	A5	A10	B6
99	0	A6	A12	B10
100	0	A7	A14	B12

* This pin is input only.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
GND*	-	GND
A1	-	TDI
B1	0	VCCO (Bank 0)
D3	0	B0
C1	0	B1
D2	0	B2
D1	0	B4
E4	0	B5
F3	0	B6
E2	0	GND (Bank 0)
E1	0	B8
E3	0	B9
F4	0	B10
G4	0	B12
F2	0	B13
G3	0	B14
H4	0	VCCO (Bank 0)
F1	0	C14
G2	0	C13
G1	0	C12
H3	0	C10
J4	0	C9
H1	0	C8
H2	0	GND (Bank 0)
J3	0	C6
J1	0	C5
J2	0	C4
K3	0	C2
K2	0	C1
K1	0	C0
L2	0	VCCO (Bank 0)
L1	-	TCK
M1	-	VCC
GND*	-	GND
L3	0	D14
M2	0	D13
K4	0	D12
M3	0	D10
K5	0	D9
L4	0	D8
M4	0	GND (Bank 0)
J5	0	VCCO (Bank 0)
L5	0	D6

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.

Industrial

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
	LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

Technical Support Assistance

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