# Lattice Semiconductor Corporation - LC4064ZE-7UMN64C Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 1.7V ~ 1.9V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | - |
| Number of I/O | 48 |
| Operating Temperature | 0°C ~ 90°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFBGA, CSPBGA |
| Supplier Device Package | 64-UCBGA (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-7umn64c |

## Introduction

The high performance ispMACH 4000ZE family from Lattice offers an ultra low power CPLD solution. The new family is based on Lattice's industry-leading ispMACH 4000 architecture. Retaining the best of the previous generation, the ispMACH 4000ZE architecture focuses on significant innovations to combine high performance with low power in a flexible CPLD family. For example, the family's new Power Guard feature minimizes dynamic power consumption by preventing internal logic toggling due to unnecessary I/O pin activity.

The ispMACH 4000ZE combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000ZE family offers densities ranging from 32 to 256 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP), Chip Scale BGA (csBGA), and Ultra Chip Scale BGA (ucBGA) packages ranging from 32 to 144 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

A user programmable internal oscillator and a timer are included in the device for tasks like LED control, keyboard scanner and similar housekeeping type state machines. This feature can be optionally disabled to save power.

The ispMACH 4000ZE family has enhanced system integration capabilities. It supports a 1.8V supply voltage and 3.3V, 2.5V, 1.8V and 1.5V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000ZE also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a "per-pin" basis. The ispMACH 4000ZE family members are 1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to $V_{CC}$ (logic core).

## Overview

The ispMACH 4000ZE devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

***Figure 1. Functional Block Diagram***

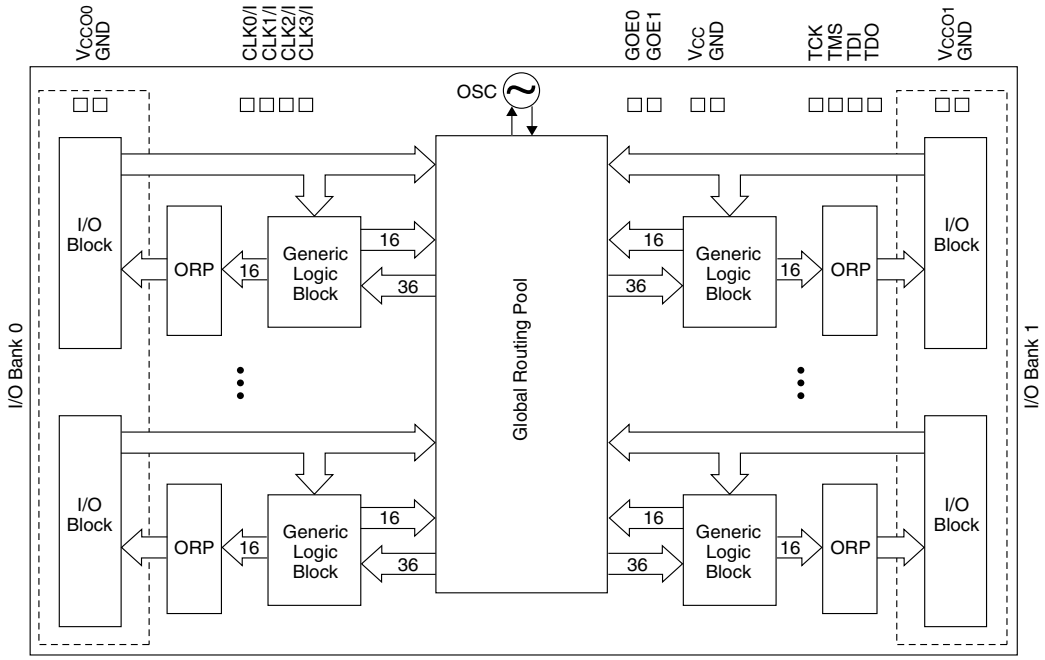
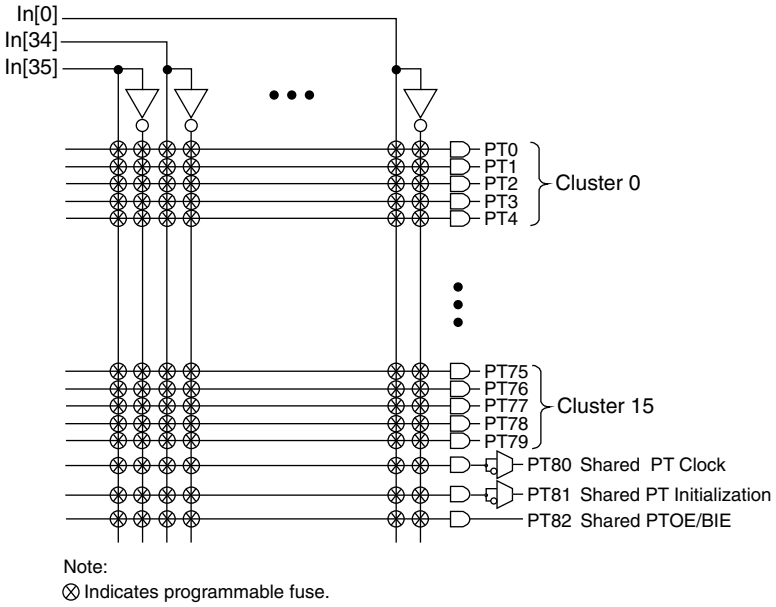


*Figure 3. AND Array*




## Enhanced Logic Allocator

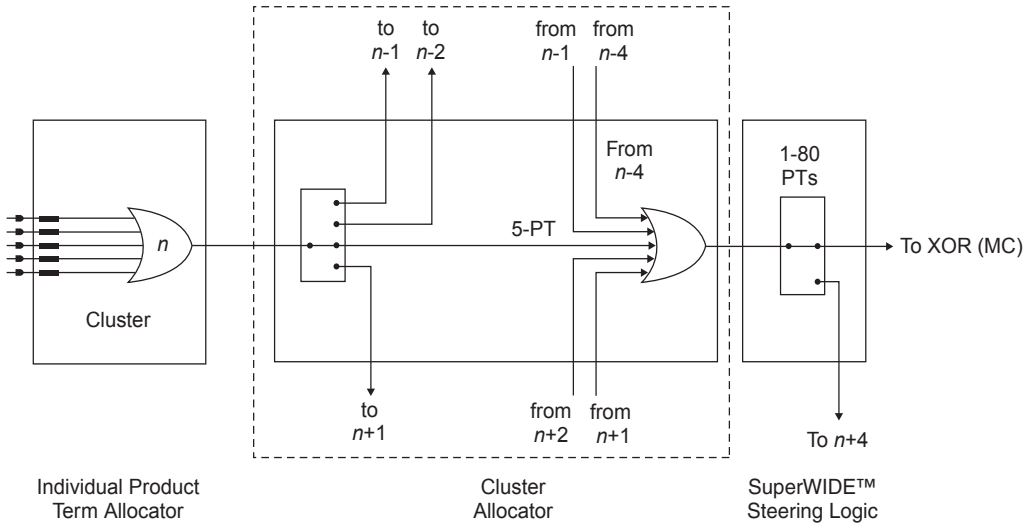
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

*Figure 4. Macrocell Slice*



## Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

***Table 2. Individual PT Steering***

| Product Term | Logic | Control |
|---|---|---|
| PT*n* | Logic PT | Single PT for XOR/OR |
| PT*n*+1 | Logic PT | Individual Clock (PT Clock) |
| PT*n*+2 | Logic PT | Individual Initialization or Individual Clock Enable (PT Initialization/CE) |
| PT*n*+3 | Logic PT | Individual Initialization (PT Initialization) |
| PT*n*+4 | Logic PT | Individual OE (PTOE) |

## Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

***Table 3. Available Clusters for Each Macrocell***

| Macrocell | Available Clusters | | | |
|---|---|---|---|---|
| M0 | — | C0 | C1 | C2 |
| M1 | C0 | C1 | C2 | C3 |
| M2 | C1 | C2 | C3 | C4 |
| M3 | C2 | C3 | C4 | C5 |
| M4 | C3 | C4 | C5 | C6 |
| M5 | C4 | C5 | C6 | C7 |
| M6 | C5 | C6 | C7 | C8 |
| M7 | C6 | C7 | C8 | C9 |
| M8 | C7 | C8 | C9 | C10 |
| M9 | C8 | C9 | C10 | C11 |
| M10 | C9 | C10 | C11 | C12 |
| M11 | C10 | C11 | C12 | C13 |
| M12 | C11 | C12 | C13 | C14 |
| M13 | C12 | C13 | C14 | C15 |
| M14 | C13 | C14 | C15 | — |
| M15 | C14 | C15 | — | — |

## Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

*Table 4. Product Term Expansion Capability*

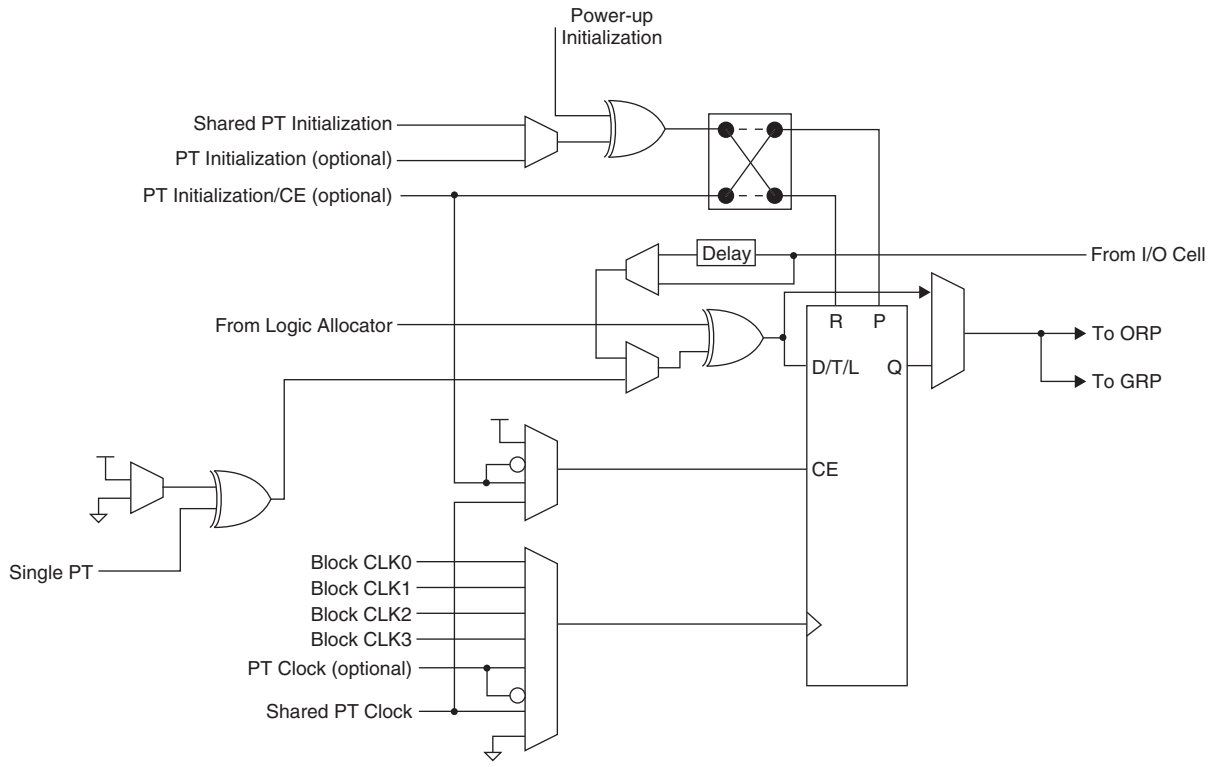
| Expansion Chains | Macrocells Associated with Expansion Chain (with Wrap Around) | Max PT/ Macrocell |
|---|---|---|
| Chain-0 | M0 Õ M4 Õ M8 Õ M12 Õ M0 | 75 |
| Chain-1 | M1 Õ M5 Õ M9 Õ M13 Õ M1 | 80 |
| Chain-2 | M2 Õ M6 Õ M10 Õ M14 Õ M2 | 75 |
| Chain-3 | M3 Õ M7 Õ M11 Õ M15 Õ M3 | 70 |

Every time the super cluster allocator is used, there is an incremental delay of $t_{EXP}$. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

## Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

*Figure 5. Macrocell*




## Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

***Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices***

| Device | Number of Logic Blocks, Power Guard Blocks and BIE Signals |
|---|---|
| ispMACH 4032ZE | Two (Blocks: A and B) |
| ispMACH 4064ZE | Four (Blocks: A, B, C and D) |
| ispMACH 4128ZE | Eight (Blocks: A, B, C, …, H) |
| ispMACH 4256ZE | Sixteen (Blocks: A, B, C, …, P) |

## Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

***Table 9. Dedicated Clock Inputs to BIE Association***

| CLK/I | 32 MC Block | 64MC Block | 128MC Block | 256MC Block |
|---|---|---|---|---|
| CLK0 / I | A | A | A | A |
| CLK1 / I | A | B | D | H |
| CLK2 / I | B | C | E | I |
| CLK3 / I | B | D | H | P |

***Table 10. Dedicated Inputs to BIE Association***

| Dedicated Input | 4064ZE Block | 4128ZE Block | 4256ZE Block |
|---|---|---|---|
| 0 | A | B | D |
| 1 | B | C | E |
| 2 | B | D | G |
| 3 | C | F | G |
| 4 | D | G | J |
| 5 | D | H | L |
| 6 | — | — | M |
| 7 | — | — | O |
| 8 | — | — | O |
| 9 | — | — | B |

For more information on the Power Guard function refer to TN1174, Advanced Features of the ispMACH 4000ZE Family.

# Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

*Table 12. OSC and TIMER MC Designation*

| Device | Macrocell | Block Number | MC Number |
|---|---|---|---|
| ispMACH 4032ZE | OSC MC<br>TIMER MC | A<br>B | 15<br>15 |
| ispMACH 4064ZE | OSC MC<br>TIMER MC | A<br>D | 15<br>15 |
| ispMACH 4128ZE | OSC MC<br>TIMER MC | A<br>G | 15<br>15 |
| ispMACH 4256ZE | OSC MC<br>TIMER MC | C<br>F | 15<br>15 |

## Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced $E^2$ low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

## IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

## I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

## IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

## Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage ($V_{CC}$) . . . . . -0.5 to 2.5V

Output Supply Voltage ($V_{CCO}$) . . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . . -0.5 to 5.5V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature ($T_j$) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of ($V_{IH}$ (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

## Recommended Operating Conditions

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Standard Voltage Operation | 1.7 | 1.9 | V |
| | | Extended Voltage Operation | 1.6[1] | 1.9 | V |
| $T_j$ | Junction Temperature (Commercial) | | 0 | 90 | °C |
| | Junction Temperature (Industrial) | | -40 | 105 | °C |

1. Devices operating at 1.6V can expect performance degradation up to 35%.

## Erase Reprogram Specifications

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Erase/Reprogram Cycle | 1,000 | — | Cycles |

Note: Valid over commercial temperature range.

## Hot Socketing Characteristics[1,2,3]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Input or I/O Leakage Current | $0 \le V_{IN} \le 3.0V$, Tj = 105°C | — | ±30 | ±150 | µA |
| | | $0 \le V_{IN} \le 3.0V$, Tj = 130°C | — | ±30 | ±200 | µA |

1. Insensitive to sequence of $V_{CC}$ or $V_{CCO}$. However, assumes monotonic rise/fall rates for $V_{CC}$ and $V_{CCO}$, provided ($V_{IN}$ - $V_{CCO}$) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. $I_{DK}$ is additive to $I_{PU}$, $I_{PD}$ or $I_{BH}$. Device defaults to pull-up until fuse circuitry is active.

## I/O Recommended Operating Conditions

| Standard | $V_{CCO}$ (V)[1] | |
|---|---|---|
| | Min. | Max. |
| LVTTL | 3.0 | 3.6 |
| LVCMOS 3.3 | 3.0 | 3.6 |
| Extended LVCMOS 3.3 | 2.7 | 3.6 |
| LVCMOS 2.5 | 2.3 | 2.7 |
| LVCMOS 1.8 | 1.65 | 1.95 |
| LVCMOS 1.5 | 1.4 | 1.6 |
| PCI 3.3 | 3.0 | 3.6 |

1. Typical values for $V_{CCO}$ are the average of the min. and max. values.

## DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2] | Input Leakage Current | $0 \le V_{IN} < V_{CCO}$ | — | 0.5 | 1 | µA |
| $I_{IH}$[1] | Input High Leakage Current | $V_{CCO} < V_{IN} \le 5.5V$ | — | — | 10 | µA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current | $0 \le V_{IN} \le 0.7V_{CCO}$ | -20 | — | -150 | µA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCO}$ | -20 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0V \le V_{IN} \le V_{BHT}$ | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $V_{BHT} \le V_{IN} \le V_{CCO}$ | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{CCO}$ * 0.35 | — | $V_{CCO}$ * 0.65 | V |
| $C_1$ | I/O Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 8 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_2$ | Clock Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_3$ | Global Input Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $I_{IH}$ excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured $T_A$ = 25°C, f = 1.0MHz.

## Supply Current

To minimize transient current during power-on, configure CPLD I/Os to a pull-up or float state. If this logic scenario is not possible, then the recommended power sequence should assert VCC and VCCO at the same time or VCC before VCCO.

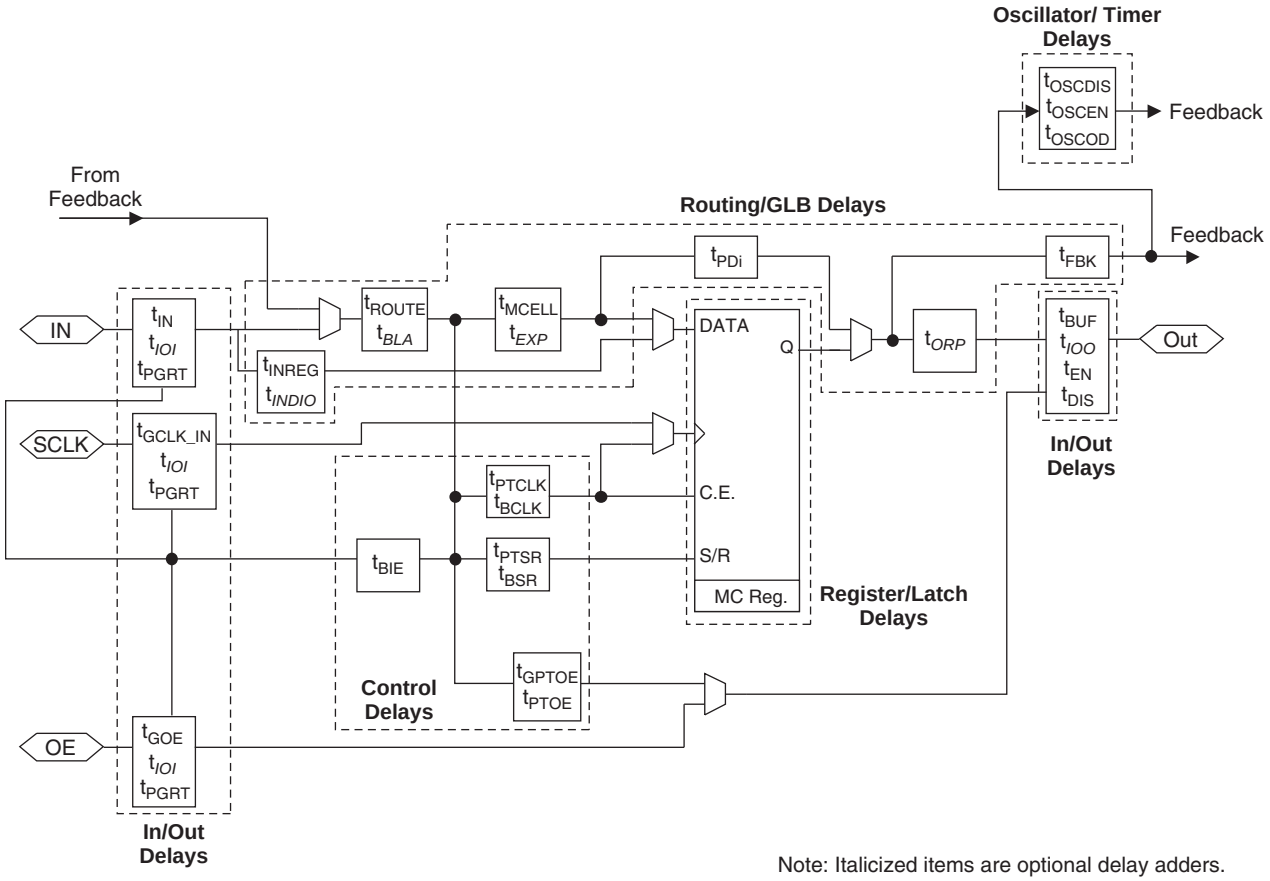
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ispMACH 4032ZE** | | | | | | |
| $ICC^{1, 2, 3, 5, 6}$ | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 50 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 58 | — | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 60 | — | µA |
| $ICC^{4, 5, 6}$ | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 10 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 13 | 25 | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 15 | 40 | µA |
| **ispMACH 4064ZE** | | | | | | |
| $ICC^{1, 2, 3, 5, 6}$ | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 80 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 89 | — | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 92 | — | µA |
| $ICC^{4, 5, 6}$ | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 11 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 15 | 30 | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 18 | 50 | µA |
| **ispMACH 4128ZE** | | | | | | |
| $ICC^{1, 2, 3, 5, 6}$ | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 168 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 190 | — | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 195 | — | µA |
| $ICC^{4, 5, 6}$ | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 12 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 16 | 40 | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 19 | 60 | µA |
| **ispMACH 4256ZE** | | | | | | |
| $ICC^{1, 2, 3, 5, 6}$ | Operating Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 341 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 361 | — | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 372 | — | µA |
| $ICC^{4, 5, 6}$ | Standby Power Supply Current | Vcc = 1.8V, $T_A$ = 25°C | — | 13 | — | µA |
| | | Vcc = 1.9V, $T_A$ = 0 to 70°C | — | 32 | 65 | µA |
| | | Vcc = 1.9V, $T_A$ = -40 to 85°C | — | 43 | 100 | µA |

1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. $I_{CC}$ varies with specific device configuration and operating frequency.
4. $V_{CCO}$ = 3.6V, $V_{IN}$ = 0V or $V_{CCO}$, bus maintenance turned off. $V_{IN}$ above $V_{CCO}$ will add transient current above the specified standby $I_{CC}$.
5. Includes $V_{CCO}$ current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15µA typical current plus additional current from any logic it drives.

## Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines.

***Figure 16. ispMACH 4000ZE Timing Model***




Note: Italicized items are optional delay adders.

# ispMACH 4000ZE Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | | LC4032ZE -4 Min. | LC4032ZE -4 Max. | LC4064ZE -4 Min. | LC4064ZE -4 Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{SRR}$ | Asynchronous Reset or Set Recovery Delay | | — | 2.00 | — | 1.70 | ns |
| **Control Delays** | | | | | | | |
| $t_{BCLK}$ | GLB PT Clock Delay | | — | 1.20 | — | 1.30 | ns |
| $t_{PTCLK}$ | Macrocell PT Clock Delay | | — | 1.40 | — | 1.50 | ns |
| $t_{BSR}$ | Block PT Set/Reset Delay | | — | 1.10 | — | 1.85 | ns |
| $t_{PTSR}$ | Macrocell PT Set/Reset Delay | | — | 1.20 | — | 1.90 | ns |
| $t_{BIE}$ | Power Guard Block Input Enable Delay | | — | 1.60 | — | 1.70 | ns |
| $t_{PTOE}$ | Macrocell PT OE Delay | | — | 2.30 | — | 3.15 | ns |
| $t_{GPTOE}$ | Global PT OE Delay | | — | 1.80 | — | 2.15 | ns |
| **Internal Oscillator** | | | | | | | |
| $t_{OSCSU}$ | Oscillator DYNOSCDIS Setup Time | | 5.00 | — | 5.00 | — | ns |
| $t_{OSCH}$ | Oscillator DYNOSCDIS Hold Time | | 5.00 | — | 5.00 | — | ns |
| $t_{OSCEN}$ | Oscillator OSCOUT Enable Time (To Stable) | | — | 5.00 | — | 5.00 | ns |
| $t_{OSCOD}$ | Oscillator Output Delay | | — | 4.00 | — | 4.00 | ns |
| $t_{OSCNOM}$ | Oscillator OSCOUT Nominal Frequency | | | 5.00 | | 5.00 | MHz |
| $t_{OSCvar}$ | Oscillator Variation of Nominal Frequency | | — | 30 | — | 30 | % |
| $t_{TMRCO20}$ | Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider) | | — | 12.50 | — | 12.50 | ns |
| $t_{TMRCO10}$ | Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider) | | — | 7.50 | — | 7.50 | ns |
| $t_{TMRCO7}$ | Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider) | | — | 6.00 | — | 6.00 | ns |
| $t_{TMRRSTO}$ | Oscillator TIMEROUT Reset to Out (Going Low) | | — | 5.00 | — | 5.00 | ns |
| $t_{TMRRR}$ | Oscillator TIMEROUT Asynchronous Reset Recovery Delay | | — | 4.00 | — | 4.00 | ns |
| $t_{TMRRSTPW}$ | Oscillator TIMEROUT Reset Minimum Pulse Width | | 3.00 | — | 3.00 | — | ns |
| **Optional Delay Adjusters** | | **Base Parameter** | | | | | |
| $t_{INDIO}$ | Input Register Delay | $t_{INREG}$ | — | 1.00 | — | 1.00 | ns |
| $t_{EXP}$ | Product Term Expander Delay | $t_{MCELL}$ | — | 0.40 | — | 0.40 | ns |
| $t_{BLA}$ | Additional Block Loading Adders | $t_{ROUTE}$ | — | 0.04 | — | 0.05 | ns |
| **$t_{IOI}$ Input Buffer Delays** | | | | | | | |
| LVTTL_in | Using LVTTL Standard with Hysteresis | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.60 | — | 0.60 | ns |
| LVCMOS15_in | Using LVCMOS 1.5 Standard | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.20 | — | 0.20 | ns |
| LVCMOS18_in | Using LVCMOS 1.8 Standard | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.00 | — | 0.00 | ns |
| LVCMOS25_in | Using LVCMOS 2.5 Standard with Hysteresis | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.80 | — | 0.80 | ns |
| LVCMOS33_in | Using LVCMOS 3.3 Standard with Hysteresis | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.80 | — | 0.80 | ns |
| PCI_in | Using PCI Compatible Input with Hysteresis | $t_{IN}$, $t_{GCLK\_IN}$, $t_{GOE}$ | — | 0.80 | — | 0.80 | ns |
| **$t_{IOO}$ Output Buffer Delays** | | | | | | | |
| LVTTL_out | Output Configured as TTL Buffer | $t_{EN}$, $t_{DIS}$, $t_{BUF}$ | — | 0.20 | — | 0.20 | ns |

# ispMACH 4000ZE Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | All Devices | | | | Units |
|---|---|---|---|---|---|---|
| | | -5 | | -7 | | |
| | | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 1.05 | — | 1.90 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.95 | — | 2.15 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 3.00 | — | 4.30 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 1.10 | — | 1.30 | ns |
| $t_{EN}$ | Output Enable Time | — | 2.50 | — | 2.70 | ns |
| $t_{DIS}$ | Output Disable Time | — | 2.50 | — | 2.70 | ns |
| $t_{PGSU}$ | Input Power Guard Setup Time | — | 4.30 | — | 5.60 | ns |
| $t_{PGH}$ | Input Power Guard Hold Time | — | 0.00 | — | 0.00 | ns |
| $t_{PGPW}$ | Input Power Guard BIE Minimum Pulse Width | — | 6.00 | — | 8.00 | ns |
| $t_{PGRT}$ | Input Power Guard Recovery Time Following BIE Dis-sertation | — | 5.00 | — | 7.00 | ns |
| **Routing Delays** | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 2.25 | — | 2.50 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.45 | — | 0.50 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.65 | — | 1.00 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 1.00 | — | 1.00 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.75 | — | 0.30 | ns |
| $t_{ORP}$ | Output Routing Pool Delay | — | 0.30 | — | 0.30 | ns |
| **Register/Latch Delays** | | | | | | |
| $t_S$ | D-Register Setup Time (Global Clock) | 0.90 | — | 1.25 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 2.00 | — | 2.35 | — | ns |
| $t_H$ | D-Register Hold Time | 2.00 | — | 3.25 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.10 | — | 1.45 | — | ns |
| $t_{ST\_PT}$ | T-register Setup Time (Product Term Clock) | 2.20 | — | 2.65 | — | ns |
| $t_{HT}$ | T-Resister Hold Time | 2.00 | — | 3.25 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 1.20 | — | 0.65 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 1.40 | — | 2.05 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 1.10 | — | 1.20 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.45 | — | 0.75 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.00 | — | 2.00 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 0.00 | — | 0.00 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 0.90 | — | 1.55 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 2.00 | — | 2.05 | — | ns |
| $t_{HL}$ | Latch Hold Time | 2.00 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.35 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.95 | — | 0.28 | ns |

## ispMACH 4064ZE Logic Signal Connections: 64 ucBGA

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| A1 | - | TDI |
| B1 | 0 | A8 |
| B2 | 0 | A10 |
| B3 | 0 | A11 |
| GND* | 0 | GND (Bank 0) |
| C1 | 0 | A12 |
| C3 | 0 | VCCO (Bank 0) |
| C2 | 0 | B15 |
| D1 | 0 | B14 |
| D2 | 0 | B13 |
| D3 | 0 | B12 |
| E1 | 0 | B11 |
| E2 | 0 | B10 |
| E3 | 0 | B9 |
| F1 | 0 | B8 |
| F2 | - | TCK |
| E4 | - | VCC |
| GND* | - | GND |
| H2 | 0 | B6 |
| H1 | 0 | B5 |
| G1 | 0 | B4 |
| GND* | 0 | GND (Bank 0) |
| F3 | 0 | VCCO (Bank 0) |
| G2 | 0 | B3 |
| G3 | 0 | B2 |
| H3 | 0 | B0 |
| G4 | 0 | CLK1/I |
| F4 | 1 | CLK2/I |
| H4 | 1 | C0 |
| H5 | 1 | C1 |
| G5 | 1 | C2 |
| H6 | 1 | C4 |
| H7 | 1 | C5 |
| H8 | 1 | C6 |
| G8 | - | TMS |
| G7 | 1 | C8 |
| G6 | 1 | C10 |
| F8 | 1 | C11 |
| GND* | 1 | GND (Bank 1) |
| F7 | 1 | C12 |
| F6 | 1 | VCCO (Bank 1) |
| F5 | 1 | D15 |
| E8 | 1 | D14 |

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | GND | GND | GND |
| 2 | - | TDI | TDI | TDI |
| 3 | 0 | A8 | B0 | C12 |
| 4 | 0 | A9 | B2 | C10 |
| 5 | 0 | A10 | B4 | C6 |
| 6 | 0 | A11 | B6 | C2 |
| 7 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 8 | 0 | A12 | B8 | D12 |
| 9 | 0 | A13 | B10 | D10 |
| 10 | 0 | A14 | B12 | D6 |
| 11 | 0 | A15 | B13 | D4 |
| 12* | 0 | I | I | I |
| 13 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 14 | 0 | B15 | C14 | E4 |
| 15 | 0 | B14 | C12 | E6 |
| 16 | 0 | B13 | C10 | E10 |
| 17 | 0 | B12 | C8 | E12 |
| 18 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 19 | 0 | B11 | C6 | F2 |
| 20 | 0 | B10 | C5 | F6 |
| 21 | 0 | B9 | C4 | F10 |
| 22 | 0 | B8 | C2 | F12 |
| 23* | 0 | I | I | I |
| 24 | - | TCK | TCK | TCK |
| 25 | - | VCC | VCC | VCC |
| 26 | - | GND | GND | GND |
| 27* | 0 | I | I | I |
| 28 | 0 | B7 | D13 | G12 |
| 29 | 0 | B6 | D12 | G10 |
| 30 | 0 | B5 | D10 | G6 |
| 31 | 0 | B4 | D8 | G2 |
| 32 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 33 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 34 | 0 | B3 | D6 | H12 |
| 35 | 0 | B2 | D4 | H10 |
| 36 | 0 | B1 | D2 | H6 |
| 37 | 0 | B0 | D0 | H2 |
| 38 | 0 | CLK1/I | CLK1/I | CLK1/I |
| 39 | 1 | CLK2/I | CLK2/I | CLK2/I |
| 40 | - | VCC | VCC | VCC |
| 41 | 1 | C0 | E0 | I2 |

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 83 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| 84 | 1 | D3 | H6 | P12 |
| 85 | 1 | D2 | H4 | P10 |
| 86 | 1 | D1 | H2 | P6 |
| 87 | 1 | D0/GOE1 | H0/GOE1 | P2/GOE1 |
| 88 | 1 | CLK3/I | CLK3/I | CLK3/I |
| 89 | 0 | CLK0/I | CLK0/I | CLK0/I |
| 90 | - | VCC | VCC | VCC |
| 91 | 0 | A0/GOE0 | A0/GOE0 | A2/GOE0 |
| 92 | 0 | A1 | A2 | A6 |
| 93 | 0 | A2 | A4 | A10 |
| 94 | 0 | A3 | A6 | A12 |
| 95 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 96 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 97 | 0 | A4 | A8 | B2 |
| 98 | 0 | A5 | A10 | B6 |
| 99 | 0 | A6 | A12 | B10 |
| 100 | 0 | A7 | A14 | B12 |

* This pin is input only.

## ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| M5 | 0 | D5 |
| J6 | 0 | D4 |
| K6 | 0 | D2 |
| L6 | 0 | D1 |
| M6 | 0 | D0 |
| K7 | 0 | CLK1/I |
| L7 | 1 | GND (Bank 1) |
| J7 | 1 | CLK2/I |
| M7 | - | VCC |
| K8 | 1 | E0 |
| L8 | 1 | E1 |
| M8 | 1 | E2 |
| J8 | 1 | E4 |
| L9 | 1 | E5 |
| M9 | 1 | E6 |
| K9 | 1 | VCCO (Bank 1) |
| J9 | 1 | GND (Bank 1) |
| L10 | 1 | E8 |
| K10 | 1 | E9 |
| M10 | 1 | E10 |
| L11 | 1 | E12 |
| K12 | 1 | E13 |
| M11 | 1 | E14 |
| GND* | - | GND |
| M12 | - | TMS |
| L12 | 1 | VCCO (Bank 1) |
| K11 | 1 | F0 |
| J10 | 1 | F1 |
| H9 | 1 | F2 |
| J12 | 1 | F4 |
| J11 | 1 | F5 |
| H10 | 1 | F6 |
| H12 | 1 | GND (Bank 1) |
| G9 | 1 | F8 |
| H11 | 1 | F9 |
| F9 | 1 | F10 |
| G12 | 1 | F12 |
| G11 | 1 | F13 |
| G10 | 1 | F14 |
| F12 | 1 | VCCO (Bank 1) |
| F10 | 1 | G14 |
| F11 | 1 | G13 |
| E11 | 1 | G12 |
| E10 | 1 | G10 |

## ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| F6 | - | GND | GND | GND |
| A1 | - | TDI | TDI | TDI |
| E4 | 0 | NC Ball | VCCO (Bank 0) | VCCO (Bank 0) |
| B2 | 0 | NC Ball | B0 | C12 |
| B1 | 0 | NC Ball | B1 | C10 |
| C3 | 0 | A8 | B2 | C8 |
| C2 | 0 | A9 | B4 | C6 |
| C1 | 0 | A10 | B5 | C4 |
| D1 | 0 | A11 | B6 | C2 |
| G5 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| D2 | 0 | NC Ball | NC Ball | D14 |
| D3 | 0 | NC Ball | NC Ball | D12 |
| E1 | 0 | NC Ball | B8 | D10 |
| E2 | 0 | A12 | B9 | D8 |
| F2 | 0 | A13 | B10 | D6 |
| D4 | 0 | A14 | B12 | D4 |
| F1 | 0 | A15 | B13 | D2 |
| F3* | 0 | I | B14 | D0 |
| F4 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| G1 | 0 | B15 | C14 | E0 |
| E3 | 0 | B14 | C13 | E2 |
| G2 | 0 | B13 | C12 | E4 |
| G3 | 0 | B12 | C10 | E6 |
| H1 | 0 | NC Ball | C9 | E8 |
| H3 | 0 | NC Ball | C8 | E10 |
| H2 | 0 | NC Ball | NC Ball | E12 |
| H4 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| J1 | 0 | B11 | C6 | F2 |
| J3 | 0 | B10 | C5 | F4 |
| J2 | 0 | B9 | C4 | F6 |
| K1 | 0 | B8 | C2 | F8 |
| K2* | 0 | I | C1 | F10 |
| L1 | 0 | NC Ball | C0 | F12 |
| G4 | 0 | NC Ball | VCCO (Bank 0) | VCCO (Bank 0) |
| L2 | - | TCK | TCK | TCK |
| H5 | - | VCC | VCC | VCC |
| G6 | - | GND | GND | GND |
| M1 | 0 | NC Ball | NC Ball | G14 |
| K3 | 0 | NC Ball | NC Ball | G12 |
| M2 | 0 | NC Ball | D14 | G10 |
| L3* | 0 | I | D13 | G8 |

## Part Number Description

LC XXXX XX – XX XX XXX X XX

**Device Family**

**Device Number**
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells

**Power**
ZE = Zero Power, Enhanced

**Speed**
4 = 4.4ns (4032ZE Only)
4 = 4.7ns (4064ZE Only)
5 = 5.8ns (All Devices)
7 = 7.5ns (All Devices)

**Production Status**
Blank = Final production device
ES = Engineering samples

**Operating Temperature Range**
C = Commercial
I = Industrial

**Pin/Ball Count**
48 (1.0 mm thickness)
64
100
132
144

**Package**
TN = Lead-free TQFP
MN = Lead-free csBGA (0.5 mm pitch)
UMN = Lead-free ucBGA (0.4 mm pitch)

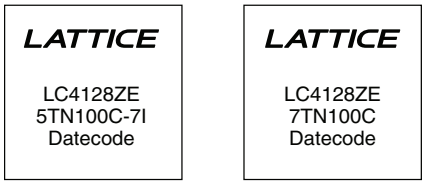
## ispMACH 4000ZE Family Speed Grade Offering

| | -4 | -5 | | -7 | |
|---|---|---|---|---|---|
| | Commercial | Commercial | Industrial | Commercial | Industrial |
| ispMACH 4032ZE | ✓ | ✓ | ✓ | ✓ | ✓ |
| ispMACH 4064ZE | ✓ | ✓ | ✓ | ✓ | ✓ |
| ispMACH 4128ZE | | ✓ | | ✓ | ✓ |
| ispMACH 4256ZE | | ✓ | | ✓ | ✓ |

## Ordering Information

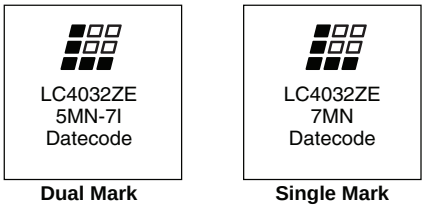
Note: ispMACH 4000ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

***Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages***




**Dual Mark** **Single Mark**

***Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages***




**Dual Mark** **Single Mark**

*Figure 20. Mark Format for 64 ucBGA and 132 ucBGA Packages*


**Dual Mark** **Single Mark**

## Lead-Free Packaging

**Commercial**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZE | LC4032ZE-4TN48C | 32 | 1.8 | 4.4 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-5TN48C | 32 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-7TN48C | 32 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-4MN64C | 32 | 1.8 | 4.4 | Lead-Free csBGA | 64 | 32 | C |
| | LC4032ZE-5MN64C | 32 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 32 | C |
| | LC4032ZE-7MN64C | 32 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 32 | C |
| LC4064ZE | LC4064ZE-4TN48C | 64 | 1.8 | 4.7 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-5TN48C | 64 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-7TN48C | 64 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-4TN100C | 64 | 1.8 | 4.7 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-5TN100C | 64 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-7TN100C | 64 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-4MN64C | 64 | 1.8 | 4.7 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-5MN64C | 64 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-7MN64C | 64 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-4MN144C | 64 | 1.8 | 4.7 | Lead-Free csBGA | 144 | 64 | C |
| | LC4064ZE-5MN144C | 64 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 64 | C |
| | LC4064ZE-7MN144C | 64 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 64 | C |
| LC4128ZE | LC4128ZE-5TN100C | 128 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4128ZE-7TN100C | 128 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4128ZE-5TN144C | 128 | 1.8 | 5.8 | Lead-Free TQFP | 144 | 96 | C |
| | LC4128ZE-7TN144C | 128 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | C |
| | LC4128ZE-5UMN132C | 128 | 1.8 | 5.8 | Lead-Free ucBGA | 132 | 96 | C |
| | LC4128ZE-7UMN132C | 128 | 1.8 | 7.5 | Lead-Free ucBGA | 132 | 96 | C |
| | LC4128ZE-5MN144C | 128 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 96 | C |
| | LC4128ZE-7MN144C | 128 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 96 | C |
| LC4256ZE | LC4256ZE-5TN100C | 256 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4256ZE-7TN100C | 256 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4256ZE-5TN144C | 256 | 1.8 | 5.8 | Lead-Free TQFP | 144 | 96 | C |
| | LC4256ZE-7TN144C | 256 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | C |
| | LC4256ZE-5MN144C | 256 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 108 | C |
| | LC4256ZE-7MN144C | 256 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 108 | C |

## Revision History

| Date | Version | Change Summary |
|---|---|---|
| April 2008 | 01.0 | Initial release. |
| July 2008 | 01.1 | Updated Features bullets. |
| | | Updated typical Hysteresis voltage. |
| | | Updated Power Guard for Dedicated Inputs section. |
| | | Updated DC Electrical Characteristics table. |
| | | Updated Supply Current table. |
| | | Updated I/O DC Electrical Characteristics table and note 2. |
| | | Updated ispMACH 4000ZE Timing Model. |
| | | Added new parameters for the Internal Oscillator. |
| | | Updated ORP Reference table. |
| | | Updated Power Supply and NC Connections table. |
| | | Updated 100 TQFP Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Updated 144 csBGA Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Added 144 TQFP Logic Signal Connections table. |
| August 2008 | 01.2 | Data sheet status changed from advance to final. |
| | | Updated Supply Current table. |
| | | Updated External Switching Characteristics. |
| | | Updated Internal Timing Parameters. |
| | | Updated Power Consumption graph and Power Estimation Coefficients table. |
| | | Updated Ordering Information mark format example. |
| December 2008 | 01.3 | Updated ispMACH 4000ZE Family Selection Guide table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated ispMACH 4000ZE Power Supply and NC Connections table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Added Logic Signal Connections tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Part Number Description diagram for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Ordering Information tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| May 2009 | 01.4 | Correction to $t_{CW}$, $t_{GW}$, $t_{WIR}$ and $f_{MAX}$ parameters in External Switching Characteristics table. |
| June 2011 | 01.5 | Added copper bond package part numbers. |
| | | Added footnote 4 to Absolute Maximum Ratings. |
| February 2012 | 01.6 | Updated document with new corporate logo. |
| February 2012 | 01.7 | Removed copper bond packaging information. Refer to PCN 04A-12 for further information. |
| | | Updated topside marks with new logos in the Ordering Information section. |