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Understanding <u>Embedded - CPLDs (Complex Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	-
Number of I/O	48
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-VFBGA, CSPBGA
Supplier Device Package	64-UCBGA (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4064ze-7umn64i

The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTL and PCI interfaces.

Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block
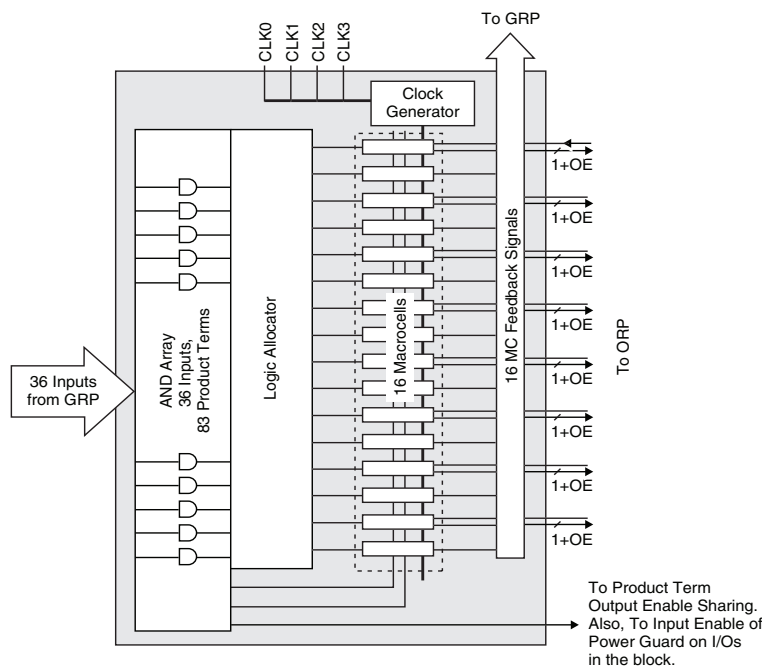
AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array

Note:
⊗ Indicates programmable fuse.
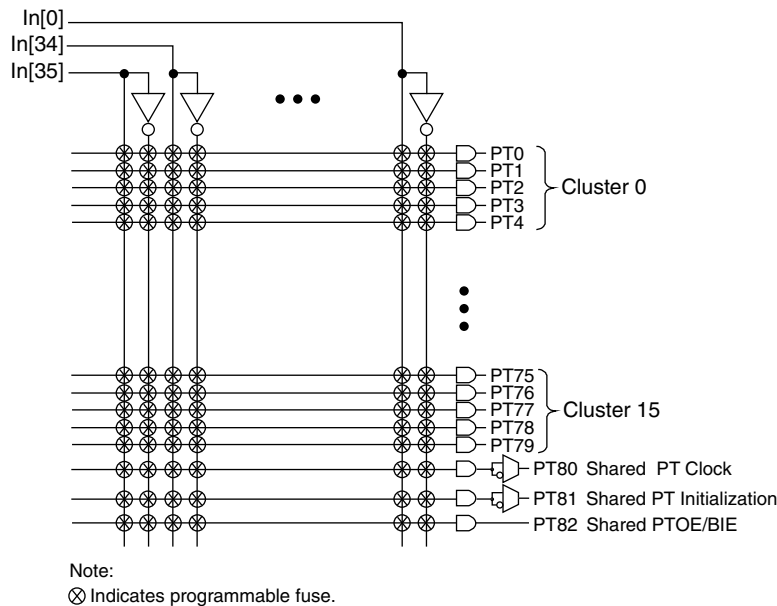
Enhanced Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.
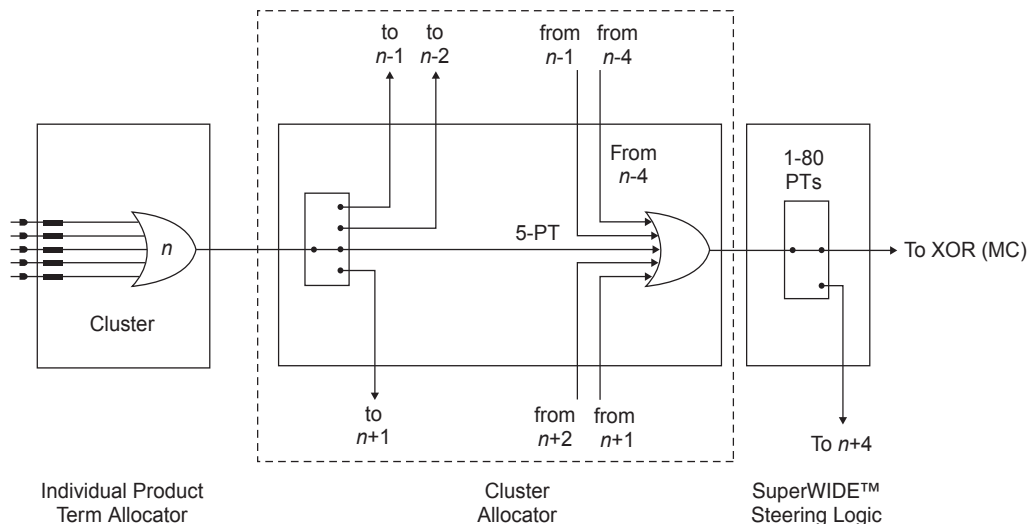
Figure 4. Macrocell Slice

Table 4. Product Term Expansion Capability

Expansion Chains	Macrocells Associated with Expansion Chain (with Wrap Around)	Max PT/ Macrocell
Chain-0	M0 Õ M4 Õ M8 Õ M12 Õ M0	75
Chain-1	M1 Õ M5 Õ M9 Õ M13 Õ M1	80
Chain-2	M2 Õ M6 Õ M10 Õ M14 Õ M2	75
Chain-3	M3 Õ M7 Õ M11 Õ M15 Õ M3	70

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP}. When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell
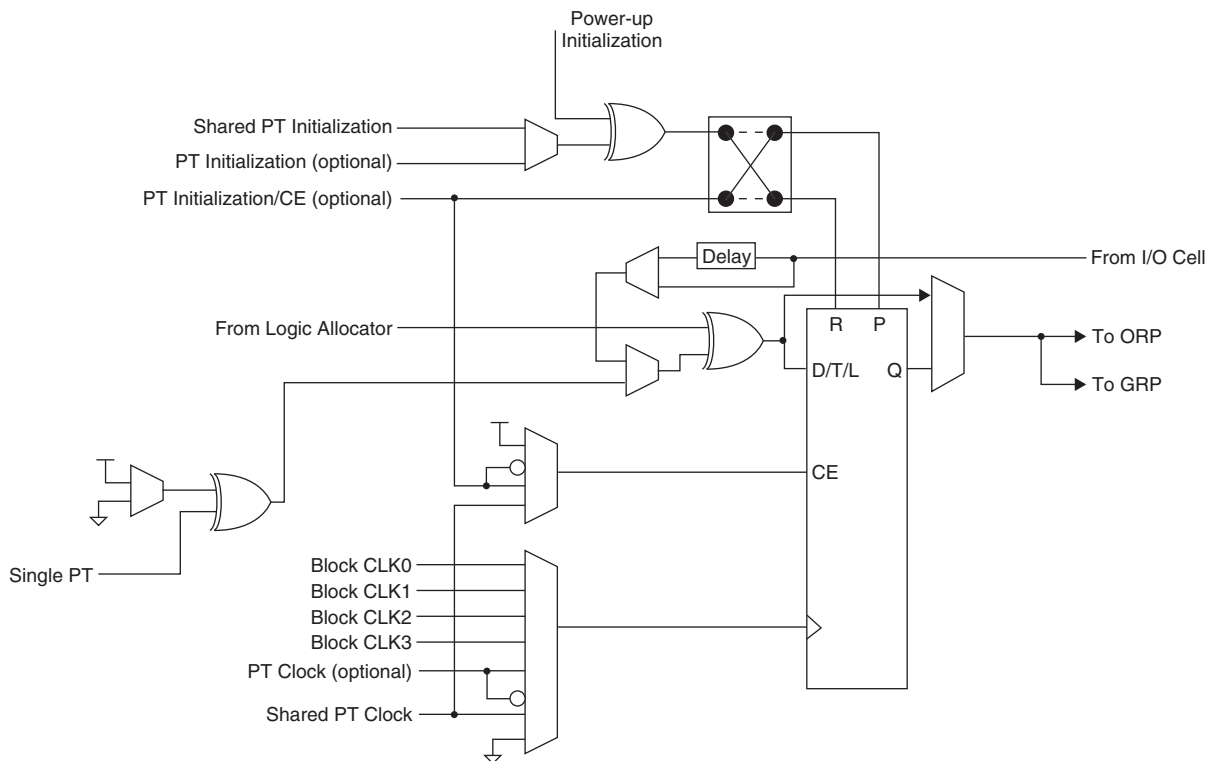
Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

The ispMACH 4000ZE family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be "stolen" from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000ZE device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator
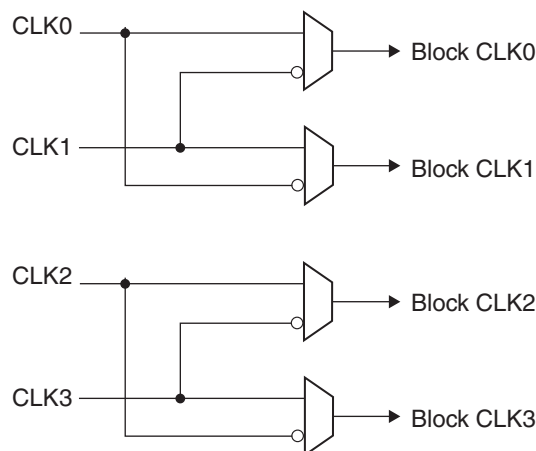
Figure 9. Power Guard
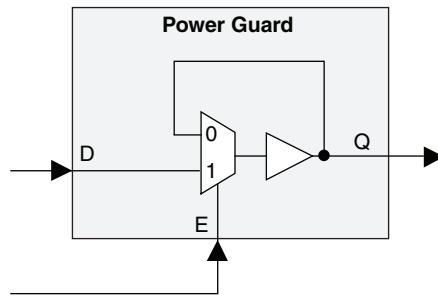
All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os
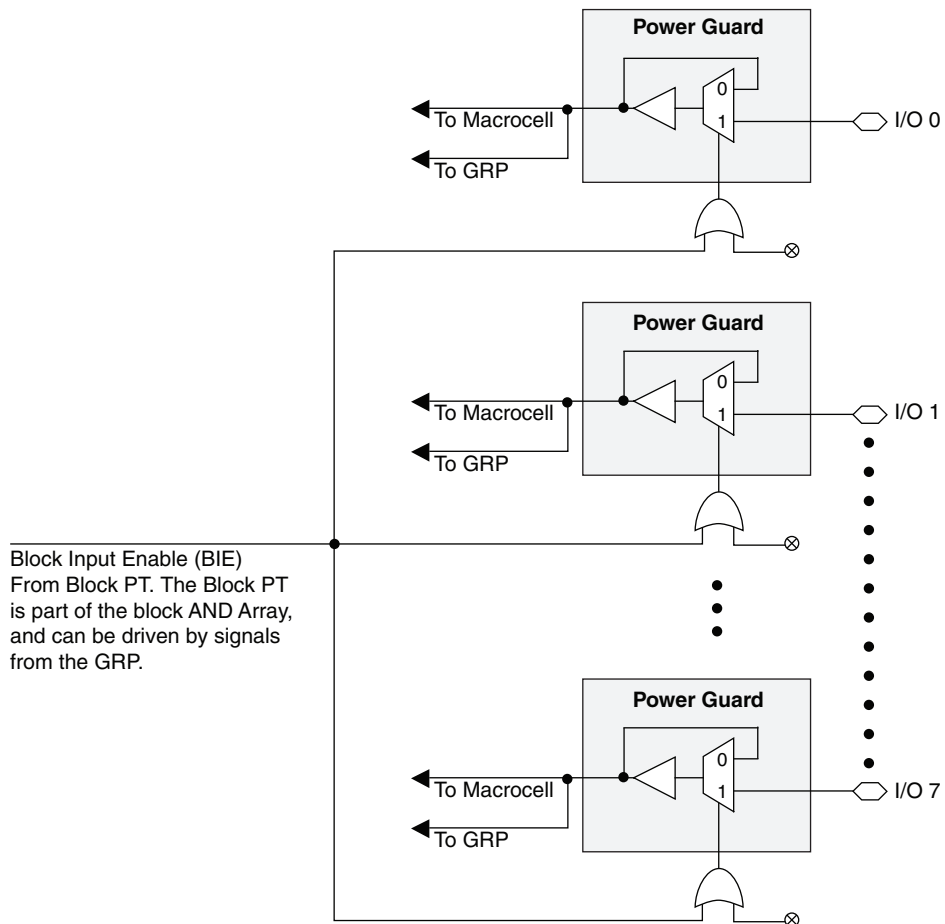
The number of BIE inputs, thus the number of Power Guard "Blocks" that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, …, H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, …, P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, [Advanced Features of the ispMACH 4000ZE Family](#).

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

Some Simple Use Scenarios

The following diagrams show a few simple examples that omit optional signals for the OSCTIMER block:

A. An oscillator giving 5MHz nominal clock

B. An oscillator that can be disabled with an external signal (5MHz nominal clock)

C. An oscillator giving approximately 5 Hz nominal clock (TIMER_DIV = 2^{20} (1,048,576))

D. An oscillator giving two output clocks: ~5MHz and ~5KHz (TIMER_DIV= 2^{10} (1,024))

OSCTIMER
TIMER_DIV= N/A — OSCOUT
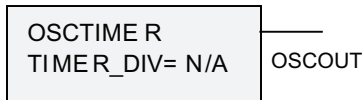
(A) A simple 5MHz oscillator.

DYNOSCDIS — OSCTIMER
TIMER_DIV= N/A — OSCOUT
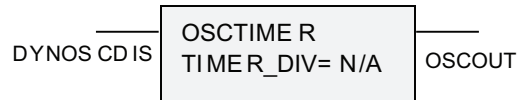
(B) An oscillator with dynamic disable.

OSCTIMER
TIMER_DIV= 2^{20} — TIMEROUT
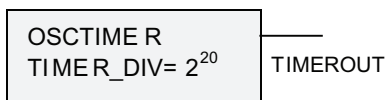
(C) A simple 5Hz oscillator.

OSCTIMER
TIMER_DIV= 2^{10} — OSCOUT / TIMEROUT
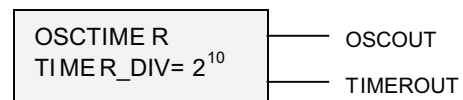
(D) Oscillator with two outputs (5MHz and 5KHz).

OSCTIMER Integration With CPLD Fabric

The OSCTIMER is integrated into the CPLD fabric using the Global Routing Pool (GRP). The macrocell (MC) feedback path for two macrocells is augmented with a programmable multiplexer, as shown in Figure 15. The OSC-TIMER outputs (OSCOUT and TIMEROUT) can optionally drive the GRP lines, whereas the macrocell outputs can drive the optional OSCTIMER inputs TIMERRES and DYNOSCDIS.

Figure 15. OSCTIMER Integration With CPLD Fabric

A Regular Macrocell
To GRP — Macrocell Feedback Signal

OSC Macrocell
To GRP — Macrocell 15 Feedback Signal
OSCOUT   DYNOSCDIS

TIMER Macrocell
To GRP — Macrocell 15 Feedback Signal
TIMEROUT   TIMERRES
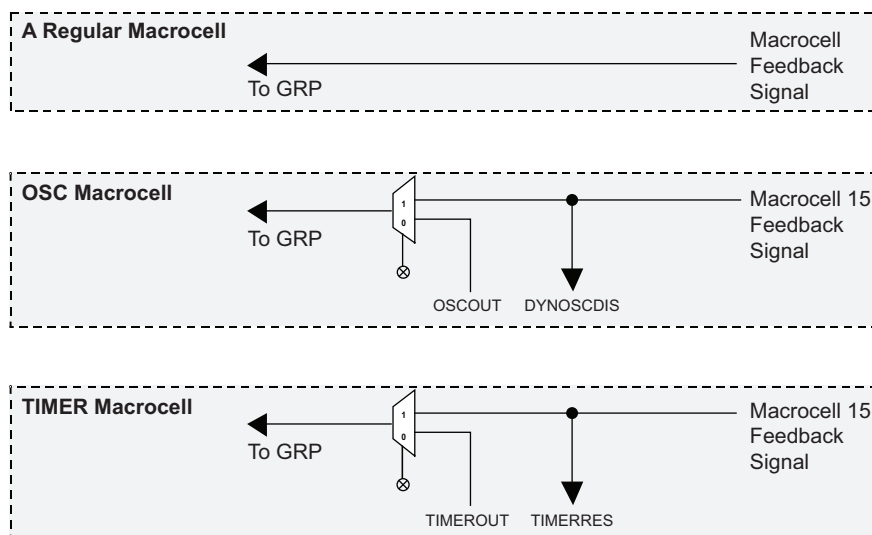
Table 12 shows how these two MCs are designated in each of the ispMACH4000ZE device.

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . -0.5 to 5.5V

Storage Temperature . . . . -65 to 150°C

Junction Temperature (T_j) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and $V_{CCO,}$ provided (V_{IN} - V_{CCO}) $\leq$ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines.

Figure 16. ispMACH 4000ZE Timing Model

Note: Italicized items are optional delay adders.
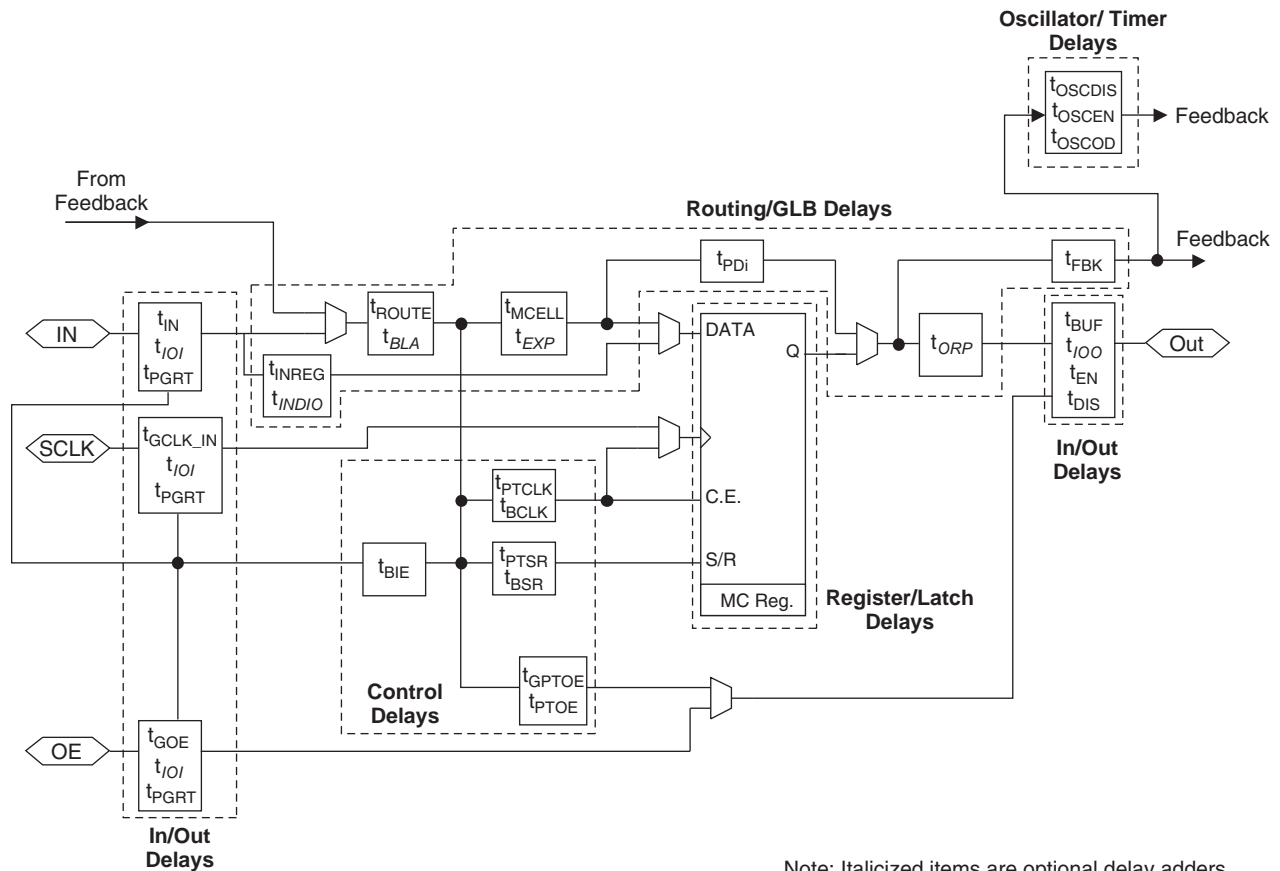
ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5 Min.	-5 Max.	-7 Min.	-7 Max.	Units
In/Out Delays						
t_{IN}	Input Buffer Delay	—	1.05	—	1.90	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	1.95	—	2.15	ns
t_{GOE}	Global OE Pin Delay	—	3.00	—	4.30	ns
t_{BUF}	Delay through Output Buffer	—	1.10	—	1.30	ns
t_{EN}	Output Enable Time	—	2.50	—	2.70	ns
t_{DIS}	Output Disable Time	—	2.50	—	2.70	ns
t_{PGSU}	Input Power Guard Setup Time	—	4.30	—	5.60	ns
t_{PGH}	Input Power Guard Hold Time	—	0.00	—	0.00	ns
t_{PGPW}	Input Power Guard BIE Minimum Pulse Width	—	6.00	—	8.00	ns
t_{PGRT}	Input Power Guard Recovery Time Following BIE Dissertation	—	5.00	—	7.00	ns
Routing Delays						
t_{ROUTE}	Delay through GRP	—	2.25	—	2.50	ns
t_{PDi}	Macrocell Propagation Delay	—	0.45	—	0.50	ns
t_{MCELL}	Macrocell Delay	—	0.65	—	1.00	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	ns
t_{FBK}	Internal Feedback Delay	—	0.75	—	0.30	ns
t_{ORP}	Output Routing Pool Delay	—	0.30	—	0.30	ns
Register/Latch Delays						
t_S	D-Register Setup Time (Global Clock)	0.90	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time (Product Term Clock)	2.00	—	2.35	—	ns
t_H	D-Register Hold Time	2.00	—	3.25	—	ns
t_{ST}	T-Register Setup Time (Global Clock)	1.10	—	1.45	—	ns
t_{ST_PT}	T-register Setup Time (Product Term Clock)	2.20	—	2.65	—	ns
t_{HT}	T-Resister Hold Time	2.00	—	3.25	—	ns
t_{SIR}	D-Input Register Setup Time (Global Clock)	1.20	—	0.65	—	ns
t_{SIR_PT}	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
t_{HIR}	D-Input Register Hold Time (Global Clock)	1.40	—	2.05	—	ns
t_{HIR_PT}	D-Input Register Hold Time (Product Term Clock)	1.10	—	1.20	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	0.45	—	0.75	ns
t_{CES}	Clock Enable Setup Time	2.00	—	2.00	—	ns
t_{CEH}	Clock Enable Hold Time	0.00	—	0.00	—	ns
t_{SL}	Latch Setup Time (Global Clock)	0.90	—	1.55	—	ns
t_{SL_PT}	Latch Setup Time (Product Term Clock)	2.00	—	2.05	—	ns
t_{HL}	Latch Hold Time	2.00	—	1.17	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	0.35	—	0.33	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	0.25	—	0.25	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.95	—	0.28	ns

Signal Descriptions

Signal Names	Description	
TMS	Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.	
TCK	Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.	
TDI	Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.	
TDO	Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.	
GOE0/IO, GOE1/IO	These pins are configured to be either Global Output Enable Input or as general I/O pins.	
GND	Ground	
NC	Not Connected	
V_{CC}	The power supply pins for logic core and JTAG port.	
CLK0/I, CLK1/I, CLK2/I, CLK3/I	These pins are configured to be either CLK input or as an input.	
V_{CCO0}, V_{CCO1}	The power supply pins for each I/O bank.	
yzz	Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.	
	ispMACH 4032ZE	y: A-B
	ispMACH 4064ZE	y: A-D
	ispMACH 4128ZE	y: A-H
	ispMACH 4256ZE	y: A-P

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032ZE GLB/MC/Pad	ispMACH 4064ZE GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
A1	-	TDI
B1	0	A8
B2	0	A10
B3	0	A11
GND*	0	GND (Bank 0)
C1	0	A12
C3	0	VCCO (Bank 0)
C2	0	B15
D1	0	B14
D2	0	B13
D3	0	B12
E1	0	B11
E2	0	B10
E3	0	B9
F1	0	B8
F2	-	TCK
E4	-	VCC
GND*	-	GND
H2	0	B6
H1	0	B5
G1	0	B4
GND*	0	GND (Bank 0)
F3	0	VCCO (Bank 0)
G2	0	B3
G3	0	B2
H3	0	B0
G4	0	CLK1/I
F4	1	CLK2/I
H4	1	C0
H5	1	C1
G5	1	C2
H6	1	C4
H7	1	C5
H8	1	C6
G8	-	TMS
G7	1	C8
G6	1	C10
F8	1	C11
GND*	1	GND (Bank 1)
F7	1	C12
F6	1	VCCO (Bank 1)
F5	1	D15
E8	1	D14

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE GLB/MC/Pad	LC4128ZE GLB/MC/Pad	LC4256ZE GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

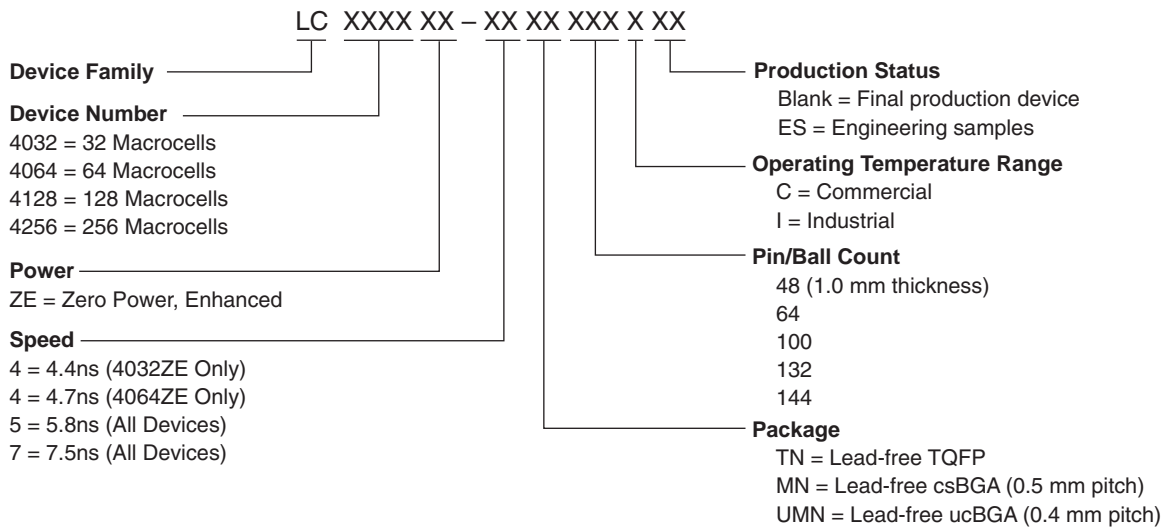| Pin Number	Bank Number	LC4064ZE GLB/MC/Pad	LC4128ZE GLB/MC/Pad	LC4256ZE GLB/MC/Pad
83	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
84	1	D3	H6	P12
85	1	D2	H4	P10
86	1	D1	H2	P6
87	1	D0/GOE1	H0/GOE1	P2/GOE1
88	1	CLK3/I	CLK3/I	CLK3/I
89	0	CLK0/I	CLK0/I	CLK0/I
90	-	VCC	VCC	VCC
91	0	A0/GOE0	A0/GOE0	A2/GOE0
92	0	A1	A2	A6
93	0	A2	A4	A10
94	0	A3	A6	A12
95	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
96	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
97	0	A4	A8	B2
98	0	A5	A10	B6
99	0	A6	A12	B10
100	0	A7	A14	B12

* This pin is input only.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE GLB/MC/Pad	LC4128ZE GLB/MC/Pad	LC4256ZE GLB/MC/Pad
J12	1	NC Ball	NC Ball	L14
J11	1	NC Ball	NC Ball	L12
H10	1	NC Ball	F8	L10
H12	1	C12	F9	L8
G11	1	C13	F10	L6
H11	1	C14	F12	L4
G12	1	C15	F13	L2
G10*	1	I	F14	L0
G9	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
F12	1	D15	G14	M0
F11	1	D14	G13	M2
E11	1	D13	G12	M4
E12	1	D12	G10	M6
D10	1	NC Ball	G9	M8
F10	1	NC Ball	G8	M10
D12	1	NC Ball	NC Ball	M12
F8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
E10	1	D11	G6	N2
D11	1	D10	G5	N4
E9	1	D9	G4	N6
C12	1	D8	G2	N8
C11*	1	I	G1	N10
B12	1	NC Ball	G0	N12
F9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
B11	-	TDO	TDO	TDO
E8	-	VCC	VCC	VCC
F7	-	GND	GND	GND
A12	1	NC Ball	NC Ball	O14
C10	1	NC Ball	NC Ball	O12
B10	1	NC Ball	H14	O10
A11*	1	I	H13	O8
D9	1	D7	H12	O6
B9	1	D6	H10	O4
C9	1	D5	H9	O2
A10	1	D4	H8	O0
E7	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
D8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
A9	1	NC Ball	H6	P12
B8	1	NC Ball	H5	P10
C8	1	D3	H4	P8
A8	1	D2	H2	P6
D7	1	D1	H1	P4
B7	1	D0/GOE1	H0/GOE1	P2/GOE1

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

Pin Number	Bank Number	LC4128ZE GLB/MC/Pad	LC4256ZE GLB/MC/Pad
1	-	GND	GND
2	-	TDI	TDI
3	0	VCCO (Bank 0)	VCCO (Bank 0)
4	0	B0	C12
5	0	B1	C10
6	0	B2	C8
7	0	B4	C6
8	0	B5	C4
9	0	B6	C2
10	0	GND (Bank 0)	GND (Bank 0)
11	0	B8	D14
12	0	B9	D12
13	0	B10	D10
14	0	B12	D8
15	0	B13	D6
16	0	B14	D4
17*	0	NC	I
18	0	GND (Bank 0)	NC
19	0	VCCO (Bank 0)	VCCO (Bank 0)
20*	0	NC	I
21	0	C14	E2
22	0	C13	E4
23	0	C12	E6
24	0	C10	E8
25	0	C9	E10
26	0	C8	E12
27	0	GND (Bank 0)	GND (Bank 0)
28	0	C6	F2
29	0	C5	F4
30	0	C4	F6
31	0	C2	F8
32	0	C1	F10
33	0	C0	F12
34	0	VCCO (Bank 0)	VCCO (Bank 0)
35	-	TCK	TCK
36	-	VCC	VCC
37	-	GND	GND
38*	0	NC	I
39	0	D14	G12
40	0	D13	G10
41	0	D12	G8
42	0	D10	G6

Part Number Description

LC XXXX XX – XX XX XXX X XX

Device Family

Device Number
4032 = 32 Macrocells
4064 = 64 Macrocells
4128 = 128 Macrocells
4256 = 256 Macrocells

Power
ZE = Zero Power, Enhanced

Speed
4 = 4.4ns (4032ZE Only)
4 = 4.7ns (4064ZE Only)
5 = 5.8ns (All Devices)
7 = 7.5ns (All Devices)

Production Status
Blank = Final production device
ES = Engineering samples

Operating Temperature Range
C = Commercial
I = Industrial

Pin/Ball Count
48 (1.0 mm thickness)
64
100
132
144

Package
TN = Lead-free TQFP
MN = Lead-free csBGA (0.5 mm pitch)
UMN = Lead-free ucBGA (0.4 mm pitch)

ispMACH 4000ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

Ordering Information

Note: ispMACH 4000ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

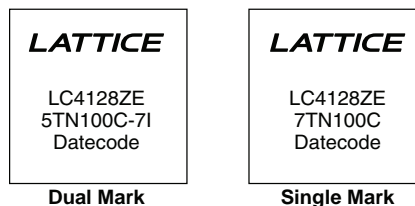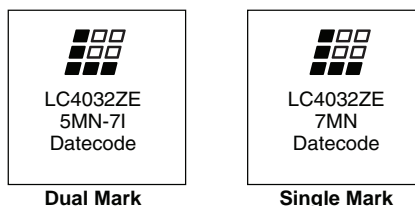*Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages*

LATTICE
LC4128ZE
5TN100C-7I
Datecode

Dual Mark

LATTICE
LC4128ZE
7TN100C
Datecode

Single Mark

Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages

LC4032ZE
5MN-7I
Datecode

Dual Mark

LC4032ZE
7MN
Datecode

Single Mark

Industrial

Device	Part Number	Macrocells	Voltage	t_{PD}	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
	LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

Technical Support Assistance

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