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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

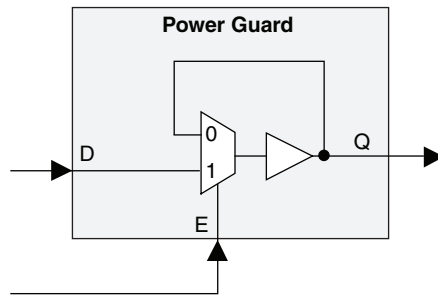
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	96
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128ze-5tn144c

Figure 9. Power Guard

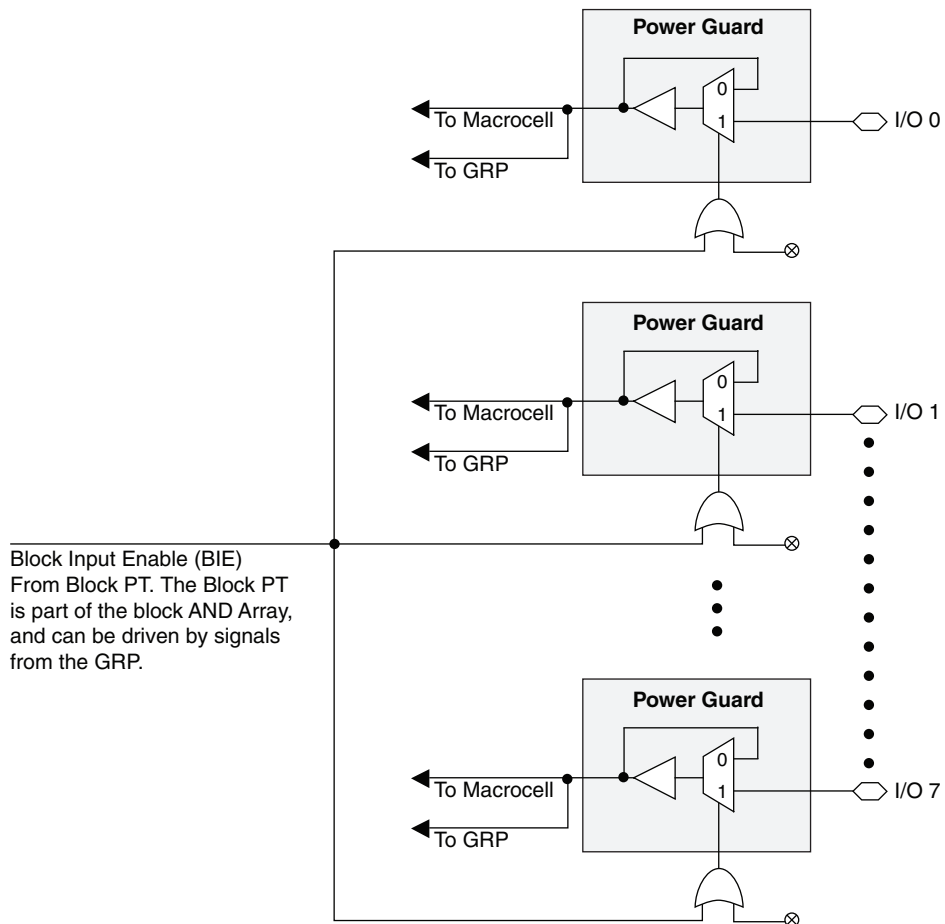


All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os



The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, ..., H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, ..., P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, [Advanced Features of the ispMACH 4000ZE Family](#).

Global OE (GOE) and Block Input Enable (BIE) Generation

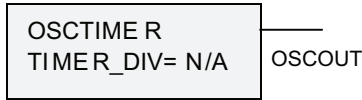
Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

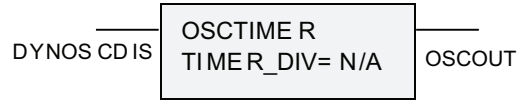
Some Simple Use Scenarios

The following diagrams show a few simple examples that omit optional signals for the OSCTIMER block:

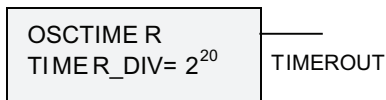
- A. An oscillator giving 5MHz nominal clock
- B. An oscillator that can be disabled with an external signal (5MHz nominal clock)
- C. An oscillator giving approximately 5 Hz nominal clock (TIMER_DIV = 2^{20} (1,048,576))
- D. An oscillator giving two output clocks: ~5MHz and ~5KHz (TIMER_DIV = 2^{10} (1,024))



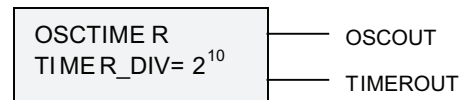
(A) A simple 5MHz oscillator.



(B) An oscillator with dynamic disable.



(C) A simple 5Hz oscillator.



(D) Oscillator with two outputs (5MHz and 5KHz).

OSCTIMER Integration With CPLD Fabric

The OSCTIMER is integrated into the CPLD fabric using the Global Routing Pool (GRP). The macrocell (MC) feedback path for two macrocells is augmented with a programmable multiplexer, as shown in Figure 15. The OSCTIMER outputs (OSCOUT and TIMEROUT) can optionally drive the GRP lines, whereas the macrocell outputs can drive the optional OSCTIMER inputs TIMERRES and DYNOSCDIS.

Figure 15. OSCTIMER Integration With CPLD Fabric

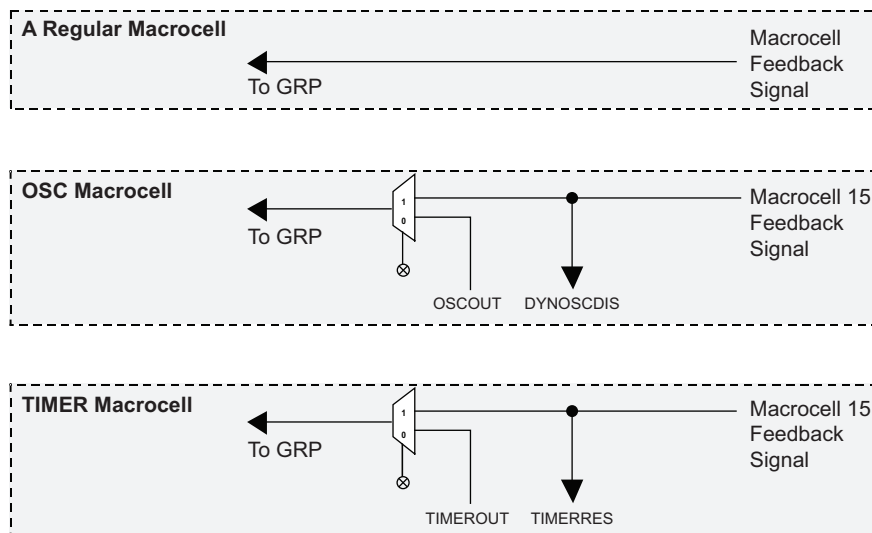


Table 12 shows how these two MCs are designated in each of the ispMACH4000ZE device.

Table 12. OSC and TIMER MC Designation

Device	Macrocell	Block Number	MC Number
ispMACH 4032ZE	OSC MC	A	15
	TIMER MC	B	15
ispMACH 4064ZE	OSC MC	A	15
	TIMER MC	D	15
ispMACH 4128ZE	OSC MC	A	15
	TIMER MC	G	15
ispMACH 4256ZE	OSC MC	C	15
	TIMER MC	F	15

Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E² low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

Absolute Maximum Ratings^{1, 2, 3, 4}

Supply Voltage (V_{CC}) -0.5 to 2.5V
 Output Supply Voltage (V_{CCO}) -0.5 to 4.5V
 Input or I/O Tristate Voltage Applied^{5, 6} -0.5 to 5.5V
 Storage Temperature -65 to 150°C
 Junction Temperature (T_j) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Please refer to the [Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary](#) for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6 ¹	1.9	V
T_j	Junction Temperature (Commercial)	0	90	°C	
	Junction Temperature (Industrial)	-40	105	°C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics^{1,2,3}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
2. $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$.
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH} . Device defaults to pull-up until fuse circuitry is active.

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	LC4032ZE		LC4064ZE		Units	
		-4		-4			
		Min.	Max.	Min.	Max.		
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	2.00	—	1.70	ns	
Control Delays							
t _{BCLK}	GLB PT Clock Delay	—	1.20	—	1.30	ns	
t _{PTCLK}	Macrocell PT Clock Delay	—	1.40	—	1.50	ns	
t _{BSR}	Block PT Set/Reset Delay	—	1.10	—	1.85	ns	
t _{PTSR}	Macrocell PT Set/Reset Delay	—	1.20	—	1.90	ns	
t _{BIE}	Power Guard Block Input Enable Delay	—	1.60	—	1.70	ns	
t _{P_{TOE}}	Macrocell PT OE Delay	—	2.30	—	3.15	ns	
t _{GPTOE}	Global PT OE Delay	—	1.80	—	2.15	ns	
Internal Oscillator							
t _{O_{SCSU}}	Oscillator DYNOSCDIS Setup Time	5.00	—	5.00	—	ns	
t _{O_{SCH}}	Oscillator DYNOSCDIS Hold Time	5.00	—	5.00	—	ns	
t _{O_{SCEN}}	Oscillator OSCOUT Enable Time (To Stable)	—	5.00	—	5.00	ns	
t _{O_{SCOD}}	Oscillator Output Delay	—	4.00	—	4.00	ns	
t _{O_{SCNOM}}	Oscillator OSCOUT Nominal Frequency	—	5.00	—	5.00	MHz	
t _{O_{SCvar}}	Oscillator Variation of Nominal Frequency	—	30	—	30	%	
t _{T_{MRCO20}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)	—	12.50	—	12.50	ns	
t _{T_{MRCO10}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)	—	7.50	—	7.50	ns	
t _{T_{MRCO7}}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)	—	6.00	—	6.00	ns	
t _{T_{MRRSTO}}	Oscillator TIMEROUT Reset to Out (Going Low)	—	5.00	—	5.00	ns	
t _{T_{MRRR}}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay	—	4.00	—	4.00	ns	
t _{T_{MRRSTPW}}	Oscillator TIMEROUT Reset Minimum Pulse Width	3.00	—	3.00	—	ns	
Optional Delay Adjusters		Base Parameter					
t _{I_{NDIO}}	Input Register Delay	t _{I_{NREG}}	—	1.00	—	1.00	ns
t _{E_{XP}}	Product Term Expander Delay	t _{M_{CELL}}	—	0.40	—	0.40	ns
t _{B_{LA}}	Additional Block Loading Adders	t _{R_{ROUTE}}	—	0.04	—	0.05	ns
t_{I_{OI}} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.60	—	0.60	ns
LVC _{MOS15_in}	Using LVC _{MOS} 1.5 Standard	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.20	—	0.20	ns
LVC _{MOS18_in}	Using LVC _{MOS} 1.8 Standard	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.00	—	0.00	ns
LVC _{MOS25_in}	Using LVC _{MOS} 2.5 Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
LVC _{MOS33_in}	Using LVC _{MOS} 3.3 Standard with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}}	—	0.80	—	0.80	ns
t_{I_{OO}} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t _{E_N} , t _{D_{IS}} , t _{B_{UF}}	—	0.20	—	0.20	ns

ispMACH 4000ZE Power Supply and NC Connections¹ (Cont.)

Signal	132 ucBGA ³	144 csBGA ³	144 TQFP ²
VCC	M1, M7, A12, B5	H5, H8, E8, E5	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	B1, H4, L2, J5, A4	E4, F4, G4, J5, D5	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	K9, L12, F12, D9, C7	J8, H9, G9, F9, D8	64, 75, 91, 106, 119
GND	E5, E8, H5, H8	F6, G6, G7, F7	1, 37, 73, 109
GND (Bank 0)	E2, H2, M4, B7, B3	G5, H4, H6, E6, F5	10, 18 ⁴ , 27, 46, 127, 137
GND (Bank 1)	L7, J9, H12, E9, A9	H7, J9, G8, F8, E7	55, 65, 82, 90 ⁴ , 99, 118
NC	—	4064ZE: E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 4128ZE: D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2	4128ZE: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 4256ZE: 18, 90

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND	GND
2	-	TDI	TDI	TDI
3	0	A8	B0	C12
4	0	A9	B2	C10
5	0	A10	B4	C6
6	0	A11	B6	C2
7	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
8	0	A12	B8	D12
9	0	A13	B10	D10
10	0	A14	B12	D6
11	0	A15	B13	D4
12*	0	I	I	I
13	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
14	0	B15	C14	E4
15	0	B14	C12	E6
16	0	B13	C10	E10
17	0	B12	C8	E12
18	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
19	0	B11	C6	F2
20	0	B10	C5	F6
21	0	B9	C4	F10
22	0	B8	C2	F12
23*	0	I	I	I
24	-	TCK	TCK	TCK
25	-	VCC	VCC	VCC
26	-	GND	GND	GND
27*	0	I	I	I
28	0	B7	D13	G12
29	0	B6	D12	G10
30	0	B5	D10	G6
31	0	B4	D8	G2
32	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
33	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
34	0	B3	D6	H12
35	0	B2	D4	H10
36	0	B1	D2	H6
37	0	B0	D0	H2
38	0	CLK1/I	CLK1/I	CLK1/I
39	1	CLK2/I	CLK2/I	CLK2/I
40	-	VCC	VCC	VCC
41	1	C0	E0	I2

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP (Cont.)**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
A2	0	A14

* All bonded core grounds are connected to the following four balls, E5, E8, H5 and H8.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
144 csBGA**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
F6	-	GND	GND	GND
A1	-	TDI	TDI	TDI
E4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
B2	0	NC Ball	B0	C12
B1	0	NC Ball	B1	C10
C3	0	A8	B2	C8
C2	0	A9	B4	C6
C1	0	A10	B5	C4
D1	0	A11	B6	C2
G5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
D2	0	NC Ball	NC Ball	D14
D3	0	NC Ball	NC Ball	D12
E1	0	NC Ball	B8	D10
E2	0	A12	B9	D8
F2	0	A13	B10	D6
D4	0	A14	B12	D4
F1	0	A15	B13	D2
F3*	0	I	B14	D0
F4	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
G1	0	B15	C14	E0
E3	0	B14	C13	E2
G2	0	B13	C12	E4
G3	0	B12	C10	E6
H1	0	NC Ball	C9	E8
H3	0	NC Ball	C8	E10
H2	0	NC Ball	NC Ball	E12
H4	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J1	0	B11	C6	F2
J3	0	B10	C5	F4
J2	0	B9	C4	F6
K1	0	B8	C2	F8
K2*	0	I	C1	F10
L1	0	NC Ball	C0	F12
G4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
L2	-	TCK	TCK	TCK
H5	-	VCC	VCC	VCC
G6	-	GND	GND	GND
M1	0	NC Ball	NC Ball	G14
K3	0	NC Ball	NC Ball	G12
M2	0	NC Ball	D14	G10
L3*	0	I	D13	G8

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
 144 csBGA (Cont.)**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND
2	-	TDI	TDI
3	0	VCCO (Bank 0)	VCCO (Bank 0)
4	0	B0	C12
5	0	B1	C10
6	0	B2	C8
7	0	B4	C6
8	0	B5	C4
9	0	B6	C2
10	0	GND (Bank 0)	GND (Bank 0)
11	0	B8	D14
12	0	B9	D12
13	0	B10	D10
14	0	B12	D8
15	0	B13	D6
16	0	B14	D4
17*	0	NC	I
18	0	GND (Bank 0)	NC
19	0	VCCO (Bank 0)	VCCO (Bank 0)
20*	0	NC	I
21	0	C14	E2
22	0	C13	E4
23	0	C12	E6
24	0	C10	E8
25	0	C9	E10
26	0	C8	E12
27	0	GND (Bank 0)	GND (Bank 0)
28	0	C6	F2
29	0	C5	F4
30	0	C4	F6
31	0	C2	F8
32	0	C1	F10
33	0	C0	F12
34	0	VCCO (Bank 0)	VCCO (Bank 0)
35	-	TCK	TCK
36	-	VCC	VCC
37	-	GND	GND
38*	0	NC	I
39	0	D14	G12
40	0	D13	G10
41	0	D12	G8
42	0	D10	G6

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

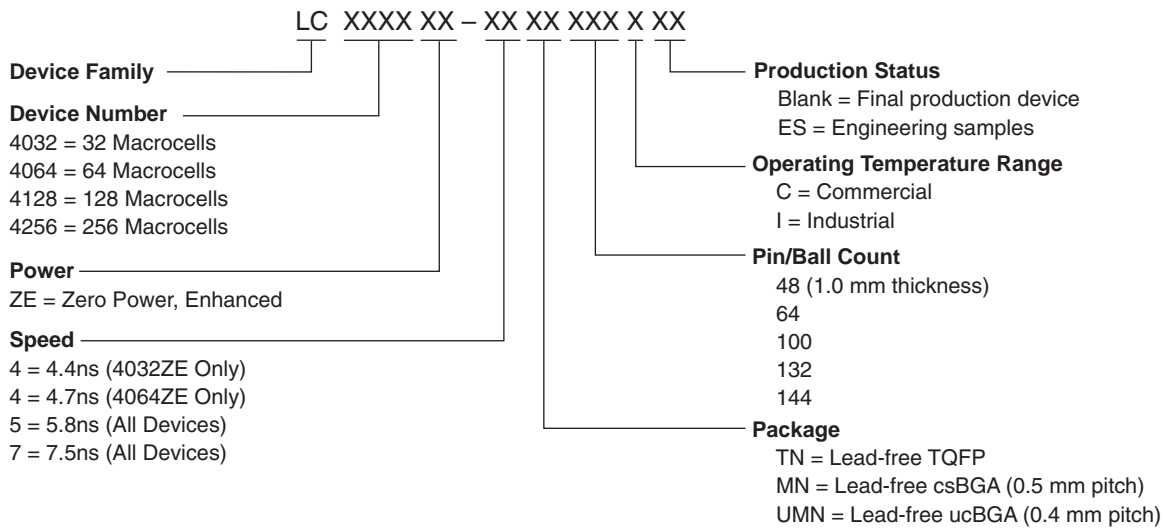
Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
86	1	F12	L8
87	1	F13	L6
88	1	F14	L4
89*	1	NC	I
90	1	GND (Bank 1)	NC
91	1	VCCO (Bank 1)	VCCO (Bank 1)
92*	1	NC	I
93	1	G14	M2
94	1	G13	M4
95	1	G12	M6
96	1	G10	M8
97	1	G9	M10
98	1	G8	M12
99	1	GND (Bank 1)	GND (Bank 1)
100	1	G6	N2
101	1	G5	N4
102	1	G4	N6
103	1	G2	N8
104	1	G1	N10
105	1	G0	N12
106	1	VCCO (Bank 1)	VCCO (Bank 1)
107	-	TDO	TDO
108	-	VCC	VCC
109	-	GND	GND
110*	1	NC	I
111	1	H14	O12
112	1	H13	O10
113	1	H12	O8
114	1	H10	O6
115	1	H9	O4
116	1	H8	O2
117*	1	NC	I
118	1	GND (Bank 1)	GND (Bank 1)
119	1	VCCO (Bank 1)	VCCO (Bank 1)
120	1	H6	P12
121	1	H5	P10
122	1	H4	P8
123	1	H2	P6
124	1	H1	P4
125	1	H0/GOE1	P2/GOE1
126	1	CLK3/I	CLK3/I
127	0	GND (Bank 0)	GND (Bank 0)
128	0	CLK0/I	CLK0/I

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.

Part Number Description



ispMACH 400ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

Ordering Information

Note: ispMACH 400ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages

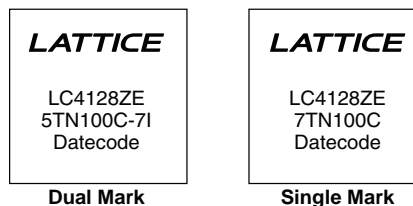


Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages

