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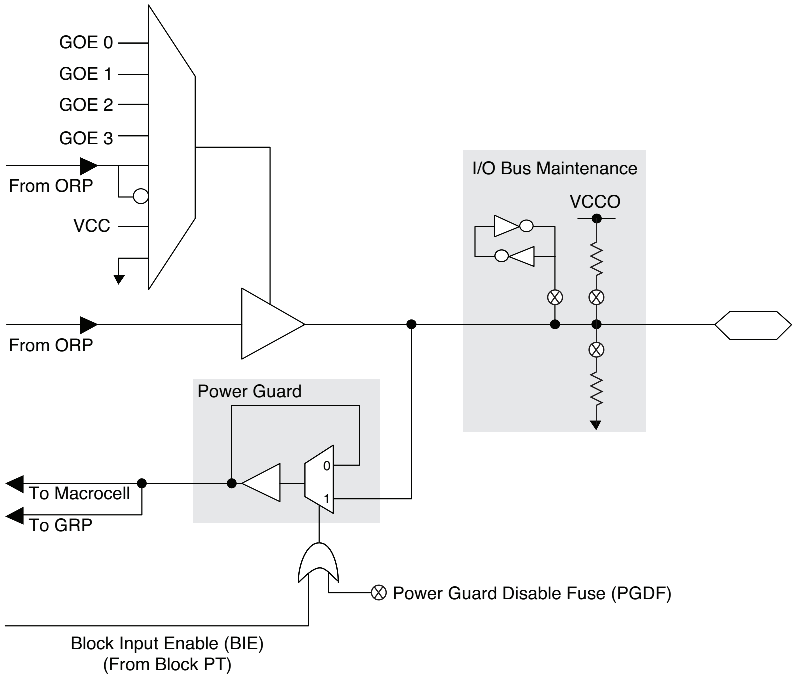
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128ze-7tcn100c

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a “per-pin” basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, …, H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, …, P)

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

Table 10. Dedicated Inputs to BIE Association

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, Advanced Features of the ispMACH 4000ZE Family.

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macro-cell device (with 16 blocks), each block's BIE signal is driven by block-level OE PT from each block.

Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE

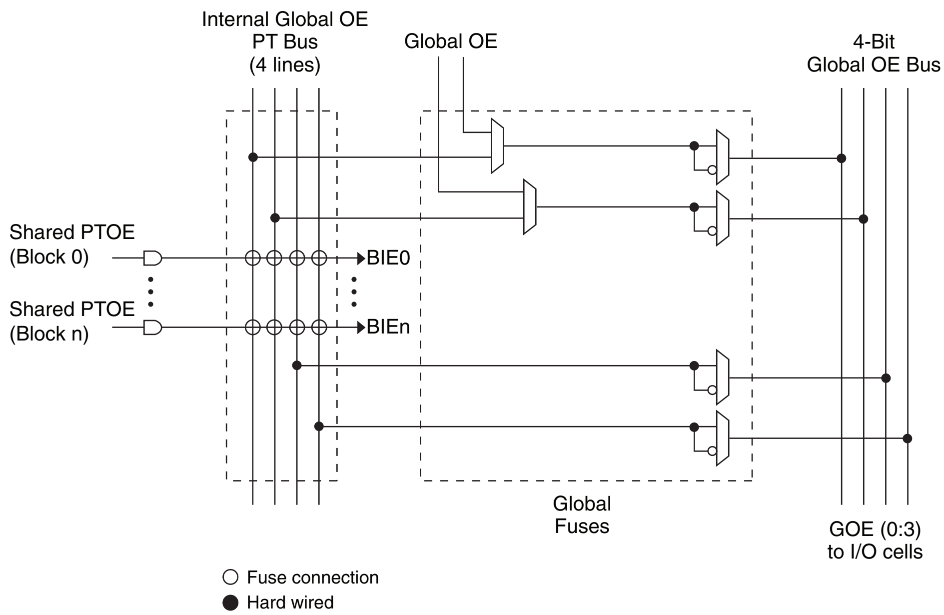
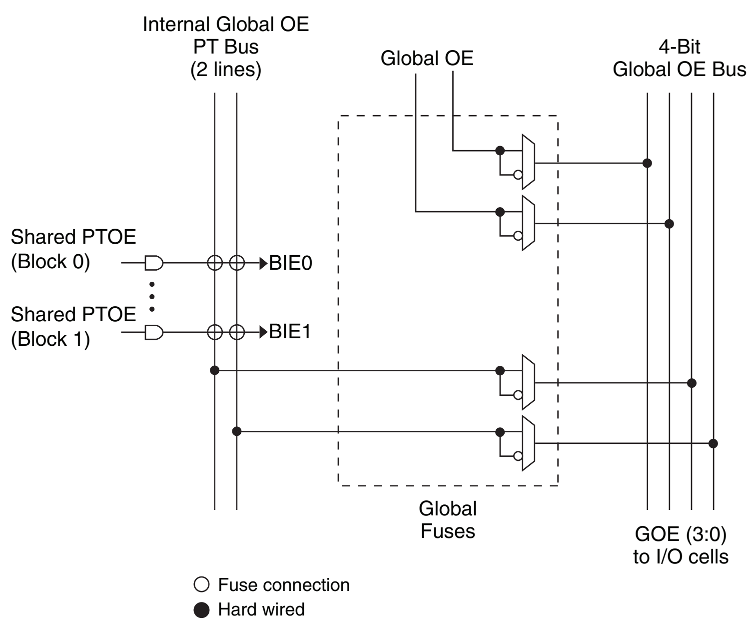


Figure 12. Global OE Generation for ispMACH 4032ZE



On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

Figure 13. On-Chip Oscillator and Timer

Table 11. On-Chip Oscillator and Timer Signal Names

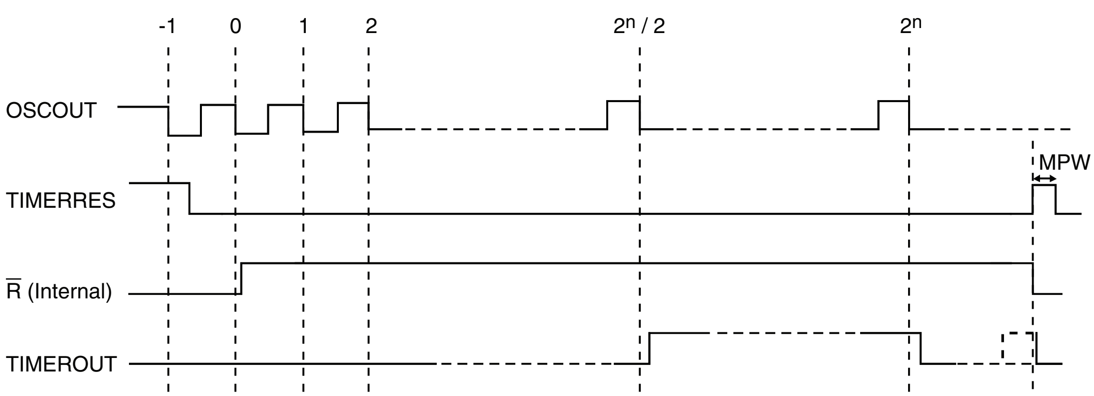
Signal Name	Input or Output	Optional / Required	Description
OSCOUT	Output	Optional	Oscillator Output (Nominal Frequency: 5MHz)
TIMEROUT	Output	Optional	Oscillator Frequency Divided by an integer TIMER_DIV (Default 128)
TIMERRES	Input	Optional	Reset the Timer
DYNOSCDIS	Input	Optional	Disables the Oscillator, resets the Timer and saves the power.

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER_DIV.

The attribute TIMER_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal "$\overline{R}$" is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT



Note: n = Number of bits in the divider (7, 10 or 20)
Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

Table 12. OSC and TIMER MC Designation

Device	Macrocell	Block Number	MC Number
ispMACH 4032ZE	OSC MC TIMER MC	A B	15 15
ispMACH 4064ZE	OSC MC TIMER MC	A D	15 15
ispMACH 4128ZE	OSC MC TIMER MC	A G	15 15
ispMACH 4256ZE	OSC MC TIMER MC	C F	15 15

Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E^2 low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

Supply Current

To minimize transient current during power-on, configure CPLD I/Os to a pull-up or float state. If this logic scenario is not possible, then the recommended power sequence should assert VCC and VCCO at the same time or VCC before VCCO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	60	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	13	25	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	15	40	µA
ispMACH 4064ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	92	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	15	30	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	18	50	µA
ispMACH 4128ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	195	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	16	40	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	19	60	µA
ispMACH 4256ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	372	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	32	65	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	43	100	µA

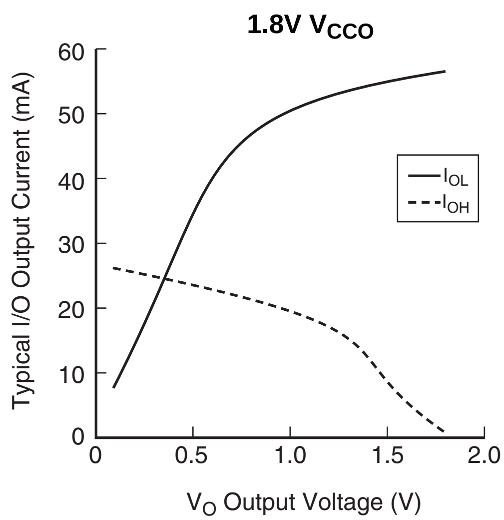
1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15µA typical current plus additional current from any logic it drives.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL} Min (V)	V_{IL} Max (V)	V_{IH} Min (V)	V_{IH} Max (V)	V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
LVTTL	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 3.3	-0.3	0.80	2.0	5.5	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 2.5	-0.3	0.70	1.70	3.6	0.40	V_{CCO} - 0.40	8.0	-4.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
LVCMOS 1.5[2]	-0.3	0.35 * V_{CC}	0.65 * V_{CC}	3.6	0.40	V_{CCO} - 0.45	2.0	-2.0
					0.20	V_{CCO} - 0.20	0.1	-0.1
PCI 3.3	-0.3	0.3 * 3.3 * (V_{CC} / 1.8)	0.5 * 3.3 * (V_{CC} / 1.8)	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from V_{CC}, if the ispMACH 4000ZE V_{CC} and the V_{CC} of the driving device (V_{CC}d-d; that determines steady state V_{IH}) are in the extreme range of their specifications. Typically, DC current drawn from V_{CC} will be 2µA per input.



ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	2.00	—	1.70	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.20	—	1.30	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.40	—	1.50	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.10	—	1.85	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.20	—	1.90	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.60	—	1.70	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.30	—	3.15	ns
t_{GPTOE}	Global PT OE Delay		—	1.80	—	2.15	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	12.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	7.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	6.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	5.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	4.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	3.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.00	—	1.00	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.40	—	0.40	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.04	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE		LC4064ZE		Units
			-4		-4		
			Min.	Max.	Min.	Max.	
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

Signal Descriptions

<table>
<tr><th>Signal Names</th><th colspan="2">Description</th></tr>
<tr><td>TMS</td><td colspan="2">Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine.</td></tr>
<tr><td>TCK</td><td colspan="2">Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine.</td></tr>
<tr><td>TDI</td><td colspan="2">Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data.</td></tr>
<tr><td>TDO</td><td colspan="2">Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out.</td></tr>
<tr><td>GOE0/IO, GOE1/IO</td><td colspan="2">These pins are configured to be either Global Output Enable Input or as general I/O pins.</td></tr>
<tr><td>GND</td><td colspan="2">Ground</td></tr>
<tr><td>NC</td><td colspan="2">Not Connected</td></tr>
<tr><td>V_{CC}</td><td colspan="2">The power supply pins for logic core and JTAG port.</td></tr>
<tr><td>CLK0/I, CLK1/I, CLK2/I, CLK3/I</td><td colspan="2">These pins are configured to be either CLK input or as an input.</td></tr>
<tr><td>V_{CCO0}, V_{CCO1}</td><td colspan="2">The power supply pins for each I/O bank.</td></tr>
<tr><td rowspan="5">yzz</td><td colspan="2">Input/Output[1] – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15.</td></tr>
<tr><td>ispMACH 4032ZE</td><td>y: A-B</td></tr>
<tr><td>ispMACH 4064ZE</td><td>y: A-D</td></tr>
<tr><td>ispMACH 4128ZE</td><td>y: A-H</td></tr>
<tr><td>ispMACH 4256ZE</td><td>y: A-P</td></tr>
</table>

1. In some packages, certain I/Os are only available for use as inputs. See the Logic Signal Connections tables for details.

ORP Reference Table

	4032ZE	4064ZE			4128ZE		4256ZE		
Number of I/Os	32	32	48	64	64	96	64	96	108
Number of GLBs	2	4	4	4	8	8	16	16	16
Number of I/Os per GLB	16	8	Mixture of 9, 10, 14, 15	16	8	12	4	6	Mixture of 6, 7, 8
Reference ORP Table (I/Os per GLB)	16	8	9, 10, 14, 15	16	8	12	4	6	6, 7, 8

ispMACH 4000ZE Power Supply and NC Connections[1] (Cont.)

Signal	132 ucBGA[3]	144 csBGA[3]	144 TQFP[2]
VCC	M1, M7, A12, B5	H5, H8, E8, E5	36, 57, 108, 129
VCCO0 VCCO (Bank 0)	B1, H4, L2, J5, A4	E4, F4, G4, J5, D5	3, 19, 34, 47, 136
VCCO1 VCCO (Bank 1)	K9, L12, F12, D9, C7	J8, H9, G9, F9, D8	64, 75, 91, 106, 119
GND	E5, E8, H5, H8	F6, G6, G7, F7	1, 37, 73, 109
GND (Bank 0)	E2, H2, M4, B7, B3	G5, H4, H6, E6, F5	10, 18[4], 27, 46, 127, 137
GND (Bank 1)	L7, J9, H12, E9, A9	H7, J9, G8, F8, E7	55, 65, 82, 90[4], 99, 118
NC	—	**4064ZE:** E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 **4128ZE:** D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2	**4128ZE:** 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 **4256ZE:** 18, 90

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	TDI	TDI
2	0	A5	A8
3	0	A6	A10
4	0	A7	A11
5	0	GND (Bank 0)	GND (Bank 0)
6	0	VCCO (Bank 0)	VCCO (Bank 0)
7	0	A8	B15
8	0	A9	B12
9	0	A10	B10
10	0	A11	B8
11	-	TCK	TCK
12	-	VCC	VCC
13	-	GND	GND
14	0	A12	B6
15	0	A13	B4
16	0	A14	B2
17	0	A15	B0
18	0	CLK1/I	CLK1/I
19	1	CLK2/I	CLK2/I
20	1	B0	C0
21	1	B1	C1
22	1	B2	C2
23	1	B3	C4
24	1	B4	C6
25	-	TMS	TMS
26	1	B5	C8
27	1	B6	C10
28	1	B7	C11
29	1	GND (Bank 1)	GND (Bank 1)
30	1	VCCO (Bank 1)	VCCO (Bank 1)
31	1	B8	D15
32	1	B9	D12
33	1	B10	D10
34	1	B11	D8
35	-	TDO	TDO
36	-	VCC	VCC
37	-	GND	GND
38	1	B12	D6
39	1	B13	D4
40	1	B14	D2
41	1	B15/GOE1	D0/GOE1
42	1	CLK3/I	CLK3/I

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA (Cont.)

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
E7	1	NC	D14
E6	1	B9	D13
D7	1	B10	D12
D8	1	NC	D11
C5	1	NC	D10
C7	1	B11	D9
C8	1	NC	D8
B8	-	TDO	TDO
D5	-	VCC	VCC
GND*	-	GND	GND
A8	1	B12	D7
A7	1	NC	D6
B7	1	NC	D5
A6	1	B13	D4
GND*	1	NC	GND (Bank 1)
C6	1	NC	VCCO (Bank 1)
B6	1	B14	D3
A5	1	NC	D2
B5	1	B15/GOE1	D0/GOE1
A4	1	CLK3/I	CLK3/I
C4	0	CLK0/I	CLK0/I
B4	0	A0/GOE0	A0/GOE0
B3	0	A1	A1
A3	0	A2	A2
A2	0	A3	A4
A1	0	A4	A6

* All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
42	1	C1	E2	I6
43	1	C2	E4	I10
44	1	C3	E6	I12
45	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
46	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
47	1	C4	E8	J2
48	1	C5	E10	J6
49	1	C6	E12	J10
50	1	C7	E14	J12
51	-	GND	GND	GND
52	-	TMS	TMS	TMS
53	1	C8	F0	K12
54	1	C9	F2	K10
55	1	C10	F4	K6
56	1	C11	F6	K2
57	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
58	1	C12	F8	L12
59	1	C13	F10	L10
60	1	C14	F12	L6
61	1	C15	F13	L4
62*	1	I	I	I
63	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
64	1	D15	G14	M4
65	1	D14	G12	M6
66	1	D13	G10	M10
67	1	D12	G8	M12
68	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
69	1	D11	G6	N2
70	1	D10	G5	N6
71	1	D9	G4	N10
72	1	D8	G2	N12
73*	1	I	I	I
74	-	TDO	TDO	TDO
75	-	VCC	VCC	VCC
76	-	GND	GND	GND
77*	1	I	I	I
78	1	D7	H13	O12
79	1	D6	H12	O10
80	1	D5	H10	O6
81	1	D4	H8	O2
82	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 100 TQFP (Cont.)

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
83	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
84	1	D3	H6	P12
85	1	D2	H4	P10
86	1	D1	H2	P6
87	1	D0/GOE1	H0/GOE1	P2/GOE1
88	1	CLK3/I	CLK3/I	CLK3/I
89	0	CLK0/I	CLK0/I	CLK0/I
90	-	VCC	VCC	VCC
91	0	A0/GOE0	A0/GOE0	A2/GOE0
92	0	A1	A2	A6
93	0	A2	A4	A10
94	0	A3	A6	A12
95	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
96	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
97	0	A4	A8	B2
98	0	A5	A10	B6
99	0	A6	A12	B10
100	0	A7	A14	B12

* This pin is input only.

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J12	1	NC Ball	NC Ball	L14
J11	1	NC Ball	NC Ball	L12
H10	1	NC Ball	F8	L10
H12	1	C12	F9	L8
G11	1	C13	F10	L6
H11	1	C14	F12	L4
G12	1	C15	F13	L2
G10*	1	I	F14	L0
G9	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
F12	1	D15	G14	M0
F11	1	D14	G13	M2
E11	1	D13	G12	M4
E12	1	D12	G10	M6
D10	1	NC Ball	G9	M8
F10	1	NC Ball	G8	M10
D12	1	NC Ball	NC Ball	M12
F8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
E10	1	D11	G6	N2
D11	1	D10	G5	N4
E9	1	D9	G4	N6
C12	1	D8	G2	N8
C11*	1	I	G1	N10
B12	1	NC Ball	G0	N12
F9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
B11	-	TDO	TDO	TDO
E8	-	VCC	VCC	VCC
F7	-	GND	GND	GND
A12	1	NC Ball	NC Ball	O14
C10	1	NC Ball	NC Ball	O12
B10	1	NC Ball	H14	O10
A11*	1	I	H13	O8
D9	1	D7	H12	O6
B9	1	D6	H10	O4
C9	1	D5	H9	O2
A10	1	D4	H8	O0
E7	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
D8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
A9	1	NC Ball	H6	P12
B8	1	NC Ball	H5	P10
C8	1	D3	H4	P8
A8	1	D2	H2	P6
D7	1	D1	H1	P4
B7	1	D0/GOE1	H0/GOE1	P2/GOE1

ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
C7	1	CLK3/I	CLK3/I	CLK3/I
E6	0	NC Ball	GND (Bank 0)	GND (Bank 0)
A7	0	CLK0/I	CLK0/I	CLK0/I
E5	-	VCC	VCC	VCC
D6	0	A0/GOE0	A0/GOE0	A2/GOE0
B6	0	A1	A1	A4
A6	0	A2	A2	A6
C6	0	A3	A4	A8
B5	0	NC Ball	A5	A10
A5	0	NC Ball	A6	A12
D5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
F5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
A4	0	A4	A8	B2
B4	0	A5	A9	B4
C5	0	A6	A10	B6
A3	0	A7	A12	B8
C4	0	NC Ball	A13	B10
B3	0	NC Ball	A14	B12
A2	0	NC Ball	NC Ball	B14

* This pin is input only for the LC4064ZE.

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.