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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4128ze-7tn100c

Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

Table 2. Individual PT Steering

Product Term	Logic	Control
PT*n*	Logic PT	Single PT for XOR/OR
PT*n*+1	Logic PT	Individual Clock (PT Clock)
PT*n*+2	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT*n*+3	Logic PT	Individual Initialization (PT Initialization)
PT*n*+4	Logic PT	Individual OE (PTOE)

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

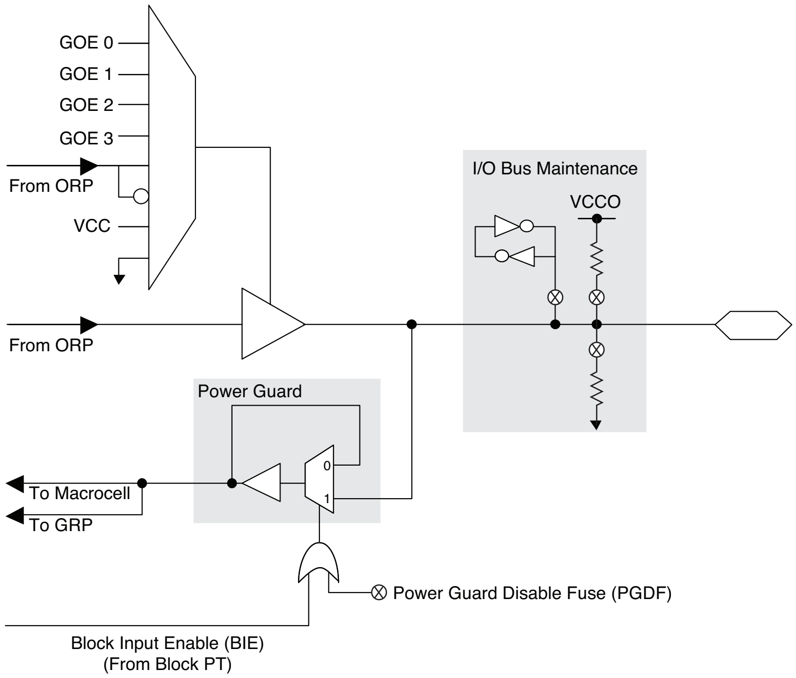
Table 3. Available Clusters for Each Macrocell

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator *n*+4. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a "per-pin" basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E^2CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings[1, 2, 3, 4]

Supply Voltage (V_{CC}) . . . . -0.5 to 2.5V

Output Supply Voltage (V_{CCO}) . . . . -0.5 to 4.5V

Input or I/O Tristate Voltage Applied[5, 6] . . . . -0.5 to 5.5V

Storage Temperature . . . .-65 to 150°C

Junction Temperature (T_j) with Power Applied . . .-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Please refer to the Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of (V_{IH} (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with VIN > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6[1]	1.9	V
T_j	Junction Temperature (Commercial)		0	90	°C
	Junction Temperature (Industrial)		-40	105	°C

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V$, Tj = 105°C	—	±30	±150	µA
		$0 \leq V_{IN} \leq 3.0V$, Tj = 130°C	—	±30	±200	µA

1. Insensitive to sequence of V_{CC} or V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCO} < V_{CCO}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until fuse circuitry is active.

Supply Current

To minimize transient current during power-on, configure CPLD I/Os to a pull-up or float state. If this logic scenario is not possible, then the recommended power sequence should assert VCC and VCCO at the same time or VCC before VCCO.

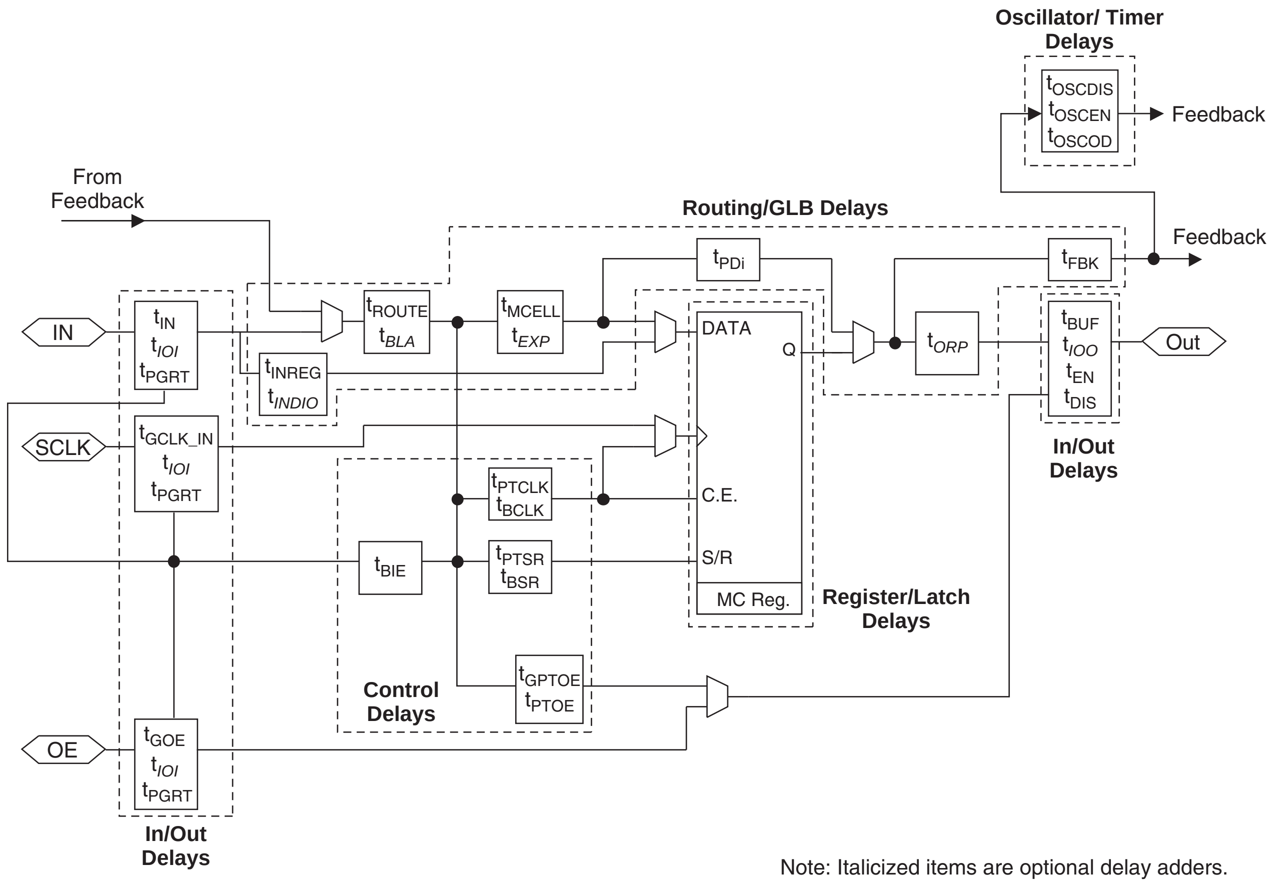
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ispMACH 4032ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	50	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	58	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	60	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	10	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	13	25	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	15	40	µA
ispMACH 4064ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	80	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	89	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	92	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	11	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	15	30	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	18	50	µA
ispMACH 4128ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	168	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	190	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	195	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	12	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	16	40	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	19	60	µA
ispMACH 4256ZE						
ICC[1, 2, 3, 5, 6]	Operating Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	341	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	361	—	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	372	—	µA
ICC[4, 5, 6]	Standby Power Supply Current	Vcc = 1.8V, T_A = 25°C	—	13	—	µA
		Vcc = 1.9V, T_A = 0 to 70°C	—	32	65	µA
		Vcc = 1.9V, T_A = -40 to 85°C	—	43	100	µA

1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or $V_{CCO,}$ bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15µA typical current plus additional current from any logic it drives.

Timing Model

The task of determining the timing through the ispMACH 4000ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, refer to TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines.

Figure 16. ispMACH 4000ZE Timing Model



Note: Italicized items are optional delay adders.

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	2.00	—	1.70	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.20	—	1.30	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.40	—	1.50	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.10	—	1.85	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.20	—	1.90	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.60	—	1.70	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.30	—	3.15	ns
t_{GPTOE}	Global PT OE Delay		—	1.80	—	2.15	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	12.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	7.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	6.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	5.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	4.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	3.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.00	—	1.00	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.40	—	0.40	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.04	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		LC4032ZE -4 Min.	LC4032ZE -4 Max.	LC4064ZE -4 Min.	LC4064ZE -4 Max.	Units
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description		All Devices				Units
			-5		-7		
			Min.	Max.	Min.	Max.	
t_{SRR}	Asynchronous Reset or Set Recovery Delay		—	1.80	—	1.67	ns
Control Delays							
t_{BCLK}	GLB PT Clock Delay		—	1.45	—	0.95	ns
t_{PTCLK}	Macrocell PT Clock Delay		—	1.45	—	1.15	ns
t_{BSR}	Block PT Set/Reset Delay		—	1.85	—	1.83	ns
t_{PTSR}	Macrocell PT Set/Reset Delay		—	1.85	—	2.72	ns
t_{BIE}	Power Guard Block Input Enable Delay		—	1.75	—	1.95	ns
t_{PTOE}	Macrocell PT OE Delay		—	2.40	—	1.90	ns
t_{GPTOE}	Global PT OE Delay		—	4.20	—	3.40	ns
Internal Oscillator							
t_{OSCSU}	Oscillator DYNOSCDIS Setup Time		5.00	—	5.00	—	ns
t_{OSCH}	Oscillator DYNOSCDIS Hold Time		5.00	—	5.00	—	ns
t_{OSCEN}	Oscillator OSCOUT Enable Time (To Stable)		—	5.00	—	5.00	ns
t_{OSCOD}	Oscillator Output Delay		—	4.00	—	4.00	ns
t_{OSCNOM}	Oscillator OSCOUT Nominal Frequency			5.00		5.00	MHz
t_{OSCvar}	Oscillator Variation of Nominal Frequency		—	30	—	30	%
$t_{TMRCO20}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider)		—	12.50	—	14.50	ns
$t_{TMRCO10}$	Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider)		—	7.50	—	9.50	ns
t_{TMRCO7}	Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider)		—	6.00	—	8.00	ns
$t_{TMRRSTO}$	Oscillator TIMEROUT Reset to Out (Going Low)		—	5.00	—	7.00	ns
t_{TMRRR}	Oscillator TIMEROUT Asynchronous Reset Recovery Delay		—	4.00	—	6.00	ns
$t_{TMRRSTPW}$	Oscillator TIMEROUT Reset Minimum Pulse Width		3.00	—	5.00	—	ns
Optional Delay Adjusters		**Base Parameter**					
t_{INDIO}	Input Register Delay	t_{INREG}	—	1.60	—	2.60	ns
t_{EXP}	Product Term Expander Delay	t_{MCELL}	—	0.45	—	0.50	ns
t_{BLA}	Additional Block Loading Adders	t_{ROUTE}	—	0.05	—	0.05	ns
t_{IOI} Input Buffer Delays							
LVTTL_in	Using LVTTL Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.60	—	0.60	ns
LVCMOS15_in	Using LVCMOS 1.5 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.20	—	0.20	ns
LVCMOS18_in	Using LVCMOS 1.8 Standard	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.00	—	0.00	ns
LVCMOS25_in	Using LVCMOS 2.5 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
LVCMOS33_in	Using LVCMOS 3.3 Standard with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
PCI_in	Using PCI Compatible Input with Hysteresis	t_{IN}, t_{GCLK_IN}, t_{GOE}	—	0.80	—	0.80	ns
t_{IOO} Output Buffer Delays							
LVTTL_out	Output Configured as TTL Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns

ispMACH 4000ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

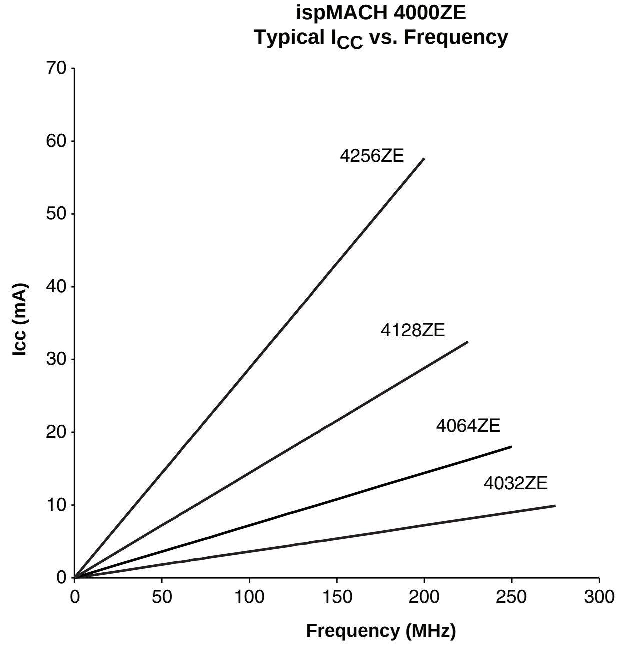
Parameter	Description		All Devices				Units
			-5		-7		
			Min.	Max.	Min.	Max.	
LVCMOS15_out	Output Configured as 1.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
LVCMOS18_out	Output Configured as 1.8V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.00	—	0.00	ns
LVCMOS25_out	Output Configured as 2.5V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.10	—	0.10	ns
LVCMOS33_out	Output Configured as 3.3V Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
PCI_out	Output Configured as PCI Compatible Buffer	t_{EN}, t_{DIS}, t_{BUF}	—	0.20	—	0.20	ns
Slow Slew	Output Configured for Slow Slew Rate	t_{EN}, t_{BUF}	—	1.00	—	1.00	ns

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
t_{BTCPSU}	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

Power Consumption



Power Estimation Coefficients[1]

Device	A	B
ispMACH 4032ZE	0.010	0.009
ispMACH 4064ZE	0.011	0.009
ispMACH 4128ZE	0.012	0.009
ispMACH 4256ZE	0.013	0.009

1. For further information about the use of these coefficients, refer to TN1187, Power Estimation in ispMACH 4000ZE Devices.

Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

Figure 17. Output Test Load, LVTTL and LVCMOS Standards

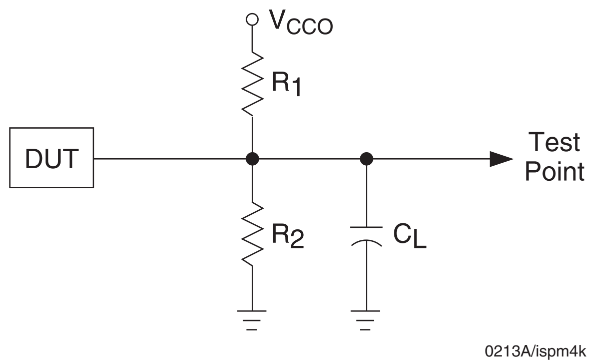


Table 13. Test Fixture Required Components

Test Condition	R_1	R_2	C_L[1]	Timing Ref.	V_{CCO}
LVCMOS I/O, (L -> H, H -> L)	106Ω	106Ω	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $\frac{V_{CCO}}{2}$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $\frac{V_{CCO}}{2}$	LVCMOS 1.8 = 1.65V
				LVCMOS 1.5 = $\frac{V_{CCO}}{2}$	LVCMOS 1.5 = 1.4V
LVCMOS I/O (Z -> H)	∞	106Ω	35pF	1.5V	3.0V
LVCMOS I/O (Z -> L)	106Ω	∞	35pF	1.5V	3.0V
LVCMOS I/O (H -> Z)	∞	106Ω	5pF	V_{OH} - 0.3	3.0V
LVCMOS I/O (L -> Z)	106Ω	∞	5pF	V_{OL} + 0.3	3.0V

1. C_L includes test fixtures and probe capacitance.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
1	-	TDI	TDI
2	0	A5	A8
3	0	A6	A10
4	0	A7	A11
5	0	GND (Bank 0)	GND (Bank 0)
6	0	VCCO (Bank 0)	VCCO (Bank 0)
7	0	A8	B15
8	0	A9	B12
9	0	A10	B10
10	0	A11	B8
11	-	TCK	TCK
12	-	VCC	VCC
13	-	GND	GND
14	0	A12	B6
15	0	A13	B4
16	0	A14	B2
17	0	A15	B0
18	0	CLK1/I	CLK1/I
19	1	CLK2/I	CLK2/I
20	1	B0	C0
21	1	B1	C1
22	1	B2	C2
23	1	B3	C4
24	1	B4	C6
25	-	TMS	TMS
26	1	B5	C8
27	1	B6	C10
28	1	B7	C11
29	1	GND (Bank 1)	GND (Bank 1)
30	1	VCCO (Bank 1)	VCCO (Bank 1)
31	1	B8	D15
32	1	B9	D12
33	1	B10	D10
34	1	B11	D8
35	-	TDO	TDO
36	-	VCC	VCC
37	-	GND	GND
38	1	B12	D6
39	1	B13	D4
40	1	B14	D2
41	1	B15/GOE1	D0/GOE1
42	1	CLK3/I	CLK3/I

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA

Ball Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
B2	-	TDI	TDI
B1	0	A5	A8
C2	0	A6	A10
C1	0	A7	A11
GND*	0	GND (Bank 0)	GND (Bank 0)
C3	0	NC	A12
E3	0	VCCO (Bank 0)	VCCO (Bank 0)
D1	0	A8	B15
D2	0	NC	B14
E1	0	A9	B13
D3	0	A10	B12
F1	0	A11	B11
E2	0	NC	B10
G1	0	NC	B9
F2	0	NC	B8
H1	-	TCK	TCK
E4	-	VCC	VCC
GND*	-	GND	GND
G2	0	A12	B6
H2	0	NC	B5
H3	0	A13	B4
GND*	0	NC	GND (Bank 0)
F4	0	NC	VCCO (Bank 0)
G3	0	A14	B3
F3	0	NC	B2
H4	0	A15	B0
G4	0	CLK1/I	CLK1/I
H5	1	CLK2/I	CLK2/I
F5	1	B0	C0
G5	1	B1	C1
G6	1	B2	C2
H6	1	B3	C4
F6	1	B4	C5
H7	1	NC	C6
H8	-	TMS	TMS
G7	1	B5	C8
F7	1	B6	C10
G8	1	B7	C11
GND*	1	GND (Bank 0)	GND (Bank 1)
F8	1	NC	C12
D6	1	VCCO (Bank 1)	VCCO (Bank 1)
E8	1	B8	D15

ispMACH 4064ZE Logic Signal Connections: 64 ucBGA

Ball Number	Bank Number	GLB/MC/Pad
A1	-	TDI
B1	0	A8
B2	0	A10
B3	0	A11
GND*	0	GND (Bank 0)
C1	0	A12
C3	0	VCCO (Bank 0)
C2	0	B15
D1	0	B14
D2	0	B13
D3	0	B12
E1	0	B11
E2	0	B10
E3	0	B9
F1	0	B8
F2	-	TCK
E4	-	VCC
GND*	-	GND
H2	0	B6
H1	0	B5
G1	0	B4
GND*	0	GND (Bank 0)
F3	0	VCCO (Bank 0)
G2	0	B3
G3	0	B2
H3	0	B0
G4	0	CLK1/I
F4	1	CLK2/I
H4	1	C0
H5	1	C1
G5	1	C2
H6	1	C4
H7	1	C5
H8	1	C6
G8	-	TMS
G7	1	C8
G6	1	C10
F8	1	C11
GND*	1	GND (Bank 1)
F7	1	C12
F6	1	VCCO (Bank 1)
F5	1	D15
E8	1	D14

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

Ball Number	Bank Number	GLB/MC/Pad
D10	1	G9
E12	1	G8
E9	1	GND (Bank 1)
D12	1	G6
D11	1	G5
C12	1	G4
C10	1	G2
C11	1	G1
B11	1	G0
D9	1	VCCO (Bank 1)
B12	-	TDO
A12	-	VCC
GND*	-	GND
A10	1	H14
A11	1	H13
B10	1	H12
C9	1	H10
D8	1	H9
C8	1	H8
A9	1	GND (Bank 1)
C7	1	VCCO (Bank 1)
B9	1	H6
B8	1	H5
D7	1	H4
A8	1	H2
A7	1	H1
B6	1	H0/GOE1
C6	1	CLK3/I
B7	0	GND (Bank 0)
D6	0	CLK0/I
B5	-	VCC
A6	0	A0/GOE0
C5	0	A1
B4	0	A2
A5	0	A4
C4	0	A5
D5	0	A6
A4	0	VCCO (Bank 0)
B3	0	GND (Bank 0)
D4	0	A8
A3	0	A9
C3	0	A10
B2	0	A12
C2	0	A13

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
86	1	F12	L8
87	1	F13	L6
88	1	F14	L4
89*	1	NC	I
90	1	GND (Bank 1)	NC
91	1	VCCO (Bank 1)	VCCO (Bank 1)
92*	1	NC	I
93	1	G14	M2
94	1	G13	M4
95	1	G12	M6
96	1	G10	M8
97	1	G9	M10
98	1	G8	M12
99	1	GND (Bank 1)	GND (Bank 1)
100	1	G6	N2
101	1	G5	N4
102	1	G4	N6
103	1	G2	N8
104	1	G1	N10
105	1	G0	N12
106	1	VCCO (Bank 1)	VCCO (Bank 1)
107	-	TDO	TDO
108	-	VCC	VCC
109	-	GND	GND
110*	1	NC	I
111	1	H14	O12
112	1	H13	O10
113	1	H12	O8
114	1	H10	O6
115	1	H9	O4
116	1	H8	O2
117*	1	NC	I
118	1	GND (Bank 1)	GND (Bank 1)
119	1	VCCO (Bank 1)	VCCO (Bank 1)
120	1	H6	P12
121	1	H5	P10
122	1	H4	P8
123	1	H2	P6
124	1	H1	P4
125	1	H0/GOE1	P2/GOE1
126	1	CLK3/I	CLK3/I
127	0	GND (Bank 0)	GND (Bank 0)
128	0	CLK0/I	CLK0/I

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
129	-	VCC	VCC
130	0	A0/GOE0	A2/GOE0
131	0	A1	A4
132	0	A2	A6
133	0	A4	A8
134	0	A5	A10
135	0	A6	A12
136	0	VCCO (Bank 0)	VCCO (Bank 0)
137	0	GND (Bank 0)	GND (Bank 0)
138	0	A8	B2
139	0	A9	B4
140	0	A10	B6
141	0	A12	B8
142	0	A13	B10
143	0	A14	B12
144*	0	NC	I

* This pin is input only for the LC4256ZE.