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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.8 ns
Voltage Supply - Internal	1.7V ~ 1.9V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256ze-5tn100c">https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256ze-5tn100c</a>

## Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

**Table 2. Individual PT Steering**

Product Term	Logic	Control
PT $n$	Logic PT	Single PT for XOR/OR
PT $n+1$	Logic PT	Individual Clock (PT Clock)
PT $n+2$	Logic PT	Individual Initialization or Individual Clock Enable (PT Initialization/CE)
PT $n+3$	Logic PT	Individual Initialization (PT Initialization)
PT $n+4$	Logic PT	Individual OE (PTOE)

## Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

**Table 3. Available Clusters for Each Macrocell**

Macrocell	Available Clusters			
M0	—	C0	C1	C2
M1	C0	C1	C2	C3
M2	C1	C2	C3	C4
M3	C2	C3	C4	C5
M4	C3	C4	C5	C6
M5	C4	C5	C6	C7
M6	C5	C6	C7	C8
M7	C6	C7	C8	C9
M8	C7	C8	C9	C10
M9	C8	C9	C10	C11
M10	C9	C10	C11	C12
M11	C10	C11	C12	C13
M12	C11	C12	C13	C14
M13	C12	C13	C14	C15
M14	C13	C14	C15	—
M15	C14	C15	—	—

## Wide Steering Logic

The wide steering logic allows the output of the cluster allocator  $n$  to be connected to the input of the cluster allocator  $n+4$ . Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

### Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

### Initialization Control

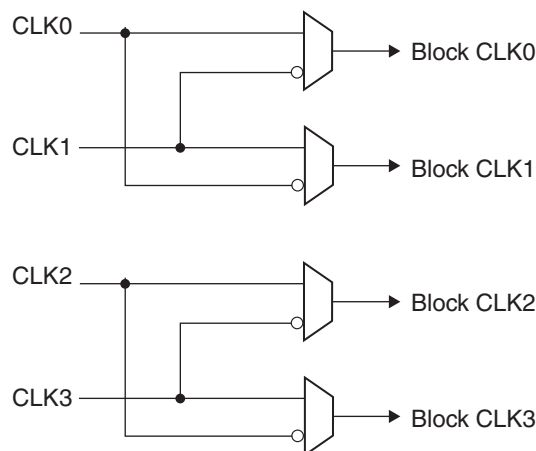
The ispMACH 4000ZE family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

### GLB Clock Generator

Each ispMACH 4000ZE device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

**Figure 6. GLB Clock Generator**



The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

**Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices**

Device	Number of Logic Blocks, Power Guard Blocks and BIE Signals
ispMACH 4032ZE	Two (Blocks: A and B)
ispMACH 4064ZE	Four (Blocks: A, B, C and D)
ispMACH 4128ZE	Eight (Blocks: A, B, C, ..., H)
ispMACH 4256ZE	Sixteen (Blocks: A, B, C, ..., P)

### Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

**Table 9. Dedicated Clock Inputs to BIE Association**

CLK/I	32 MC Block	64MC Block	128MC Block	256MC Block
CLK0 / I	A	A	A	A
CLK1 / I	A	B	D	H
CLK2 / I	B	C	E	I
CLK3 / I	B	D	H	P

**Table 10. Dedicated Inputs to BIE Association**

Dedicated Input	4064ZE Block	4128ZE Block	4256ZE Block
0	A	B	D
1	B	C	E
2	B	D	G
3	C	F	G
4	D	G	J
5	D	H	L
6	—	—	M
7	—	—	O
8	—	—	O
9	—	—	B

For more information on the Power Guard function refer to TN1174, [Advanced Features of the ispMACH 4000ZE Family](#).

### Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

**Figure 13. On-Chip Oscillator and Timer**

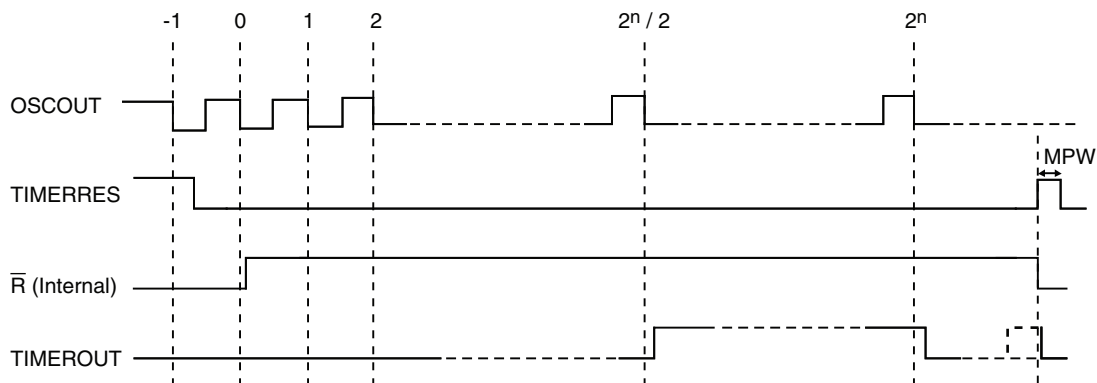
**Table 11. On-Chip Oscillator and Timer Signal Names**

Signal Name	Input or Output	Optional / Required	Description
OSCOUT	Output	Optional	Oscillator Output (Nominal Frequency: 5MHz)
TIMEROUT	Output	Optional	Oscillator Frequency Divided by an integer TIMER_DIV (Default 128)
TIMERRES	Input	Optional	Reset the Timer
DYNOSCDIS	Input	Optional	Disables the Oscillator, resets the Timer and saves the power.

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER\_DIV.

The attribute TIMER\_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal “ $\bar{R}$ ” is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

**Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT**


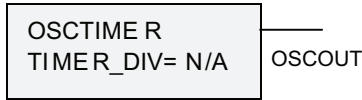
Note:  $n$  = Number of bits in the divider (7, 10 or 20)

Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

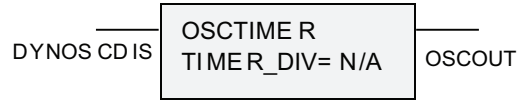
### Some Simple Use Scenarios

The following diagrams show a few simple examples that omit optional signals for the OSCTIMER block:

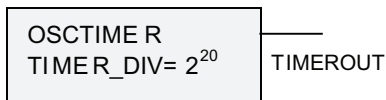
- A. An oscillator giving 5MHz nominal clock
- B. An oscillator that can be disabled with an external signal (5MHz nominal clock)
- C. An oscillator giving approximately 5 Hz nominal clock (TIMER\_DIV =  $2^{20}$  (1,048,576))
- D. An oscillator giving two output clocks: ~5MHz and ~5KHz (TIMER\_DIV =  $2^{10}$  (1,024))



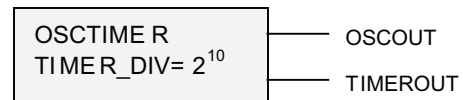
(A) A simple 5MHz oscillator.



(B) An oscillator with dynamic disable.



(C) A simple 5Hz oscillator.



(D) Oscillator with two outputs (5MHz and 5KHz).

### OSCTIMER Integration With CPLD Fabric

The OSCTIMER is integrated into the CPLD fabric using the Global Routing Pool (GRP). The macrocell (MC) feedback path for two macrocells is augmented with a programmable multiplexer, as shown in Figure 15. The OSCTIMER outputs (OSCOUT and TIMEROUT) can optionally drive the GRP lines, whereas the macrocell outputs can drive the optional OSCTIMER inputs TIMERRES and DYNOSCDIS.

Figure 15. OSCTIMER Integration With CPLD Fabric

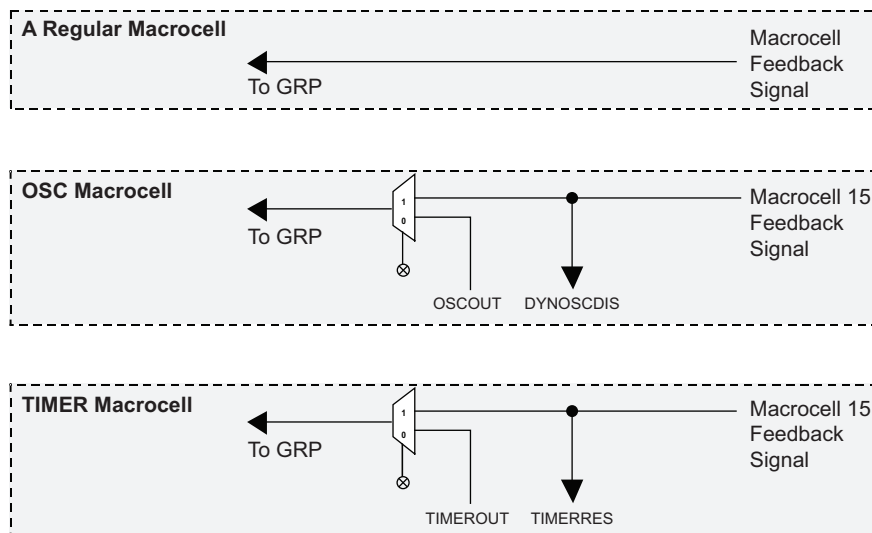


Table 12 shows how these two MCs are designated in each of the ispMACH4000ZE device.

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

## **User Electronic Signature**

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E<sup>2</sup>CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## **Security Bit**

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## **Hot Socketing**

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

## **Density Migration**

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

## Absolute Maximum Ratings<sup>1, 2, 3, 4</sup>

Supply Voltage ( $V_{CC}$ ) . . . . . -0.5 to 2.5V  
 Output Supply Voltage ( $V_{CCO}$ ) . . . . . -0.5 to 4.5V  
 Input or I/O Tristate Voltage Applied<sup>5, 6</sup> . . . . . -0.5 to 5.5V  
 Storage Temperature . . . . . -65 to 150°C  
 Junction Temperature ( $T_j$ ) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. Please refer to the [Lattice ispMACH 4000V/B/C/ZC/ZE Product Family Qualification Summary](#) for complete data, including the ESD performance data.
5. Undershoot of -2V and overshoot of ( $V_{IH}$  (MAX) + 2V), up to a total pin voltage of 6V is permitted for a duration of <20ns.
6. Maximum of 64 I/Os per device with  $V_{IN} > 3.6V$  is allowed.

## Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Supply Voltage	Standard Voltage Operation	1.7	1.9	V
		Extended Voltage Operation	1.6 <sup>1</sup>	1.9	V
$T_j$	Junction Temperature (Commercial)	0	90	°C	
	Junction Temperature (Industrial)	-40	105	°C	

1. Devices operating at 1.6V can expect performance degradation up to 35%.

## Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle	1,000	—	Cycles

Note: Valid over commercial temperature range.

## Hot Socketing Characteristics<sup>1,2,3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{DK}$	Input or I/O Leakage Current	$0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$	—	±30	±150	μA
		$0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$	—	±30	±200	μA

1. Insensitive to sequence of  $V_{CC}$  or  $V_{CCO}$ . However, assumes monotonic rise/fall rates for  $V_{CC}$  and  $V_{CCO}$ , provided  $(V_{IN} - V_{CCO}) \leq 3.6V$ .
2.  $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$ .
3.  $I_{DK}$  is additive to  $I_{PU}, I_{PD}$  or  $I_{BH}$ . Device defaults to pull-up until fuse circuitry is active.



## Supply Current

To minimize transient current during power-on, configure CPLD I/Os to a pull-up or float state. If this logic scenario is not possible, then the recommended power sequence should assert VCC and VCCO at the same time or VCC before VCCO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
<b>ispMACH 4032ZE</b>						
ICC <sup>1, 2, 3, 5, 6</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	50	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	58	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	60	—	μA
ICC <sup>4, 5, 6</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	10	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	13	25	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	15	40	μA
<b>ispMACH 4064ZE</b>						
ICC <sup>1, 2, 3, 5, 6</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	80	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	89	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	92	—	μA
ICC <sup>4, 5, 6</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	11	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	15	30	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	18	50	μA
<b>ispMACH 4128ZE</b>						
ICC <sup>1, 2, 3, 5, 6</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	168	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	190	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	195	—	μA
ICC <sup>4, 5, 6</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	12	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	16	40	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	19	60	μA
<b>ispMACH 4256ZE</b>						
ICC <sup>1, 2, 3, 5, 6</sup>	Operating Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	341	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	361	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	372	—	μA
ICC <sup>4, 5, 6</sup>	Standby Power Supply Current	V <sub>CC</sub> = 1.8V, T <sub>A</sub> = 25°C	—	13	—	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = 0 to 70°C	—	32	65	μA
		V <sub>CC</sub> = 1.9V, T <sub>A</sub> = -40 to 85°C	—	43	100	μA

1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I<sub>CC</sub> varies with specific device configuration and operating frequency.
4. V<sub>CCO</sub> = 3.6V, V<sub>IN</sub> = 0V or V<sub>CCO</sub>, bus maintenance turned off. V<sub>IN</sub> above V<sub>CCO</sub> will add transient current above the specified standby I<sub>CC</sub>.
5. Includes V<sub>CCO</sub> current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15μA typical current plus additional current from any logic it drives.

**ispMACH 400ZE Internal Timing Parameters (Cont.)**

Over Recommended Operating Conditions

Parameter	Description	All Devices				Units
		-5		-7		
		Min.	Max.	Min.	Max.	
<b>In/Out Delays</b>						
$t_{IN}$	Input Buffer Delay	—	1.05	—	1.90	ns
$t_{GCLK\_IN}$	Global Clock Input Buffer Delay	—	1.95	—	2.15	ns
$t_{GOE}$	Global OE Pin Delay	—	3.00	—	4.30	ns
$t_{BUF}$	Delay through Output Buffer	—	1.10	—	1.30	ns
$t_{EN}$	Output Enable Time	—	2.50	—	2.70	ns
$t_{DIS}$	Output Disable Time	—	2.50	—	2.70	ns
$t_{PGSU}$	Input Power Guard Setup Time	—	4.30	—	5.60	ns
$t_{PGH}$	Input Power Guard Hold Time	—	0.00	—	0.00	ns
$t_{PGPW}$	Input Power Guard BIE Minimum Pulse Width	—	6.00	—	8.00	ns
$t_{PGRT}$	Input Power Guard Recovery Time Following BIE Dis- sertation	—	5.00	—	7.00	ns
<b>Routing Delays</b>						
$t_{ROUTE}$	Delay through GRP	—	2.25	—	2.50	ns
$t_{PDi}$	Macrocell Propagation Delay	—	0.45	—	0.50	ns
$t_{MCELL}$	Macrocell Delay	—	0.65	—	1.00	ns
$t_{INREG}$	Input Buffer to Macrocell Register Delay	—	1.00	—	1.00	ns
$t_{FBK}$	Internal Feedback Delay	—	0.75	—	0.30	ns
$t_{ORP}$	Output Routing Pool Delay	—	0.30	—	0.30	ns
<b>Register/Latch Delays</b>						
$t_S$	D-Register Setup Time (Global Clock)	0.90	—	1.25	—	ns
$t_{S\_PT}$	D-Register Setup Time (Product Term Clock)	2.00	—	2.35	—	ns
$t_H$	D-Register Hold Time	2.00	—	3.25	—	ns
$t_{ST}$	T-Register Setup Time (Global Clock)	1.10	—	1.45	—	ns
$t_{ST\_PT}$	T-register Setup Time (Product Term Clock)	2.20	—	2.65	—	ns
$t_{HT}$	T-Register Hold Time	2.00	—	3.25	—	ns
$t_{SIR}$	D-Input Register Setup Time (Global Clock)	1.20	—	0.65	—	ns
$t_{SIR\_PT}$	D-Input Register Setup Time (Product Term Clock)	1.45	—	1.45	—	ns
$t_{HIR}$	D-Input Register Hold Time (Global Clock)	1.40	—	2.05	—	ns
$t_{HIR\_PT}$	D-Input Register Hold Time (Product Term Clock)	1.10	—	1.20	—	ns
$t_{COi}$	Register Clock to Output/Feedback MUX Time	—	0.45	—	0.75	ns
$t_{CES}$	Clock Enable Setup Time	2.00	—	2.00	—	ns
$t_{CEH}$	Clock Enable Hold Time	0.00	—	0.00	—	ns
$t_{SL}$	Latch Setup Time (Global Clock)	0.90	—	1.55	—	ns
$t_{SL\_PT}$	Latch Setup Time (Product Term Clock)	2.00	—	2.05	—	ns
$t_{HL}$	Latch Hold Time	2.00	—	1.17	—	ns
$t_{GOi}$	Latch Gate to Output/Feedback MUX Time	—	0.35	—	0.33	ns
$t_{PDLi}$	Propagation Delay through Transparent Latch to Output/ Feedback MUX	—	0.25	—	0.25	ns
$t_{SRi}$	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.95	—	0.28	ns

## Boundary Scan Waveforms and Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t <sub>BTCP</sub>	TCK [BSCAN test] clock cycle	40	—	ns
t <sub>BTCH</sub>	TCK [BSCAN test] pulse width high	20	—	ns
t <sub>BTCL</sub>	TCK [BSCAN test] pulse width low	20	—	ns
t <sub>BTSU</sub>	TCK [BSCAN test] setup time	8	—	ns
t <sub>BTH</sub>	TCK [BSCAN test] hold time	10	—	ns
t <sub>BRF</sub>	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t <sub>BTCO</sub>	TAP controller falling edge of clock to valid output	—	10	ns
t <sub>BTOZ</sub>	TAP controller falling edge of clock to data output disable	—	10	ns
t <sub>BTVO</sub>	TAP controller falling edge of clock to data output enable	—	10	ns
t <sub>BTCPsu</sub>	BSCAN test Capture register setup time	8	—	ns
t <sub>BTCPH</sub>	BSCAN test Capture register hold time	10	—	ns
t <sub>BTUCO</sub>	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t <sub>BTUOZ</sub>	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t <sub>BTUOV</sub>	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

**ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)**

Pin Number	Bank Number	ispMACH 4032ZE	ispMACH 4064ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	CLK0/I	CLK0/I
44	0	A0/GOE0	A0/GOE0
45	0	A1	A1
46	0	A2	A2
47	0	A3	A4
48	0	A4	A6

**ispMACH 4064ZE Logic Signal Connections: 64 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
E7	1	D13
E6	1	D12
D8	1	D11
D7	1	D10
D6	1	D9
C8	1	D8
C7	-	TDO
D5	-	VCC
GND*	-	GND
B8	1	D7
A8	1	D6
B7	1	D5
A7	1	D4
GND*	1	GND (Bank 1)
A6	1	VCCO (Bank 1)
B6	1	D3
C6	1	D2
A5	1	D0/GOE1
B5	1	CLK3/I
C5	0	CLK0/I
A4	0	A0/GOE0
B4	0	A1
C4	0	A2
A3	0	A4
A2	0	A6

\* All bonded grounds are connected to the following two balls, D4 and E5.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
 100 TQFP**

Pin Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
1	-	GND	GND	GND
2	-	TDI	TDI	TDI
3	0	A8	B0	C12
4	0	A9	B2	C10
5	0	A10	B4	C6
6	0	A11	B6	C2
7	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
8	0	A12	B8	D12
9	0	A13	B10	D10
10	0	A14	B12	D6
11	0	A15	B13	D4
12*	0	I	I	I
13	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
14	0	B15	C14	E4
15	0	B14	C12	E6
16	0	B13	C10	E10
17	0	B12	C8	E12
18	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
19	0	B11	C6	F2
20	0	B10	C5	F6
21	0	B9	C4	F10
22	0	B8	C2	F12
23*	0	I	I	I
24	-	TCK	TCK	TCK
25	-	VCC	VCC	VCC
26	-	GND	GND	GND
27*	0	I	I	I
28	0	B7	D13	G12
29	0	B6	D12	G10
30	0	B5	D10	G6
31	0	B4	D8	G2
32	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
33	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
34	0	B3	D6	H12
35	0	B2	D4	H10
36	0	B1	D2	H6
37	0	B0	D0	H2
38	0	CLK1/I	CLK1/I	CLK1/I
39	1	CLK2/I	CLK2/I	CLK2/I
40	-	VCC	VCC	VCC
41	1	C0	E0	I2

**ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)**

Ball Number	Bank Number	GLB/MC/Pad
M5	0	D5
J6	0	D4
K6	0	D2
L6	0	D1
M6	0	D0
K7	0	CLK1/I
L7	1	GND (Bank 1)
J7	1	CLK2/I
M7	-	VCC
K8	1	E0
L8	1	E1
M8	1	E2
J8	1	E4
L9	1	E5
M9	1	E6
K9	1	VCCO (Bank 1)
J9	1	GND (Bank 1)
L10	1	E8
K10	1	E9
M10	1	E10
L11	1	E12
K12	1	E13
M11	1	E14
GND*	-	GND
M12	-	TMS
L12	1	VCCO (Bank 1)
K11	1	F0
J10	1	F1
H9	1	F2
J12	1	F4
J11	1	F5
H10	1	F6
H12	1	GND (Bank 1)
G9	1	F8
H11	1	F9
F9	1	F10
G12	1	F12
G11	1	F13
G10	1	F14
F12	1	VCCO (Bank 1)
F10	1	G14
F11	1	G13
E11	1	G12
E10	1	G10

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
144 csBGA**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
F6	-	GND	GND	GND
A1	-	TDI	TDI	TDI
E4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
B2	0	NC Ball	B0	C12
B1	0	NC Ball	B1	C10
C3	0	A8	B2	C8
C2	0	A9	B4	C6
C1	0	A10	B5	C4
D1	0	A11	B6	C2
G5	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
D2	0	NC Ball	NC Ball	D14
D3	0	NC Ball	NC Ball	D12
E1	0	NC Ball	B8	D10
E2	0	A12	B9	D8
F2	0	A13	B10	D6
D4	0	A14	B12	D4
F1	0	A15	B13	D2
F3*	0	I	B14	D0
F4	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
G1	0	B15	C14	E0
E3	0	B14	C13	E2
G2	0	B13	C12	E4
G3	0	B12	C10	E6
H1	0	NC Ball	C9	E8
H3	0	NC Ball	C8	E10
H2	0	NC Ball	NC Ball	E12
H4	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J1	0	B11	C6	F2
J3	0	B10	C5	F4
J2	0	B9	C4	F6
K1	0	B8	C2	F8
K2*	0	I	C1	F10
L1	0	NC Ball	C0	F12
G4	0	NC Ball	VCCO (Bank 0)	VCCO (Bank 0)
L2	-	TCK	TCK	TCK
H5	-	VCC	VCC	VCC
G6	-	GND	GND	GND
M1	0	NC Ball	NC Ball	G14
K3	0	NC Ball	NC Ball	G12
M2	0	NC Ball	D14	G10
L3*	0	I	D13	G8



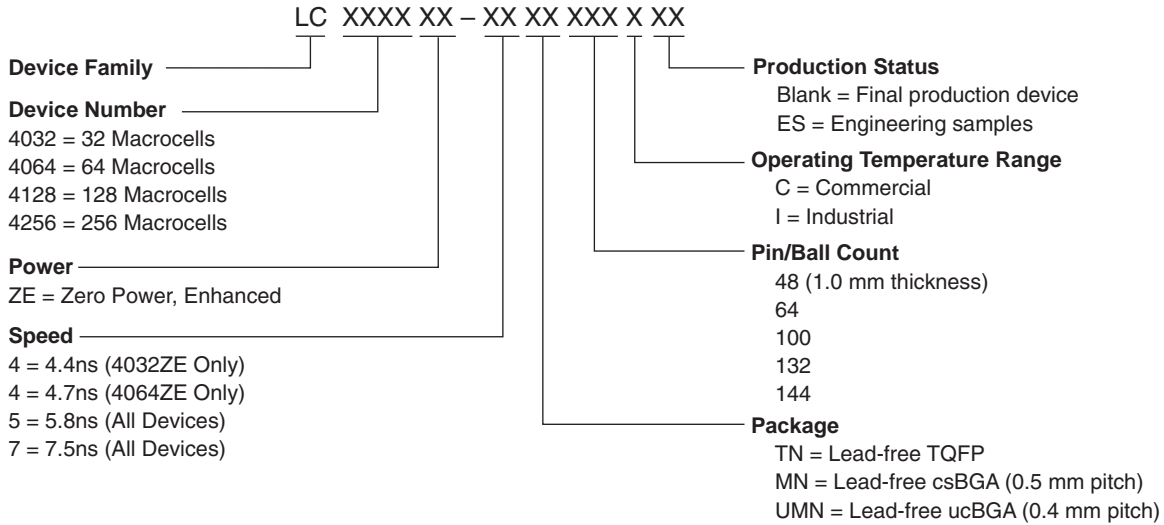
**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:  
 144 csBGA (Cont.)**

Ball Number	Bank Number	LC4064ZE	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad	GLB/MC/Pad
J4	0	B7	D12	G6
K4	0	B6	D10	G4
M3	0	B5	D9	G2
L4	0	B4	D8	G0
H6	0	GND (Bank 0)	GND (Bank 0)	GND (Bank 0)
J5	0	VCCO (Bank 0)	VCCO (Bank 0)	VCCO (Bank 0)
M4	0	NC Ball	D6	H12
L5	0	NC Ball	D5	H10
K5	0	B3	D4	H8
J6	0	B2	D2	H6
M5	0	B1	D1	H4
K6	0	B0	D0	H2
L6	0	CLK1/I	CLK1/I	CLK1/I
H7	1	NC Ball	GND (Bank 1)	GND (Bank 1)
M6	1	CLK2/I	CLK2/I	CLK2/I
H8	-	VCC	VCC	VCC
K7	1	C0	E0	I2
M7	1	C1	E1	I4
L7	1	C2	E2	I6
J7	1	C3	E4	I8
L8	1	NC Ball	E5	I10
M8	1	NC Ball	E6	I12
J8	1	VCCO (Bank 1)	VCCO (Bank 1)	VCCO (Bank 1)
J9	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)
M9	1	C4	E8	J2
L9	1	C5	E9	J4
K8	1	C6	E10	J6
M10	1	C7	E12	J8
L10	1	NC Ball	E13	J10
K9	1	NC Ball	E14	J12
M11	1	NC Ball	NC Ball	J14
G7	-	GND	GND	GND
M12	-	TMS	TMS	TMS
H9	1	NC Ball	VCCO (Bank 1)	VCCO (Bank 1)
L12	1	NC Ball	F0	K12
L11	1	NC Ball	F1	K10
K10	1	C8	F2	K8
K12	1	C9	F4	K6
J10	1	C10	F5	K4
K11	1	C11	F6	K2
G8	1	GND (Bank 1)	GND (Bank 1)	GND (Bank 1)

**ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)**

Pin Number	Bank Number	LC4128ZE	LC4256ZE
		GLB/MC/Pad	GLB/MC/Pad
43	0	D9	G4
44	0	D8	G2
45*	0	NC	I
46	0	GND (Bank 0)	GND (Bank 0)
47	0	VCCO (Bank 0)	VCCO (Bank 0)
48	0	D6	H12
49	0	D5	H10
50	0	D4	H8
51	0	D2	H6
52	0	D1	H4
53	0	D0	H2
54	0	CLK1/I	CLK1/I
55	1	GND (Bank 1)	GND (Bank 1)
56	1	CLK2/I	CLK2/I
57	-	VCC	VCC
58	1	E0	I2
59	1	E1	I4
60	1	E2	I6
61	1	E4	I8
62	1	E5	I10
63	1	E6	I12
64	1	VCCO (Bank 1)	VCCO (Bank 1)
65	1	GND (Bank 1)	GND (Bank 1)
66	1	E8	J2
67	1	E9	J4
68	1	E10	J6
69	1	E12	J8
70	1	E13	J10
71	1	E14	J12
72*	1	NC	I
73	-	GND	GND
74	-	TMS	TMS
75	1	VCCO (Bank 1)	VCCO (Bank 1)
76	1	F0	K12
77	1	F1	K10
78	1	F2	K8
79	1	F4	K6
80	1	F5	K4
81	1	F6	K2
82	1	GND (Bank 1)	GND (Bank 1)
83	1	F8	L14
84	1	F9	L12
85	1	F10	L10

### Part Number Description



### ispMACH 400ZE Family Speed Grade Offering

	-4	-5		-7	
	Commercial	Commercial	Industrial	Commercial	Industrial
ispMACH 4032ZE	✓	✓	✓	✓	✓
ispMACH 4064ZE	✓	✓	✓	✓	✓
ispMACH 4128ZE		✓		✓	✓
ispMACH 4256ZE		✓		✓	✓

### Ordering Information

Note: ispMACH 400ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages

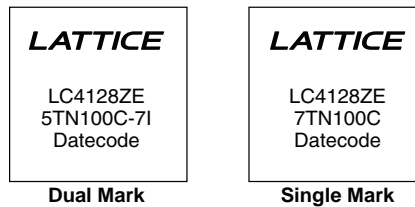
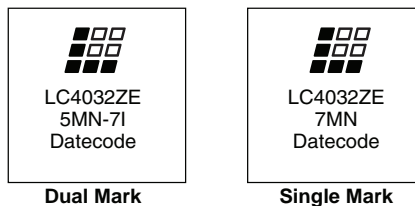
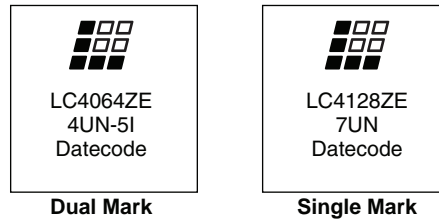


Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages



**Figure 20. Mark Format for 64 ucBGA and 132 ucBGA Packages**


## Lead-Free Packaging

### Commercial

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-4TN48C	32	1.8	4.4	Lead-Free TQFP	48	32	C
	LC4032ZE-5TN48C	32	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4032ZE-7TN48C	32	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4032ZE-4MN64C	32	1.8	4.4	Lead-Free csBGA	64	32	C
	LC4032ZE-5MN64C	32	1.8	5.8	Lead-Free csBGA	64	32	C
	LC4032ZE-7MN64C	32	1.8	7.5	Lead-Free csBGA	64	32	C
LC4064ZE	LC4064ZE-4TN48C	64	1.8	4.7	Lead-Free TQFP	48	32	C
	LC4064ZE-5TN48C	64	1.8	5.8	Lead-Free TQFP	48	32	C
	LC4064ZE-7TN48C	64	1.8	7.5	Lead-Free TQFP	48	32	C
	LC4064ZE-4TN100C	64	1.8	4.7	Lead-Free TQFP	100	64	C
	LC4064ZE-5TN100C	64	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4064ZE-7TN100C	64	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4064ZE-4MN64C	64	1.8	4.7	Lead-Free csBGA	64	48	C
	LC4064ZE-5MN64C	64	1.8	5.8	Lead-Free csBGA	64	48	C
	LC4064ZE-7MN64C	64	1.8	7.5	Lead-Free csBGA	64	48	C
	LC4064ZE-4MN144C	64	1.8	4.7	Lead-Free csBGA	144	64	C
LC4064ZE-5MN144C	64	1.8	5.8	Lead-Free csBGA	144	64	C	
LC4064ZE-7MN144C	64	1.8	7.5	Lead-Free csBGA	144	64	C	
LC4128ZE	LC4128ZE-5TN100C	128	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4128ZE-7TN100C	128	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4128ZE-5TN144C	128	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4128ZE-7TN144C	128	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4128ZE-5UMN132C	128	1.8	5.8	Lead-Free ucBGA	132	96	C
	LC4128ZE-7UMN132C	128	1.8	7.5	Lead-Free ucBGA	132	96	C
	LC4128ZE-5MN144C	128	1.8	5.8	Lead-Free csBGA	144	96	C
	LC4128ZE-7MN144C	128	1.8	7.5	Lead-Free csBGA	144	96	C
LC4256ZE	LC4256ZE-5TN100C	256	1.8	5.8	Lead-Free TQFP	100	64	C
	LC4256ZE-7TN100C	256	1.8	7.5	Lead-Free TQFP	100	64	C
	LC4256ZE-5TN144C	256	1.8	5.8	Lead-Free TQFP	144	96	C
	LC4256ZE-7TN144C	256	1.8	7.5	Lead-Free TQFP	144	96	C
	LC4256ZE-5MN144C	256	1.8	5.8	Lead-Free csBGA	144	108	C
	LC4256ZE-7MN144C	256	1.8	7.5	Lead-Free csBGA	144	108	C

**Industrial**

Device	Part Number	Macrocells	Voltage	t <sub>PD</sub>	Package	Pin/Ball Count	I/O	Grade
LC4032ZE	LC4032ZE-5TN48I	32	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4032ZE-7TN48I	32	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4032ZE-5MN64I	32	1.8	5.8	Lead-Free csBGA	64	32	I
	LC4032ZE-7MN64I	32	1.8	7.5	Lead-Free csBGA	64	32	I
LC4064ZE	LC4064ZE-5TN48I	64	1.8	5.8	Lead-Free TQFP	48	32	I
	LC4064ZE-7TN48I	64	1.8	7.5	Lead-Free TQFP	48	32	I
	LC4064ZE-5TN100I	64	1.8	5.8	Lead-Free TQFP	100	64	I
	LC4064ZE-7TN100I	64	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4064ZE-5MN64I	64	1.8	5.8	Lead-Free csBGA	64	48	I
	LC4064ZE-7MN64I	64	1.8	7.5	Lead-Free csBGA	64	48	I
	LC4064ZE-5UMN64I	64	1.8	5.8	Lead-Free ucBGA	64	48	I
	LC4064ZE-7UMN64I	64	1.8	7.5	Lead-Free ucBGA	64	48	I
	LC4064ZE-5MN144I	64	1.8	5.8	Lead-Free csBGA	144	64	I
LC4064ZE-7MN144I	64	1.8	7.5	Lead-Free csBGA	144	64	I	
LC4128ZE	LC4128ZE-7TN100I	128	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4128ZE-7UMN132I	128	1.8	7.5	Lead-Free ucBGA	132	96	I
	LC4128ZE-7TN144I	128	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4128ZE-7MN144I	128	1.8	7.5	Lead-Free csBGA	144	96	I
LC4256ZE	LC4256ZE-7TN100I	256	1.8	7.5	Lead-Free TQFP	100	64	I
	LC4256ZE-7TN144I	256	1.8	7.5	Lead-Free TQFP	144	96	I
	LC4256ZE-7MN144I	256	1.8	7.5	Lead-Free csBGA	144	108	I

1. Contact factory for product availability.

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, [ispMACH 4000ZE Timing Model Design and Usage Guidelines](#)
- TN1174, [Advanced Features of the ispMACH 4000ZE Family](#)
- TN1187, [Power Estimation in ispMACH 4000ZE Devices](#)
- [Package Diagrams](#)

## Technical Support Assistance

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