

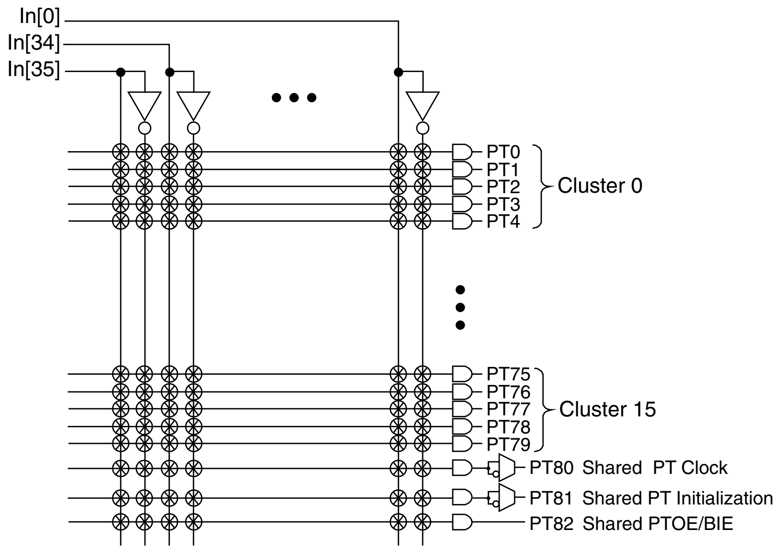

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5.8 ns |
| Voltage Supply - Internal | 1.7V ~ 1.9V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | - |
| Number of I/O | 96 |
| Operating Temperature | 0°C ~ 90°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lc4256ze-5tn144c |

*Figure 3. AND Array*




Note:
⊗ Indicates programmable fuse.

## Enhanced Logic Allocator

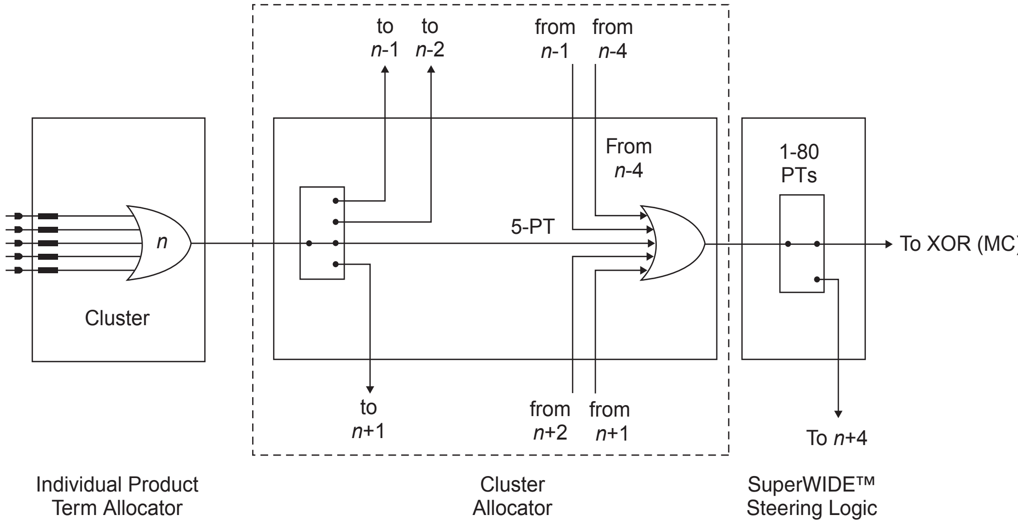
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

*Figure 4. Macrocell Slice*



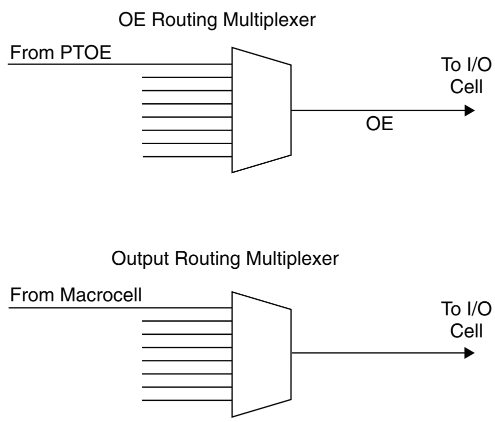
## Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. The enhanced ORP of the ispMACH 4000ZE family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

***Figure 7. ORP Slice***



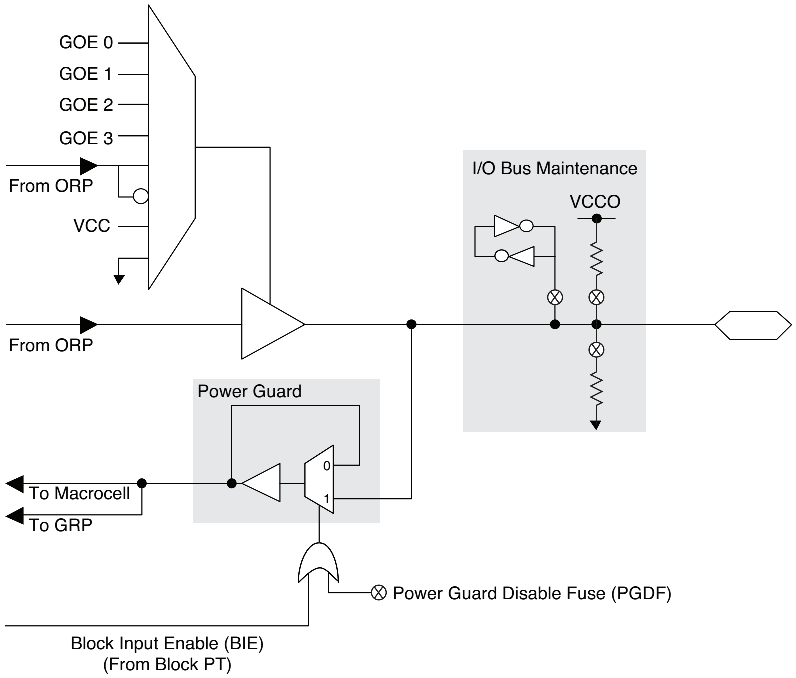

## Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-7 provide the connection details.

***Table 5. GLB/MC/ORP Combinations for ispMACH 4256ZE***

| GLB/MC | ORP Mux Input Macrocells |
|---|---|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 2] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 3] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 4] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 5] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 6] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 7] | M14, M15, M0, M1, M2, M3, M4, M5 |

*Figure 8. I/O Cell*




Each output supports a variety of output standards dependent on the $V_{CCO}$ supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the $V_{CCO}$ supplied to its I/O bank. The I/O standards supported are:

- LVTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a "per-pin" basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

## Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macrocell device (with 16 blocks), each block's BIE signal is driven by block-level OE PT from each block.

***Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE***

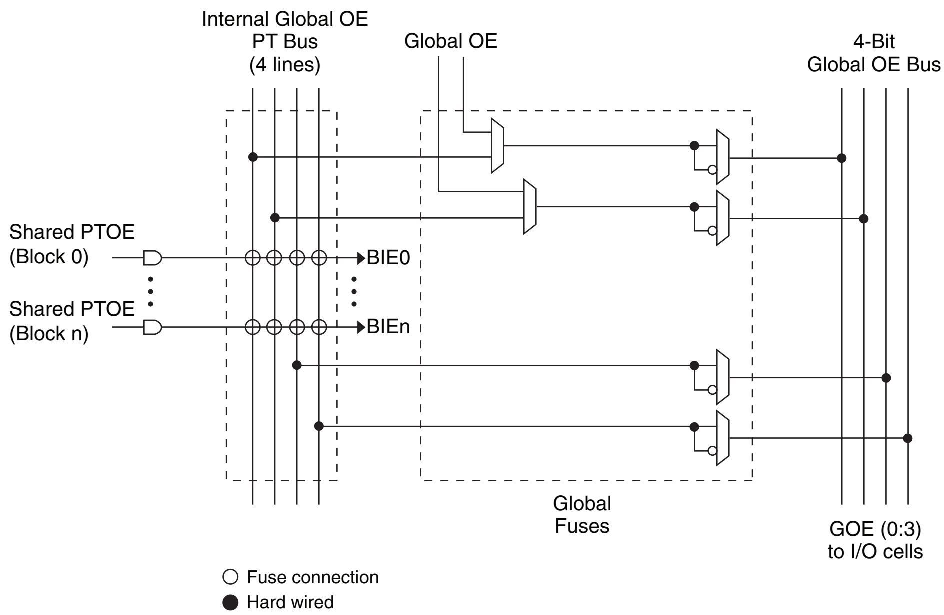
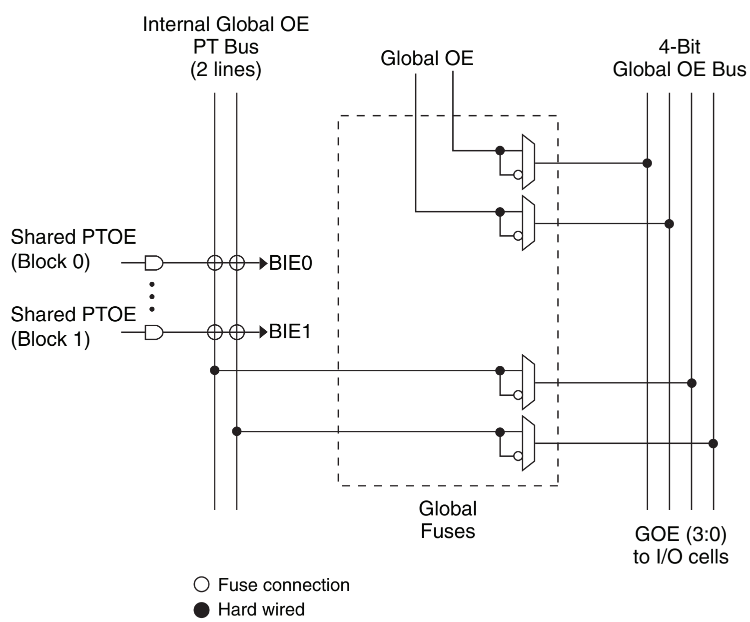



***Figure 12. Global OE Generation for ispMACH 4032ZE***




## On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

*Figure 13. On-Chip Oscillator and Timer*


*Table 11. On-Chip Oscillator and Timer Signal Names*

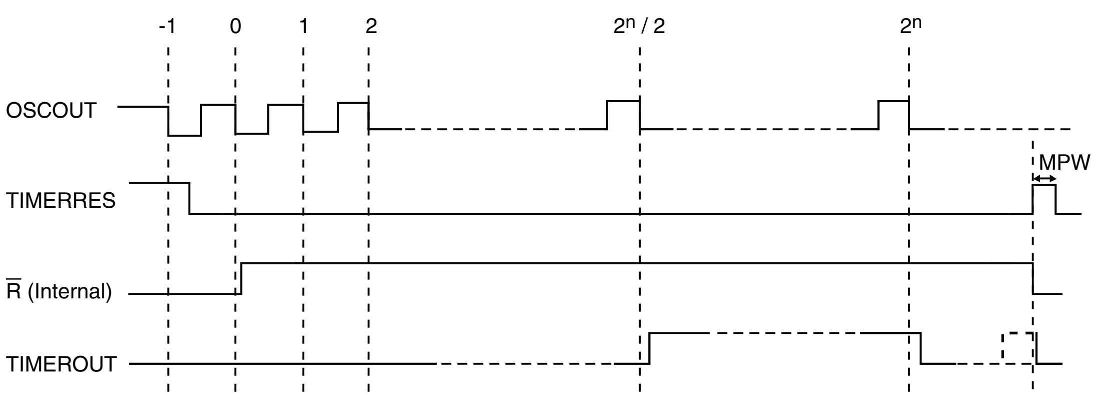
| Signal Name | Input or Output | Optional / Required | Description |
|---|---|---|---|
| OSCOUT | Output | Optional | Oscillator Output (Nominal Frequency: 5MHz) |
| TIMEROUT | Output | Optional | Oscillator Frequency Divided by an integer TIMER_DIV (Default 128) |
| TIMERRES | Input | Optional | Reset the Timer |
| DYNOSCDIS | Input | Optional | Disables the Oscillator, resets the Timer and saves the power. |

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER_DIV.

The attribute TIMER_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal "$\overline{R}$" is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

*Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT*




Note: n = Number of bits in the divider (7, 10 or 20)
Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

## User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in $E^2$CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

## Security Bit

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## Hot Socketing

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

## Density Migration

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

# I/O Recommended Operating Conditions

| Standard | $V_{CCO}$ (V)[1] | |
|---|---|---|
| | Min. | Max. |
| LVTTL | 3.0 | 3.6 |
| LVCMOS 3.3 | 3.0 | 3.6 |
| Extended LVCMOS 3.3 | 2.7 | 3.6 |
| LVCMOS 2.5 | 2.3 | 2.7 |
| LVCMOS 1.8 | 1.65 | 1.95 |
| LVCMOS 1.5 | 1.4 | 1.6 |
| PCI 3.3 | 3.0 | 3.6 |

1. Typical values for $V_{CCO}$ are the average of the min. and max. values.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2] | Input Leakage Current | $0 \le V_{IN} < V_{CCO}$ | — | 0.5 | 1 | µA |
| $I_{IH}$[1] | Input High Leakage Current | $V_{CCO} < V_{IN} \le 5.5V$ | — | — | 10 | µA |
| $I_{PU}$ | I/O Weak Pull-up Resistor Current | $0 \le V_{IN} \le 0.7V_{CCO}$ | -20 | — | -150 | µA |
| $I_{PD}$ | I/O Weak Pull-down Resistor Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 150 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCO}$ | -20 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0V \le V_{IN} \le V_{BHT}$ | — | — | 150 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $V_{BHT} \le V_{IN} \le V_{CCO}$ | — | — | -150 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | — | $V_{CCO}$ * 0.35 | — | $V_{CCO}$ * 0.65 | V |
| $C_1$ | I/O Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 8 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_2$ | Clock Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |
| $C_3$ | Global Input Capacitance[3] | $V_{CCO}$ = 3.3V, 2.5V, 1.8V, 1.5V | — | 6 | — | pf |
| | | $V_{CC}$ = 1.8V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | | — | |

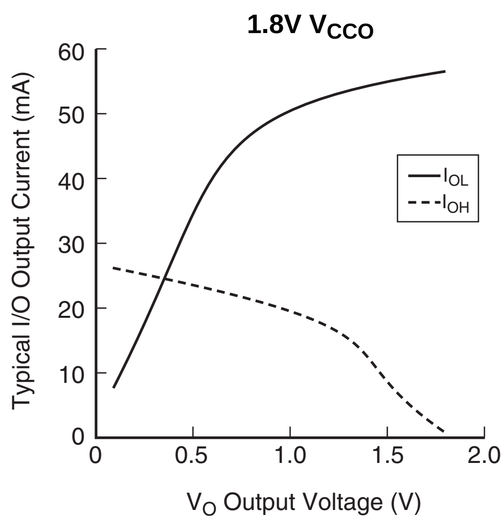
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $I_{IH}$ excursions of up to 1.5µA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured $T_A$ = 25°C, f = 1.0MHz.

# I/O DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Standard | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$ Max (V) | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| LVTTL | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 3.3 | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.70 | 1.70 | 3.6 | 0.40 | $V_{CCO}$ - 0.40 | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| LVCMOS 1.5[2] | -0.3 | 0.35 * $V_{CC}$ | 0.65 * $V_{CC}$ | 3.6 | 0.40 | $V_{CCO}$ - 0.45 | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO}$ - 0.20 | 0.1 | -0.1 |
| PCI 3.3 | -0.3 | 0.3 * 3.3 * ($V_{CC}$ / 1.8) | 0.5 * 3.3 * ($V_{CC}$ / 1.8) | 5.5 | 0.1 $V_{CCO}$ | 0.9 $V_{CCO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed *n**8mA. Where *n* is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from $V_{CC}$, if the ispMACH 4000ZE $V_{CC}$ and the $V_{CC}$ of the driving device ($V_{CC}$d-d; that determines steady state $V_{IH}$) are in the extreme range of their specifications. Typically, DC current drawn from $V_{CC}$ will be 2µA per input.



# ispMACH 4000ZE Internal Timing Parameters (Cont.)

**Over Recommended Operating Conditions**

| Parameter | Description | All Devices | | | | Units |
|---|---|---|---|---|---|---|
| | | -5 | | -7 | | |
| | | Min. | Max. | Min. | Max. | |
| **In/Out Delays** | | | | | | |
| $t_{IN}$ | Input Buffer Delay | — | 1.05 | — | 1.90 | ns |
| $t_{GCLK\_IN}$ | Global Clock Input Buffer Delay | — | 1.95 | — | 2.15 | ns |
| $t_{GOE}$ | Global OE Pin Delay | — | 3.00 | — | 4.30 | ns |
| $t_{BUF}$ | Delay through Output Buffer | — | 1.10 | — | 1.30 | ns |
| $t_{EN}$ | Output Enable Time | — | 2.50 | — | 2.70 | ns |
| $t_{DIS}$ | Output Disable Time | — | 2.50 | — | 2.70 | ns |
| $t_{PGSU}$ | Input Power Guard Setup Time | — | 4.30 | — | 5.60 | ns |
| $t_{PGH}$ | Input Power Guard Hold Time | — | 0.00 | — | 0.00 | ns |
| $t_{PGPW}$ | Input Power Guard BIE Minimum Pulse Width | — | 6.00 | — | 8.00 | ns |
| $t_{PGRT}$ | Input Power Guard Recovery Time Following BIE Dissertation | — | 5.00 | — | 7.00 | ns |
| **Routing Delays** | | | | | | |
| $t_{ROUTE}$ | Delay through GRP | — | 2.25 | — | 2.50 | ns |
| $t_{PDi}$ | Macrocell Propagation Delay | — | 0.45 | — | 0.50 | ns |
| $t_{MCELL}$ | Macrocell Delay | — | 0.65 | — | 1.00 | ns |
| $t_{INREG}$ | Input Buffer to Macrocell Register Delay | — | 1.00 | — | 1.00 | ns |
| $t_{FBK}$ | Internal Feedback Delay | — | 0.75 | — | 0.30 | ns |
| $t_{ORP}$ | Output Routing Pool Delay | — | 0.30 | — | 0.30 | ns |
| **Register/Latch Delays** | | | | | | |
| $t_S$ | D-Register Setup Time (Global Clock) | 0.90 | — | 1.25 | — | ns |
| $t_{S\_PT}$ | D-Register Setup Time (Product Term Clock) | 2.00 | — | 2.35 | — | ns |
| $t_H$ | D-Register Hold Time | 2.00 | — | 3.25 | — | ns |
| $t_{ST}$ | T-Register Setup Time (Global Clock) | 1.10 | — | 1.45 | — | ns |
| $t_{ST\_PT}$ | T-register Setup Time (Product Term Clock) | 2.20 | — | 2.65 | — | ns |
| $t_{HT}$ | T-Resister Hold Time | 2.00 | — | 3.25 | — | ns |
| $t_{SIR}$ | D-Input Register Setup Time (Global Clock) | 1.20 | — | 0.65 | — | ns |
| $t_{SIR\_PT}$ | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | ns |
| $t_{HIR}$ | D-Input Register Hold Time (Global Clock) | 1.40 | — | 2.05 | — | ns |
| $t_{HIR\_PT}$ | D-Input Register Hold Time (Product Term Clock) | 1.10 | — | 1.20 | — | ns |
| $t_{COi}$ | Register Clock to Output/Feedback MUX Time | — | 0.45 | — | 0.75 | ns |
| $t_{CES}$ | Clock Enable Setup Time | 2.00 | — | 2.00 | — | ns |
| $t_{CEH}$ | Clock Enable Hold Time | 0.00 | — | 0.00 | — | ns |
| $t_{SL}$ | Latch Setup Time (Global Clock) | 0.90 | — | 1.55 | — | ns |
| $t_{SL\_PT}$ | Latch Setup Time (Product Term Clock) | 2.00 | — | 2.05 | — | ns |
| $t_{HL}$ | Latch Hold Time | 2.00 | — | 1.17 | — | ns |
| $t_{GOi}$ | Latch Gate to Output/Feedback MUX Time | — | 0.35 | — | 0.33 | ns |
| $t_{PDLi}$ | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | ns |
| $t_{SRi}$ | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.95 | — | 0.28 | ns |

## Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

***Figure 17. Output Test Load, LVTTL and LVCMOS Standards***

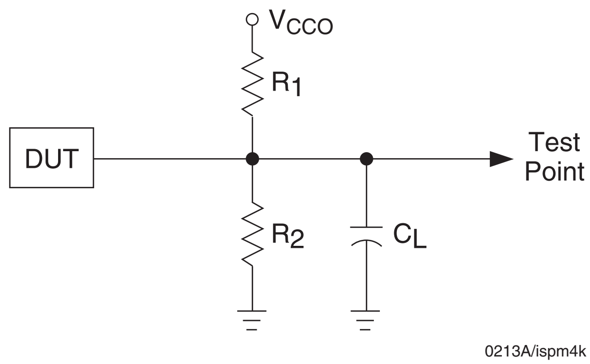



***Table 13. Test Fixture Required Components***

| Test Condition | $R_1$ | $R_2$ | $C_L$[1] | Timing Ref. | $V_{CCO}$ |
|---|---|---|---|---|---|
| LVCMOS I/O, (L -> H, H -> L) | 106Ω | 106Ω | 35pF | LVCMOS 3.3 = 1.5V | LVCMOS 3.3 = 3.0V |
| | | | | LVCMOS 2.5 = $\frac{V_{CCO}}{2}$ | LVCMOS 2.5 = 2.3V |
| | | | | LVCMOS 1.8 = $\frac{V_{CCO}}{2}$ | LVCMOS 1.8 = 1.65V |
| | | | | LVCMOS 1.5 = $\frac{V_{CCO}}{2}$ | LVCMOS 1.5 = 1.4V |
| LVCMOS I/O (Z -> H) | ∞ | 106Ω | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (Z -> L) | 106Ω | ∞ | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (H -> Z) | ∞ | 106Ω | 5pF | $V_{OH}$ - 0.3 | 3.0V |
| LVCMOS I/O (L -> Z) | 106Ω | ∞ | 5pF | $V_{OL}$ + 0.3 | 3.0V |

1. $C_L$ includes test fixtures and probe capacitance.

# ispMACH 4000ZE Power Supply and NC Connections[1]

| Signal | 48 TQFP[2] | 64 csBGA[3, 4] | 64 ucBGA[3, 4] | 100 TQFP[2] |
|---|---|---|---|---|
| VCC | 12, 36 | E4, D5 | E4, D5 | 25, 40, 75, 90 |
| VCCO0<br>VCCO (Bank 0) | 6 | **4032ZE:** E3<br>**4064ZE:** E3, F4 | C3, F3 | 13, 33, 95 |
| VCCO1<br>VCCO (Bank 1) | 30 | **4032ZE:** D6<br>**4064ZE:** D6, C6 | F6, A6 | 45, 63, 83 |
| GND | 13, 37 | D4, E5 | D4, D5 | 1, 26, 51, 76 |
| GND (Bank 0) | 5 | D4, E5 | D4, D5 | 7, 18, 32, 96 |
| GND (Bank 1) | 29 | D4, E5 | D4, D5 | 46, 57, 68, 82 |
| NC | — | — | — | — |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

## ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

| Pin Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | TDI | TDI |
| 2 | 0 | A5 | A8 |
| 3 | 0 | A6 | A10 |
| 4 | 0 | A7 | A11 |
| 5 | 0 | GND (Bank 0) | GND (Bank 0) |
| 6 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 7 | 0 | A8 | B15 |
| 8 | 0 | A9 | B12 |
| 9 | 0 | A10 | B10 |
| 10 | 0 | A11 | B8 |
| 11 | - | TCK | TCK |
| 12 | - | VCC | VCC |
| 13 | - | GND | GND |
| 14 | 0 | A12 | B6 |
| 15 | 0 | A13 | B4 |
| 16 | 0 | A14 | B2 |
| 17 | 0 | A15 | B0 |
| 18 | 0 | CLK1/I | CLK1/I |
| 19 | 1 | CLK2/I | CLK2/I |
| 20 | 1 | B0 | C0 |
| 21 | 1 | B1 | C1 |
| 22 | 1 | B2 | C2 |
| 23 | 1 | B3 | C4 |
| 24 | 1 | B4 | C6 |
| 25 | - | TMS | TMS |
| 26 | 1 | B5 | C8 |
| 27 | 1 | B6 | C10 |
| 28 | 1 | B7 | C11 |
| 29 | 1 | GND (Bank 1) | GND (Bank 1) |
| 30 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 31 | 1 | B8 | D15 |
| 32 | 1 | B9 | D12 |
| 33 | 1 | B10 | D10 |
| 34 | 1 | B11 | D8 |
| 35 | - | TDO | TDO |
| 36 | - | VCC | VCC |
| 37 | - | GND | GND |
| 38 | 1 | B12 | D6 |
| 39 | 1 | B13 | D4 |
| 40 | 1 | B14 | D2 |
| 41 | 1 | B15/GOE1 | D0/GOE1 |
| 42 | 1 | CLK3/I | CLK3/I |

## ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 43 | 0 | CLK0/I | CLK0/I |
| 44 | 0 | A0/GOE0 | A0/GOE0 |
| 45 | 0 | A1 | A1 |
| 46 | 0 | A2 | A2 |
| 47 | 0 | A3 | A4 |
| 48 | 0 | A4 | A6 |

## ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA (Cont.)

| Ball Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| E7 | 1 | NC | D14 |
| E6 | 1 | B9 | D13 |
| D7 | 1 | B10 | D12 |
| D8 | 1 | NC | D11 |
| C5 | 1 | NC | D10 |
| C7 | 1 | B11 | D9 |
| C8 | 1 | NC | D8 |
| B8 | - | TDO | TDO |
| D5 | - | VCC | VCC |
| GND* | - | GND | GND |
| A8 | 1 | B12 | D7 |
| A7 | 1 | NC | D6 |
| B7 | 1 | NC | D5 |
| A6 | 1 | B13 | D4 |
| GND* | 1 | NC | GND (Bank 1) |
| C6 | 1 | NC | VCCO (Bank 1) |
| B6 | 1 | B14 | D3 |
| A5 | 1 | NC | D2 |
| B5 | 1 | B15/GOE1 | D0/GOE1 |
| A4 | 1 | CLK3/I | CLK3/I |
| C4 | 0 | CLK0/I | CLK0/I |
| B4 | 0 | A0/GOE0 | A0/GOE0 |
| B3 | 0 | A1 | A1 |
| A3 | 0 | A2 | A2 |
| A2 | 0 | A3 | A4 |
| A1 | 0 | A4 | A6 |

* All bonded grounds are connected to the following two balls, D4 and E5.

## ispMACH 4064ZE Logic Signal Connections: 64 ucBGA

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| A1 | - | TDI |
| B1 | 0 | A8 |
| B2 | 0 | A10 |
| B3 | 0 | A11 |
| GND* | 0 | GND (Bank 0) |
| C1 | 0 | A12 |
| C3 | 0 | VCCO (Bank 0) |
| C2 | 0 | B15 |
| D1 | 0 | B14 |
| D2 | 0 | B13 |
| D3 | 0 | B12 |
| E1 | 0 | B11 |
| E2 | 0 | B10 |
| E3 | 0 | B9 |
| F1 | 0 | B8 |
| F2 | - | TCK |
| E4 | - | VCC |
| GND* | - | GND |
| H2 | 0 | B6 |
| H1 | 0 | B5 |
| G1 | 0 | B4 |
| GND* | 0 | GND (Bank 0) |
| F3 | 0 | VCCO (Bank 0) |
| G2 | 0 | B3 |
| G3 | 0 | B2 |
| H3 | 0 | B0 |
| G4 | 0 | CLK1/I |
| F4 | 1 | CLK2/I |
| H4 | 1 | C0 |
| H5 | 1 | C1 |
| G5 | 1 | C2 |
| H6 | 1 | C4 |
| H7 | 1 | C5 |
| H8 | 1 | C6 |
| G8 | - | TMS |
| G7 | 1 | C8 |
| G6 | 1 | C10 |
| F8 | 1 | C11 |
| GND* | 1 | GND (Bank 1) |
| F7 | 1 | C12 |
| F6 | 1 | VCCO (Bank 1) |
| F5 | 1 | D15 |
| E8 | 1 | D14 |

# ispMACH 4128ZE Logic Signal Connections: 132 ucBGA (Cont.)

| Ball Number | Bank Number | GLB/MC/Pad |
|---|---|---|
| M5 | 0 | D5 |
| J6 | 0 | D4 |
| K6 | 0 | D2 |
| L6 | 0 | D1 |
| M6 | 0 | D0 |
| K7 | 0 | CLK1/I |
| L7 | 1 | GND (Bank 1) |
| J7 | 1 | CLK2/I |
| M7 | - | VCC |
| K8 | 1 | E0 |
| L8 | 1 | E1 |
| M8 | 1 | E2 |
| J8 | 1 | E4 |
| L9 | 1 | E5 |
| M9 | 1 | E6 |
| K9 | 1 | VCCO (Bank 1) |
| J9 | 1 | GND (Bank 1) |
| L10 | 1 | E8 |
| K10 | 1 | E9 |
| M10 | 1 | E10 |
| L11 | 1 | E12 |
| K12 | 1 | E13 |
| M11 | 1 | E14 |
| GND* | - | GND |
| M12 | - | TMS |
| L12 | 1 | VCCO (Bank 1) |
| K11 | 1 | F0 |
| J10 | 1 | F1 |
| H9 | 1 | F2 |
| J12 | 1 | F4 |
| J11 | 1 | F5 |
| H10 | 1 | F6 |
| H12 | 1 | GND (Bank 1) |
| G9 | 1 | F8 |
| H11 | 1 | F9 |
| F9 | 1 | F10 |
| G12 | 1 | F12 |
| G11 | 1 | F13 |
| G10 | 1 | F14 |
| F12 | 1 | VCCO (Bank 1) |
| F10 | 1 | G14 |
| F11 | 1 | G13 |
| E11 | 1 | G12 |
| E10 | 1 | G10 |

# ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections: 144 csBGA (Cont.)

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|---|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| J4 | 0 | B7 | D12 | G6 |
| K4 | 0 | B6 | D10 | G4 |
| M3 | 0 | B5 | D9 | G2 |
| L4 | 0 | B4 | D8 | G0 |
| H6 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| J5 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| M4 | 0 | NC Ball | D6 | H12 |
| L5 | 0 | NC Ball | D5 | H10 |
| K5 | 0 | B3 | D4 | H8 |
| J6 | 0 | B2 | D2 | H6 |
| M5 | 0 | B1 | D1 | H4 |
| K6 | 0 | B0 | D0 | H2 |
| L6 | 0 | CLK1/I | CLK1/I | CLK1/I |
| H7 | 1 | NC Ball | GND (Bank 1) | GND (Bank 1) |
| M6 | 1 | CLK2/I | CLK2/I | CLK2/I |
| H8 | - | VCC | VCC | VCC |
| K7 | 1 | C0 | E0 | I2 |
| M7 | 1 | C1 | E1 | I4 |
| L7 | 1 | C2 | E2 | I6 |
| J7 | 1 | C3 | E4 | I8 |
| L8 | 1 | NC Ball | E5 | I10 |
| M8 | 1 | NC Ball | E6 | I12 |
| J8 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| J9 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| M9 | 1 | C4 | E8 | J2 |
| L9 | 1 | C5 | E9 | J4 |
| K8 | 1 | C6 | E10 | J6 |
| M10 | 1 | C7 | E12 | J8 |
| L10 | 1 | NC Ball | E13 | J10 |
| K9 | 1 | NC Ball | E14 | J12 |
| M11 | 1 | NC Ball | NC Ball | J14 |
| G7 | - | GND | GND | GND |
| M12 | - | TMS | TMS | TMS |
| H9 | 1 | NC Ball | VCCO (Bank 1) | VCCO (Bank 1) |
| L12 | 1 | NC Ball | F0 | K12 |
| L11 | 1 | NC Ball | F1 | K10 |
| K10 | 1 | C8 | F2 | K8 |
| K12 | 1 | C9 | F4 | K6 |
| J10 | 1 | C10 | F5 | K4 |
| K11 | 1 | C11 | F6 | K2 |
| G8 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |

# ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|---|---|---|---|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 129 | - | VCC | VCC |
| 130 | 0 | A0/GOE0 | A2/GOE0 |
| 131 | 0 | A1 | A4 |
| 132 | 0 | A2 | A6 |
| 133 | 0 | A4 | A8 |
| 134 | 0 | A5 | A10 |
| 135 | 0 | A6 | A12 |
| 136 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 137 | 0 | GND (Bank 0) | GND (Bank 0) |
| 138 | 0 | A8 | B2 |
| 139 | 0 | A9 | B4 |
| 140 | 0 | A10 | B6 |
| 141 | 0 | A12 | B8 |
| 142 | 0 | A13 | B10 |
| 143 | 0 | A14 | B12 |
| 144* | 0 | NC | I |

* This pin is input only for the LC4256ZE.

**Industrial**

| Device | Part Number | Macrocells | Voltage | $t_{PD}$ | Package | Pin/Ball Count | I/O | Grade |
|---|---|---|---|---|---|---|---|---|
| LC4032ZE | LC4032ZE-5TN48I | 32 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-7TN48I | 32 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-5MN64I | 32 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 32 | I |
| | LC4032ZE-7MN64I | 32 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 32 | I |
| LC4064ZE | LC4064ZE-5TN48I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-7TN48I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-5TN100I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-7TN100I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-5MN64I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-7MN64I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-5UMN64I | 64 | 1.8 | 5.8 | Lead-Free ucBGA | 64 | 48 | I |
| | LC4064ZE-7UMN64I | 64 | 1.8 | 7.5 | Lead-Free ucBGA | 64 | 48 | I |
| | LC4064ZE-5MN144I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 64 | I |
| | LC4064ZE-7MN144I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 64 | I |
| LC4128ZE | LC4128ZE-7TN100I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4128ZE-7UMN132I | 128 | 1.8 | 7.5 | Lead-Free ucBGA | 132 | 96 | I |
| | LC4128ZE-7TN144I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4128ZE-7MN144I | 128 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 96 | I |
| LC4256ZE | LC4256ZE-7TN100I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4256ZE-7TN144I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4256ZE-7MN144I | 256 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 108 | I |

1. Contact factory for product availability.

## For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168, ispMACH 4000ZE Timing Model Design and Usage Guidelines
- TN1174, Advanced Features of the ispMACH 4000ZE Family
- TN1187, Power Estimation in ispMACH 4000ZE Devices
- Package Diagrams

## Technical Support Assistance

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# Revision History

| Date | Version | Change Summary |
|---|---|---|
| April 2008 | 01.0 | Initial release. |
| July 2008 | 01.1 | Updated Features bullets. |
| | | Updated typical Hysteresis voltage. |
| | | Updated Power Guard for Dedicated Inputs section. |
| | | Updated DC Electrical Characteristics table. |
| | | Updated Supply Current table. |
| | | Updated I/O DC Electrical Characteristics table and note 2. |
| | | Updated ispMACH 4000ZE Timing Model. |
| | | Added new parameters for the Internal Oscillator. |
| | | Updated ORP Reference table. |
| | | Updated Power Supply and NC Connections table. |
| | | Updated 100 TQFP Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Updated 144 csBGA Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Added 144 TQFP Logic Signal Connections table. |
| August 2008 | 01.2 | Data sheet status changed from advance to final. |
| | | Updated Supply Current table. |
| | | Updated External Switching Characteristics. |
| | | Updated Internal Timing Parameters. |
| | | Updated Power Consumption graph and Power Estimation Coefficients table. |
| | | Updated Ordering Information mark format example. |
| December 2008 | 01.3 | Updated ispMACH 4000ZE Family Selection Guide table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated ispMACH 4000ZE Power Supply and NC Connections table to include 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Added Logic Signal Connections tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Part Number Description diagram for 64-ball ucBGA and 132-ball ucBGA packages. |
| | | Updated Ordering Information tables for 64-ball ucBGA and 132-ball ucBGA packages. |
| May 2009 | 01.4 | Correction to $t_{CW}$, $t_{GW}$, $t_{WIR}$ and $f_{MAX}$ parameters in External Switching Characteristics table. |
| June 2011 | 01.5 | Added copper bond package part numbers. |
| | | Added footnote 4 to Absolute Maximum Ratings. |
| February 2012 | 01.6 | Updated document with new corporate logo. |
| February 2012 | 01.7 | Removed copper bond packaging information. Refer to PCN 04A-12 for further information. |
| | | Updated topside marks with new logos in the Ordering Information section. |