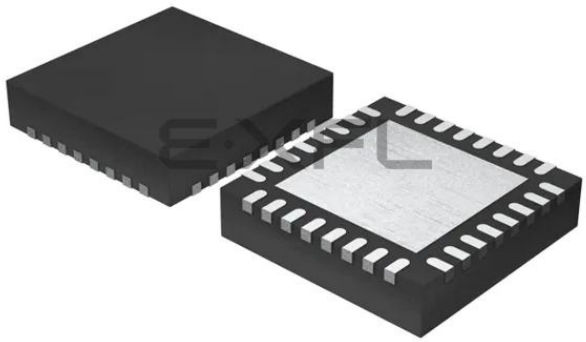

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b120f128im32-a

1. Feature List

The EFM32TG11 highlighted features are listed below.

- **ARM Cortex-M0+ CPU platform**
  - High performance 32-bit processor @ up to 48 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 37 µA/MHz in Active Mode (EM0)
  - 1.30 µA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power absent/ insufficient
- **Up to 128 kB flash program memory**
- **Up to 32 kB RAM data memory**
- **Communication Interfaces**
  - CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (24 MHz) operation on one instance
  - 1 × Universal Asynchronous Receiver/ Transmitter
  - 1 × Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2 × I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 67 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 8 Channel DMA Controller**
- **Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 × 32 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Up to 2 × Analog Comparator (ACMP)
  - Up to 4 × Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
  - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

- **Timers/Counters**
  - 2 × 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
    - Dead-Time Insertion on one timer instance
  - 2 × 32-bit Timer/Counter
  - 32-bit Real Time Counter and Calendar (RTCC)
  - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
  - 16-bit Low Energy Timer for waveform generation
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
  - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 4-pin JTAG interface
  - Micro Trace Buffer (MTB)
- **Pre-Programmed UART Bootloader**
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_A) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - QFN32 (5x5 mm)
  - TQFP48 (7x7 mm)
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - QFN80 (9x9 mm)
  - TQFP80 (12x12 mm)

Table of Contents

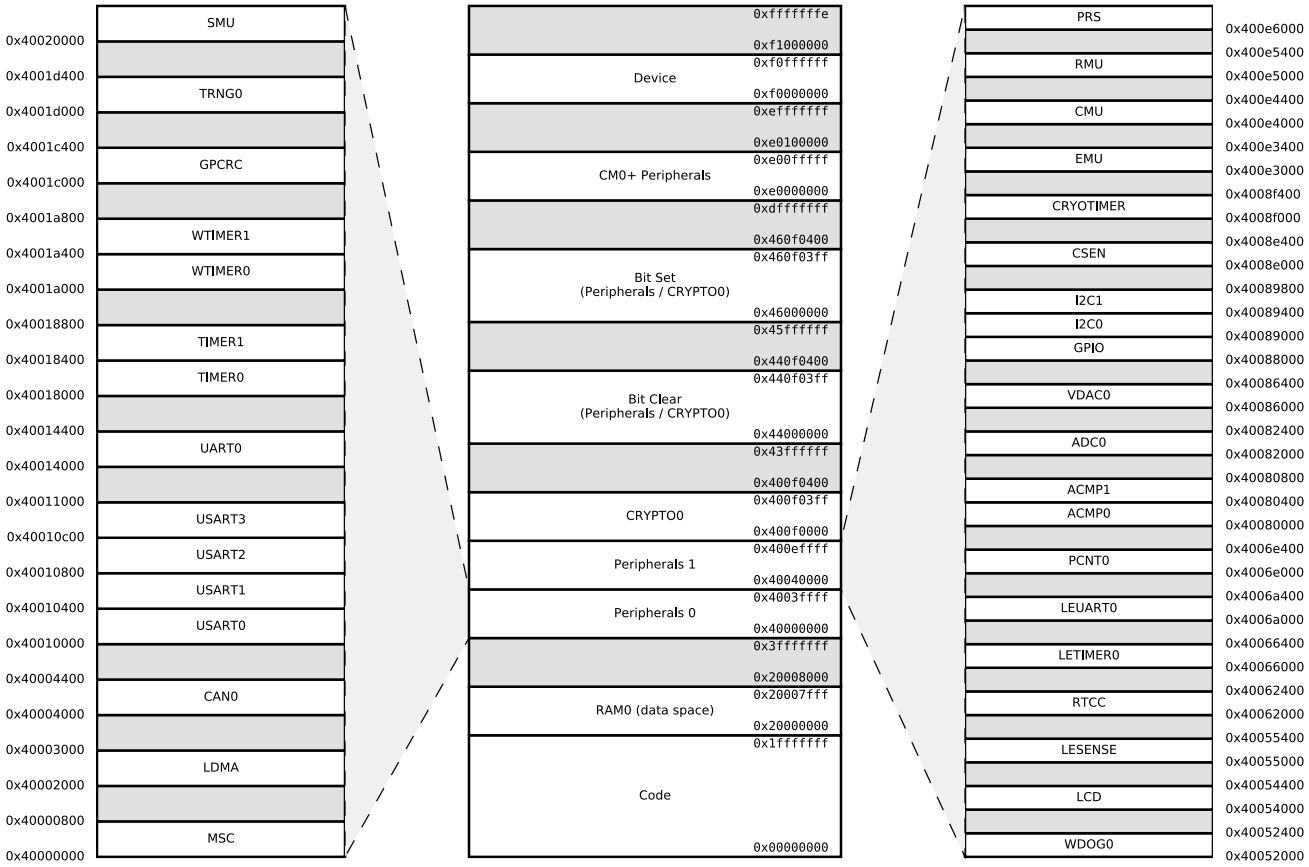

Figure 3.3. EFM32TG11 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32TG11 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA, SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S, SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA, SmartCard, High-Speed	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	I^2S, SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	f_{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f_{HFRCO} < 19 MHz	—	1	—	µs
		f_{HFRCO} ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 48 MHz	—	258	TBD	µA
		f_{HFRCO} = 38 MHz	—	218	TBD	µA
		f_{HFRCO} = 32 MHz	—	182	TBD	µA
		f_{HFRCO} = 26 MHz	—	156	TBD	µA
		f_{HFRCO} = 19 MHz	—	130	TBD	µA
		f_{HFRCO} = 16 MHz	—	112	TBD	µA
		f_{HFRCO} = 13 MHz	—	101	TBD	µA
		f_{HFRCO} = 7 MHz	—	80	TBD	µA
		f_{HFRCO} = 4 MHz	—	29	TBD	µA
		f_{HFRCO} = 2 MHz	—	26	TBD	µA
		f_{HFRCO} = 1 MHz	—	24	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	393	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	313	TBD	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	180	TBD	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	46	TBD	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	33	TBD	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	TBD	—	TBD	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

4.1.21.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.30. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

SPI Slave Timing

Table 4.32. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [3] [2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [3] [2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		20	—	70	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		15	—	150	ns
MOSI setup time [1] [3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		7	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		14 + 1.5 * $t_{HFPERCLK}$	—	40 + 2.5 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

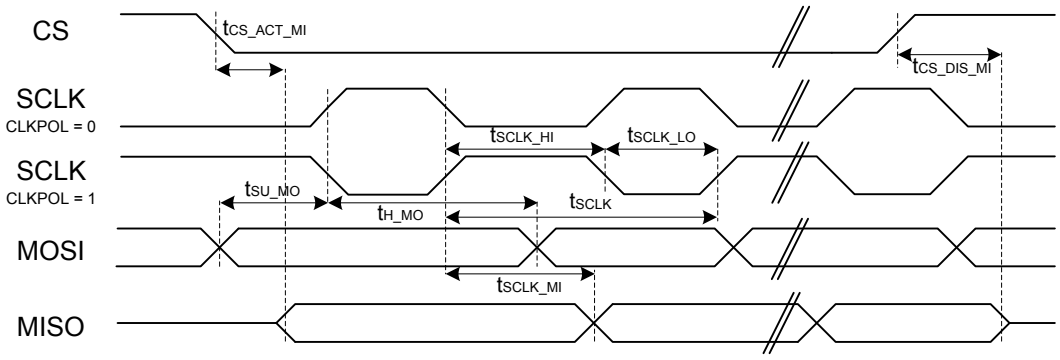

Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

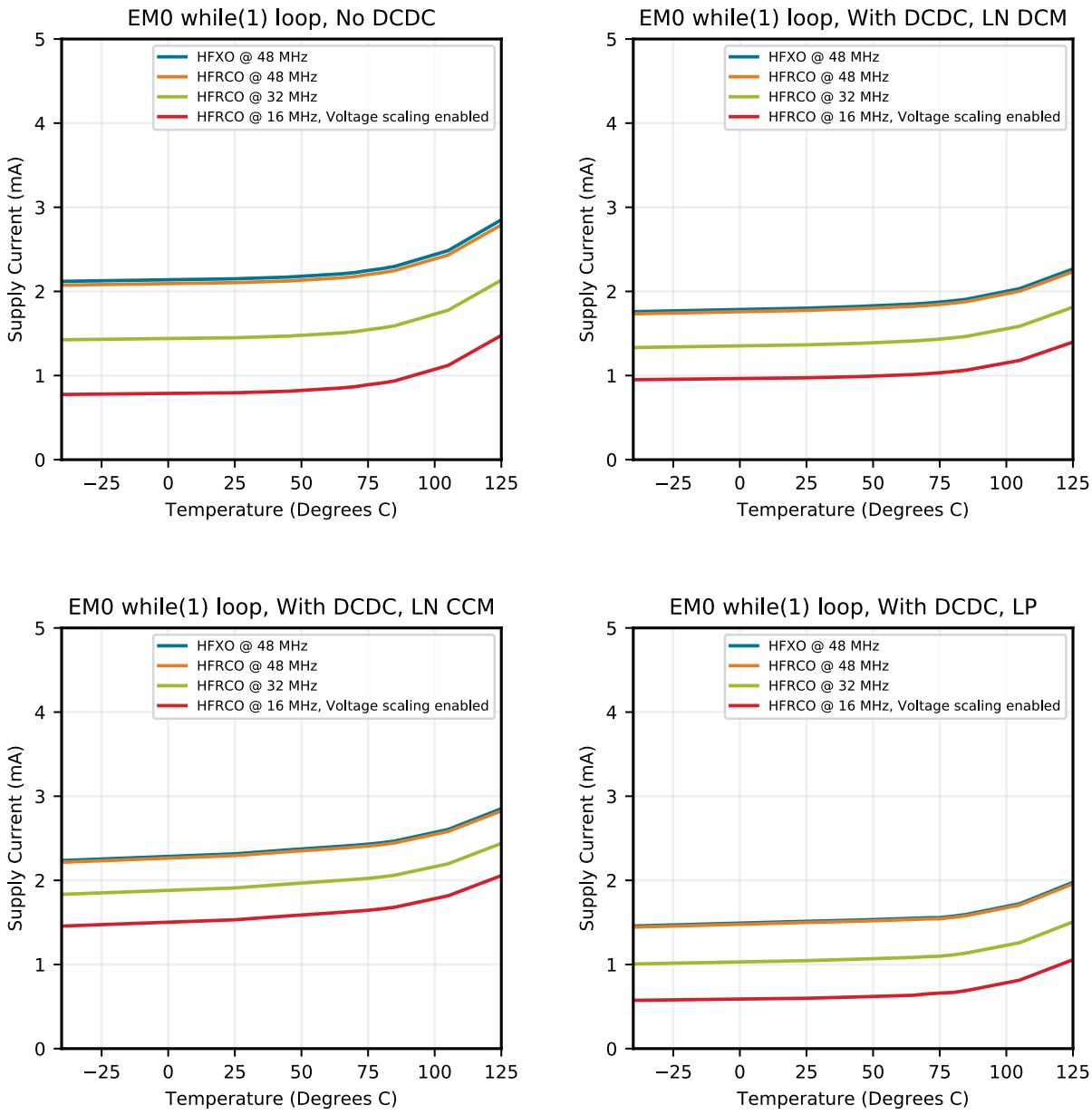

Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

5.3 EFM32TG11B5xx in QFP64 Device Pinout

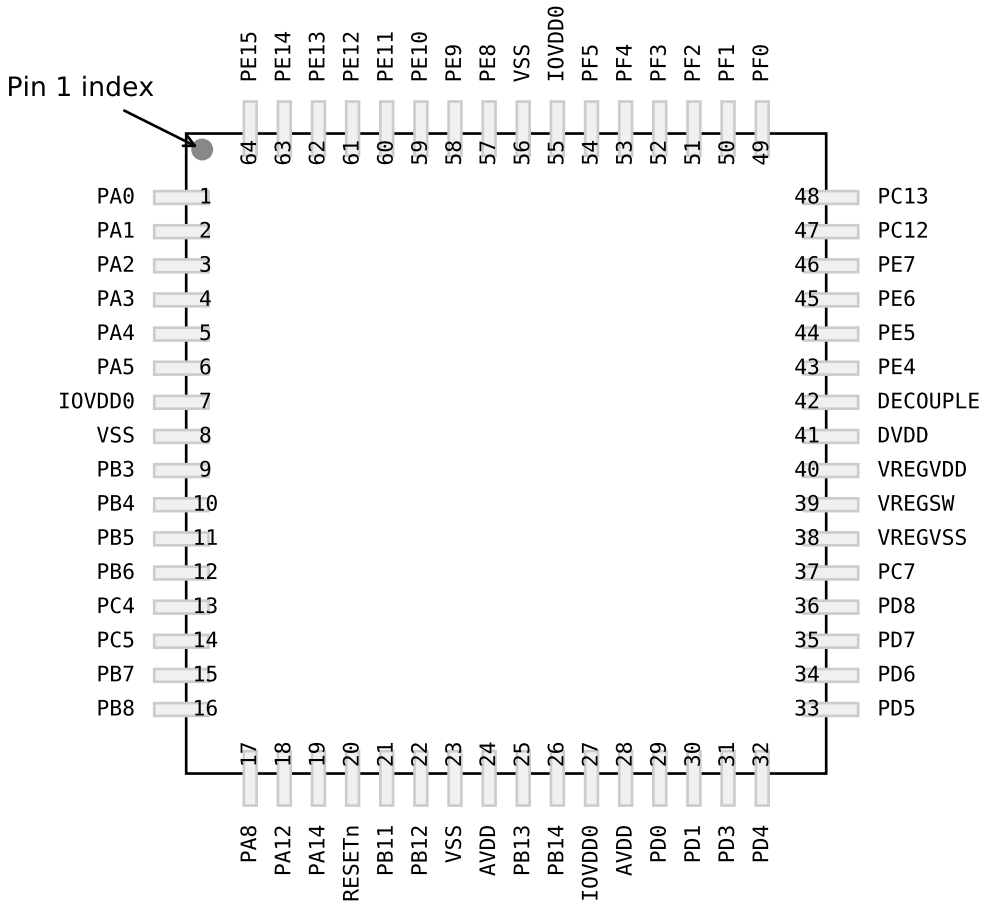

Figure 5.3. EFM32TG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.3. EFM32TG11B5xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.12 EFM32TG11B5xx in QFN32 Device Pinout

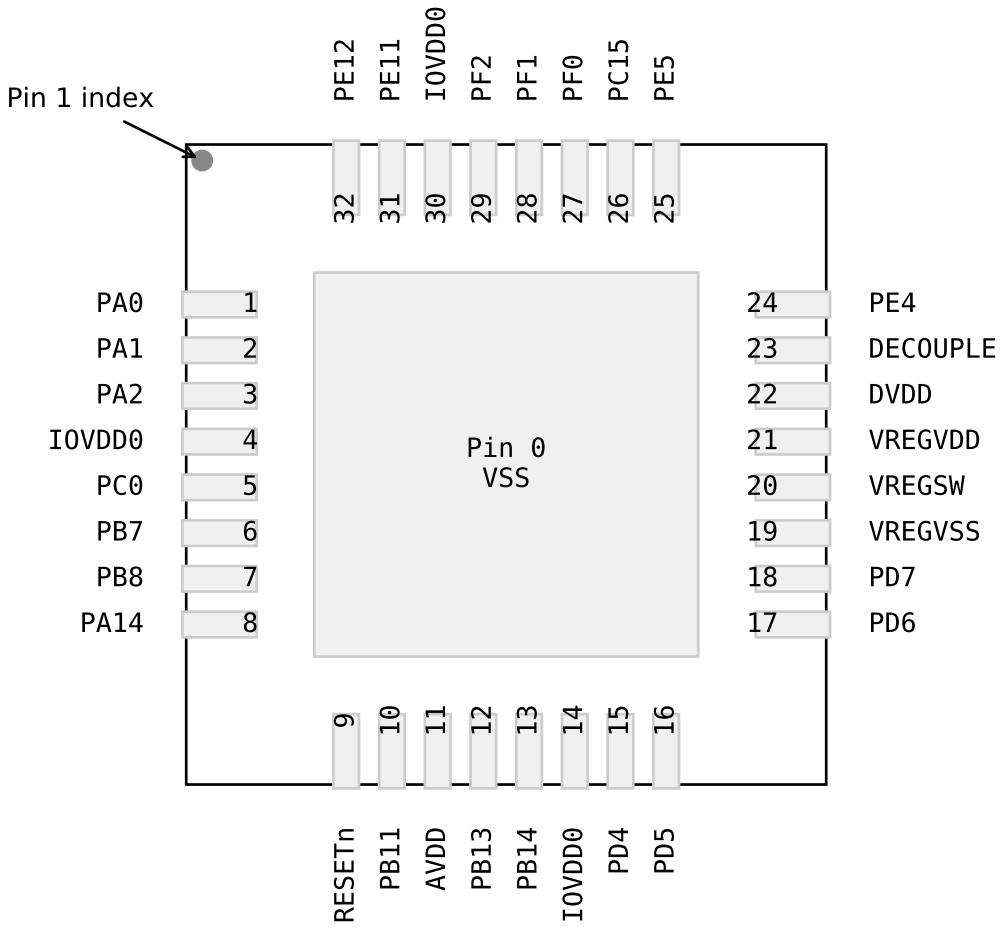

Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

5.13 EFM32TG11B1xx in QFN32 Device Pinout

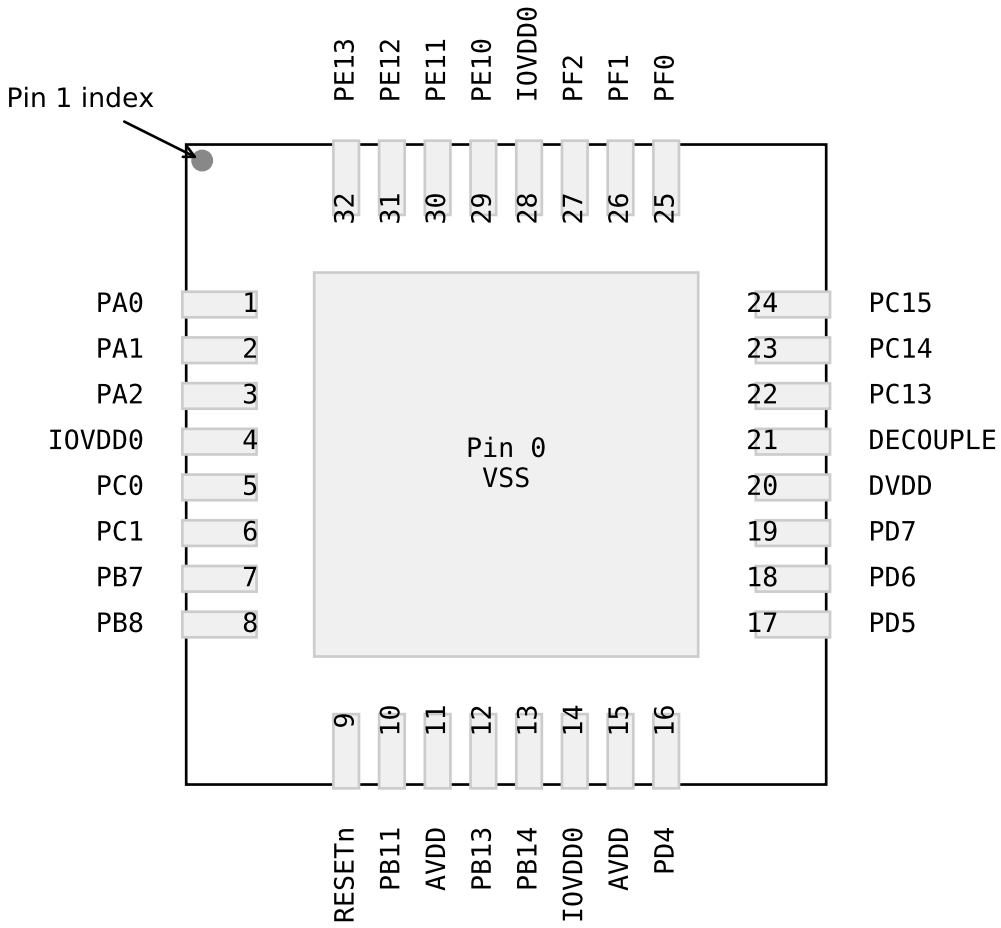

Figure 5.13. EFM32TG11B1xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.13. EFM32TG11B1xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 28	Digital IO power supply 0.	PC0	5	GPIO (5V)
PC1	6	GPIO (5V)	PB7	7	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.
LCD_SEG7	0: PE11		LCD segment line 7.
LCD_SEG8	0: PE12		LCD segment line 8.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG35	0: PC9		LCD segment line 35.
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM0_CC0	0: PA0 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 2: PD3 3: PC1	4: PF2 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 3: PB7	4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 3: PB8	4: PD7 5: PF3	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 3: PB11	4: PC13 5: PF4	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 6: PF5	Timer 1 Capture Compare input / output channel 3.
U0_CTS	 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 8.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 TQFP64 Package Marking

Figure 8.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 9.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions