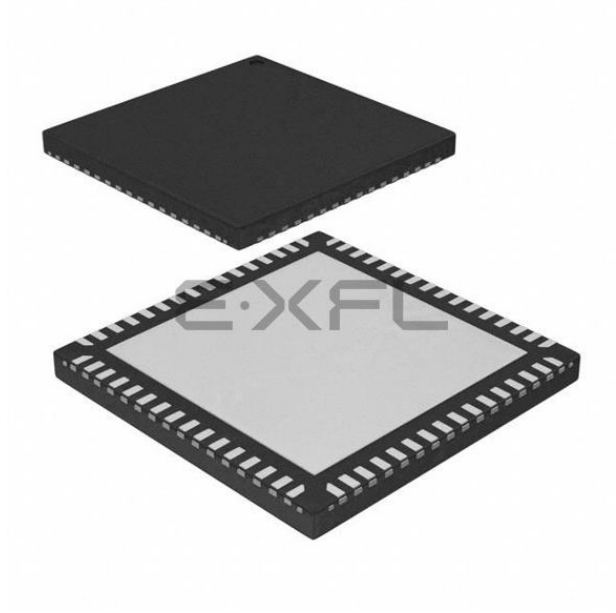

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  - TQFP48 (7x7 mm)
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - QFN80 (9x9 mm)
  - TQFP80 (12x12 mm)

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[6]	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage[2]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[2] [1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins[5]	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[3] [4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS1	—	—	48	MHz
		VSCALE2, MODE = WS0	—	—	25	MHz
		VSCALE0, MODE = WS1	—	—	20	MHz
		VSCALE0, MODE = WS0	—	—	10	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	—	°C/W
Thermal resistance, TQFP48 Package	$THETA_{JA\_TQFP48}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	43.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	—	°C/W
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	37.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	35.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	—	°C/W
Thermal resistance, QFN80 Package	$THETA_{JA\_QFN80}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP80 Package	$THETA_{JA\_TQFP80}$	4-Layer PCB, Air velocity = 0 m/s	—	49.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	44.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.6	—	°C/W

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive[2], T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 µF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 µF. See Application Note AN0948 for details.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1147	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	30	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	144	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	48 MHz crystal	—	31	—	µA/MHz
		48 MHz HFRCO	—	30	—	µA/MHz
		32 MHz HFRCO	—	36	—	µA/MHz
		26 MHz HFRCO	—	41	—	µA/MHz
		16 MHz HFRCO	—	54	—	µA/MHz
		1 MHz HFRCO	—	581	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	25	—	µA/MHz
		26 MHz HFRCO	—	26	—	µA/MHz
		16 MHz HFRCO	—	29	—	µA/MHz
		1 MHz HFRCO	—	153	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	46	—	µA/MHz
		1 MHz HFRCO	—	573	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	25	—	µA/MHz
		1 MHz HFRCO	—	140	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 32 kB RAM retention and RTCC running from LFXO	—	1.26	—	µA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.54	—	µA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	1.30	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	0.93	—	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.78	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.50	—	µA
		128 byte RAM retention, no RTCC	—	0.50	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.06	—	µA

4.1.14 Analog Comparator (ACMP)

Table 4.21. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG[4] ≤ 0x10 or FULLBIAS[4] = 0	1.8	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[4] ≤ 0x20 and FULLBIAS[4] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference[2]	I_{ACMP}	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	50	—	nA
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	306	—	nA
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	6.5	—	µA
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	74	TBD	µA
Current consumption of internal voltage reference[2]	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

4.1.17 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[8] [1].

Table 4.24. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage (from AVDD)	V_{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V_{IN}	HCMDIS = 0, Rail-to-rail input range	V_{VSS}	—	V_{OPA}	V
		HCMDIS = 1	V_{VSS}	—	V_{OPA}-1.2	V
Input impedance	R_{IN}		100	—	—	MΩ
Output voltage	V_{OUT}		V_{VSS}	—	V_{OPA}	V
Load capacitance[2]	C_{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R_{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G_{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current[4]	I_{OPA}	DRIVESTRENGTH = 3, OUTSCALE = 0	—	580	—	µA
		DRIVESTRENGTH = 2, OUTSCALE = 0	—	176	—	µA
		DRIVESTRENGTH = 1, OUTSCALE = 0	—	13	—	µA
		DRIVESTRENGTH = 0, OUTSCALE = 0	—	4.7	—	µA

4.1.21.2 I2C Fast-mode (Fm)[1]

Table 4.29. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

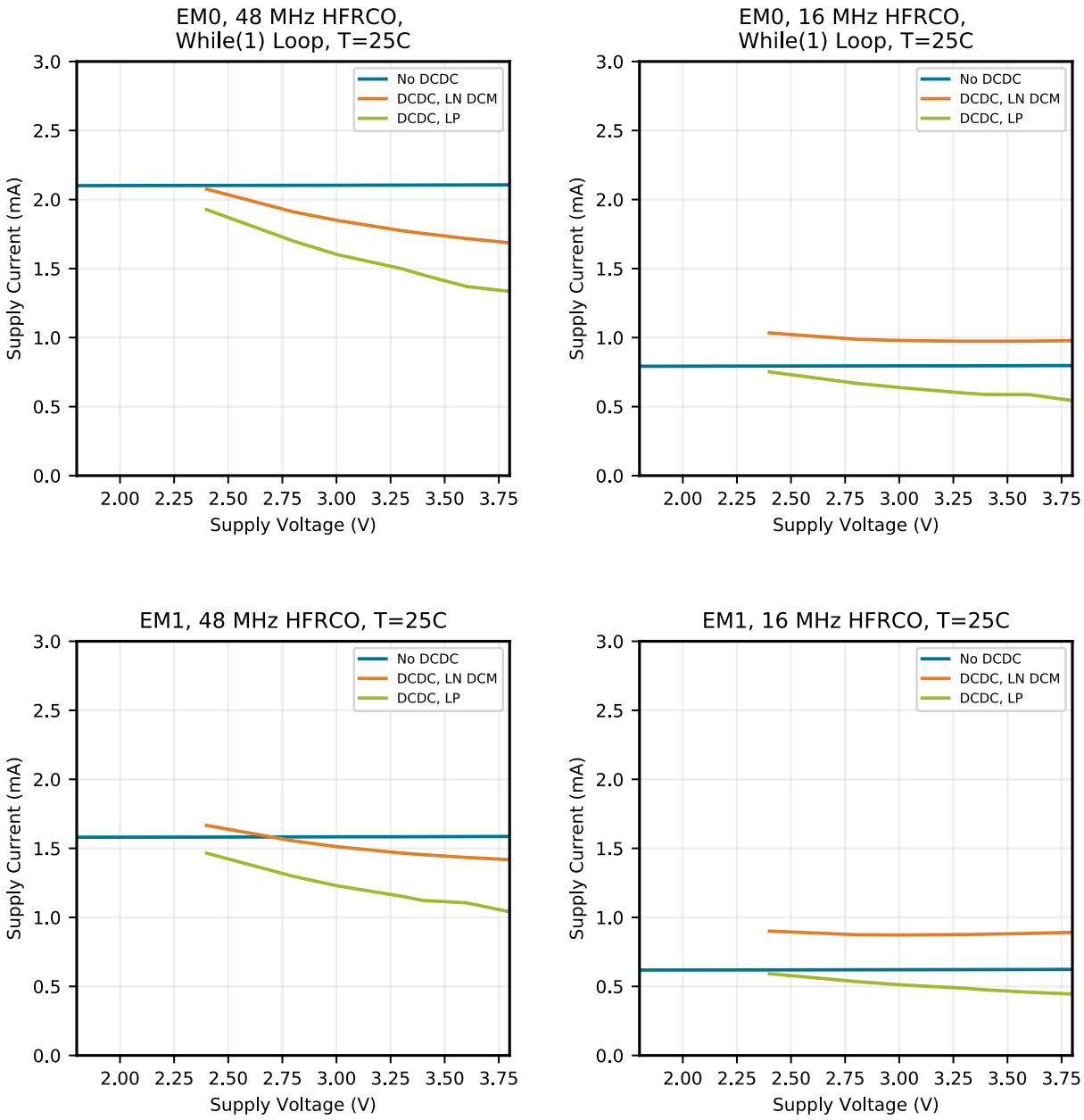

Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	11	GPIO	PA8	12	GPIO
PA12	13	GPIO	PA14	14	GPIO
RESETn	15	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	16	GPIO
AVDD	18 22	Analog power supply.	PB13	19	GPIO
PB14	20	GPIO	PD4	23	GPIO
PD5	24	GPIO	PD6	25	GPIO
PD7	26	GPIO	PD8	27	GPIO
VREGVSS	28	Voltage regulator VSS	VREGSW	29	DCDC regulator switching node
VREGVDD	30	Voltage regulator VDD input	DVDD	31	Digital power supply.
DECOUPLE	32	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	33	GPIO
PE5	34	GPIO	PE6	35	GPIO
PE7	36	GPIO	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.12 EFM32TG11B5xx in QFN32 Device Pinout

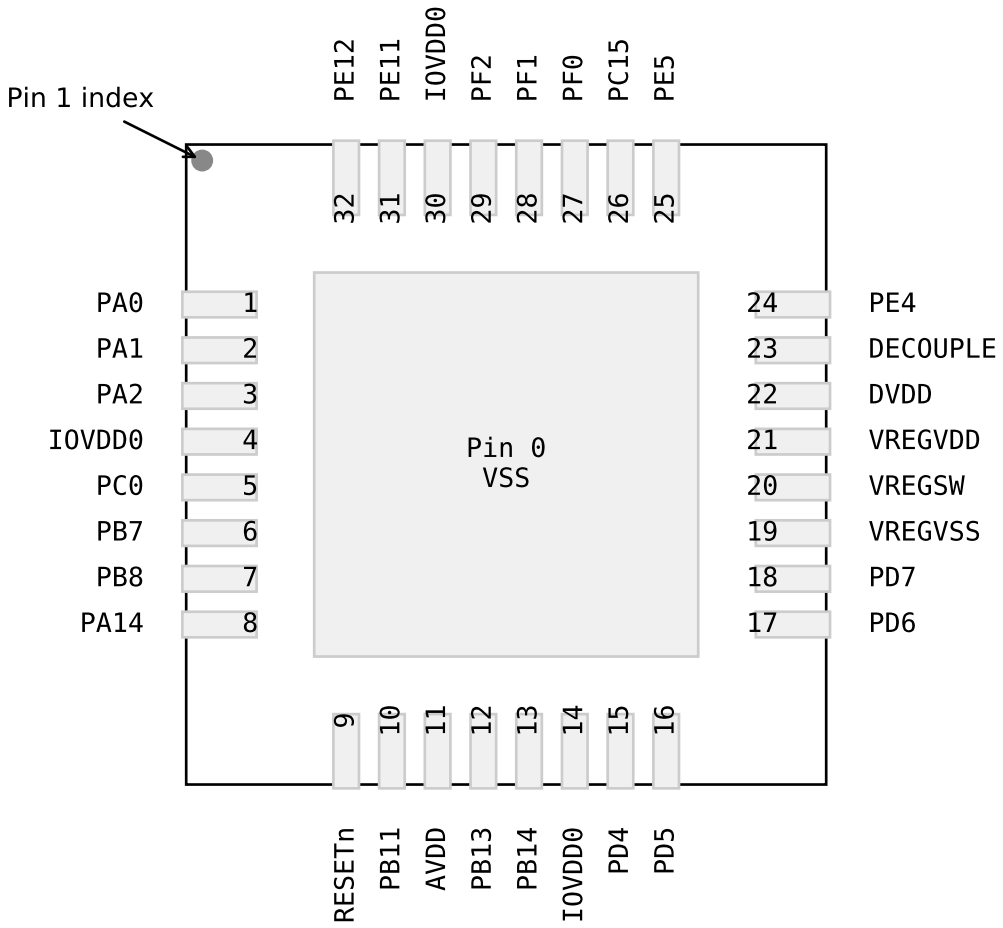

Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

5.14 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.15 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.14. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PA0	BUSBY BUSAX LCD_SEG13	TIM0_CC0 #0 TIM0_CC1 #7 PCNT0_S0IN #4	US1_RX #5 US3_TX #0 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PA1	BUSAY BUSBX LCD_SEG14	TIM0_CC0 #7 TIM0_CC1 #0 PCNT0_S1IN #4	US3_RX #0 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PA2	BUSBY BUSAX LCD_SEG15	TIM0_CC2 #0	US1_RX #6 US3_CLK #0	CMU_CLK0 #0
PA3	BUSAY BUSBX LCD_SEG16	TIM0_CDTI0 #0	US3_CS #0 U0_TX #2	CMU_CLK2 #1 CMU_CLK2 #4 CMU_CLKI0 #1 LES_ALTEX2
PA4	BUSBY BUSAX LCD_SEG17	TIM0_CDTI1 #0	US3_CTS #0 U0_RX #2	LES_ALTEX3
PA5	BUSAY BUSBX LCD_SEG18	TIM0_CDTI2 #0	US3_RTS #0 U0_CTS #2	LES_ALTEX4 ACMP1_O #7
PA6	BUSBY BUSAX LCD_SEG19	WTIM0_CC0 #1	U0_RTS #2	PRS_CH6 #0 ACMP0_O #4 GPIO_EM4WU1
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	TIM1_CC3 #2 WTIM0_CC0 #6	US2_TX #1 US3_TX #2	ACMP0_O #7
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	WTIM0_CC1 #6	US2_RX #1	
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	WTIM0_CC2 #6 PCNT0_S0IN #6	US0_RTS #4 US2_CLK #1	
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	TIM0_CC0 #3 PCNT0_S1IN #6	US0_CTS #4 US2_CS #1	
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	TIM0_CC1 #3 PCNT0_S0IN #2	CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	TIM0_CC2 #3 WTIM0_CC0 #7 PCNT0_S1IN #2	CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	TIM0_CDTI0 #3 WTIM0_CC1 #7	US1_RX #4 US2_TX #0	LES_CH2
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X	TIM0_CDTI1 #3 WTIM0_CC2 #7	US1_CLK #4 US2_RX #0	LES_CH3

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8	Low Energy Timer LETIM0, output channel 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

5.16 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.14 APORT Connection Diagram on page 119 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

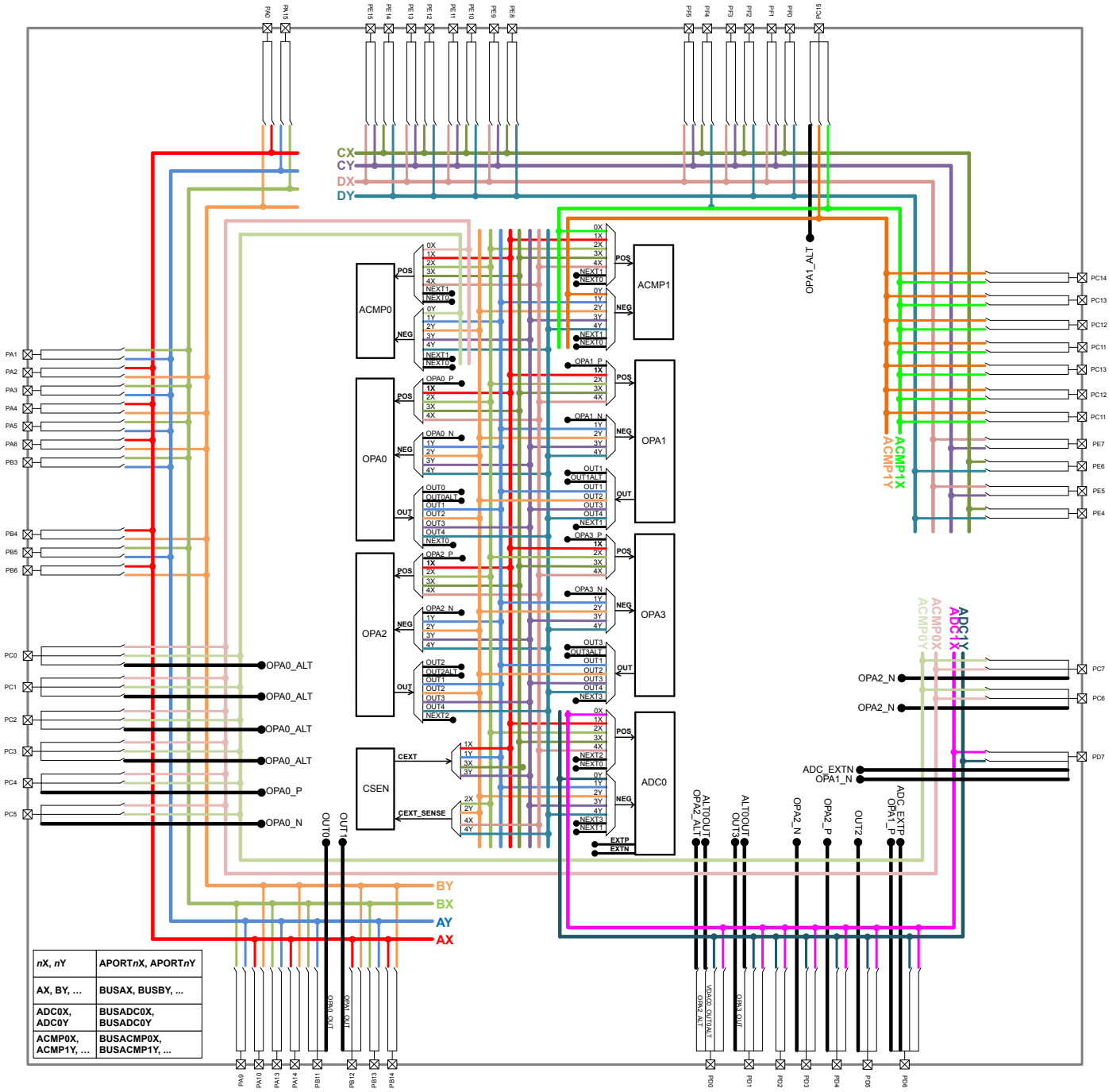

Figure 5.14. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

10.3 TQFP48 Package Marking

Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

11.2 QFN32 PCB Land Pattern

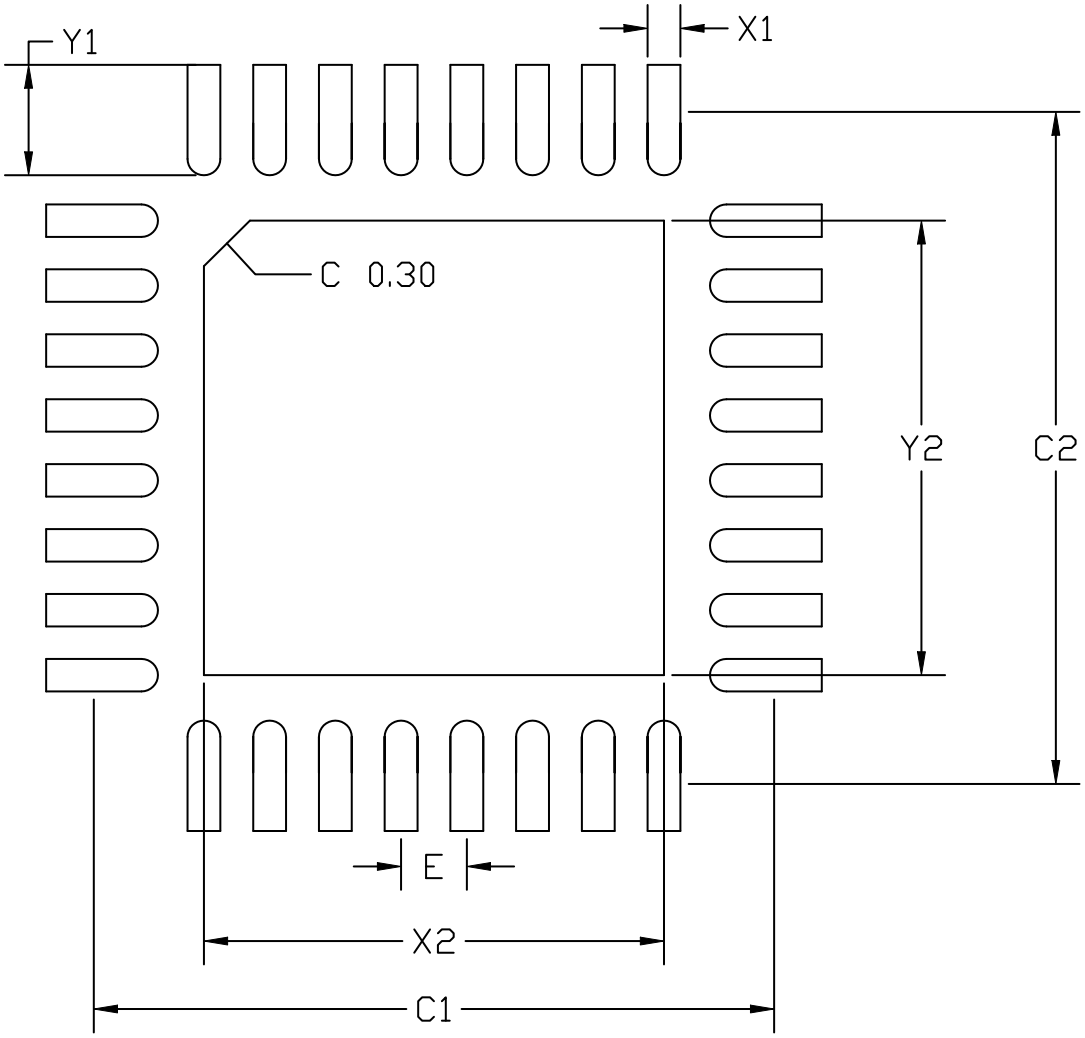

Figure 11.2. QFN32 PCB Land Pattern Drawing

Table 11.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
C1	5.00
C2	5.00
E	0.50
X1	0.30
Y1	0.80
X2	3.80
Y2	3.80

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 2x2 array of 0.9 mm square openings on a 1.2 mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Revision History

Revision 0.5

February, 2018

- 4.1 Electrical Characteristics updated with latest characterization data and production test limits.
- Added 4.1.3 Thermal Characteristics.
- Added 4.2 Typical Performance Curves section.
- Corrected OPA / VDAC output connections in Figure 5.14 APORT Connection Diagram on page 119.

Revision 0.1

May 1st, 2017

Initial release.