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Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b120f128iq48-a

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4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive[2], T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 µF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 µF. See Application Note AN0948 for details.

4.1.6.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{ACTIVE_DCM}	48 MHz crystal, CPU running while loop from flash	—	38	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	37	—	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	45	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	53	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	43	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	47	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	61	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	587	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]	I_{ACTIVE_CCM}	48 MHz crystal, CPU running while loop from flash	—	49	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	48	—	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	55	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	63	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	60	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	68	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	96	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1157	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	32	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	33	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	36	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	156	—	µA/MHz

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	f_{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f_{HFRCO} < 19 MHz	—	1	—	µs
		f_{HFRCO} ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 48 MHz	—	258	TBD	µA
		f_{HFRCO} = 38 MHz	—	218	TBD	µA
		f_{HFRCO} = 32 MHz	—	182	TBD	µA
		f_{HFRCO} = 26 MHz	—	156	TBD	µA
		f_{HFRCO} = 19 MHz	—	130	TBD	µA
		f_{HFRCO} = 16 MHz	—	112	TBD	µA
		f_{HFRCO} = 13 MHz	—	101	TBD	µA
		f_{HFRCO} = 7 MHz	—	80	TBD	µA
		f_{HFRCO} = 4 MHz	—	29	TBD	µA
		f_{HFRCO} = 2 MHz	—	26	TBD	µA
		f_{HFRCO} = 1 MHz	—	24	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	393	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	313	TBD	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	180	TBD	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	46	TBD	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	33	TBD	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, V_{INPUT} = 0.5 V, V_{OUTPUT} = 1.5 V. Nominal voltage gain is 3.
2. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. Step between 0.2V and V_{OPA}-0.2V, 10%-90% rising/falling range.
6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. V_{INPUT} = 0.5 V, V_{OUTPUT} = 0.5 V.
9. When HCMDIS=1 and input common mode transitions the region from V_{OPA}-1.4V to V_{OPA}-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

4.1.18 LCD Driver

Table 4.25. LCD Driver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		TBD	—	TBD	Hz
LCD supply range[2]	V_{LCDIN}		1.8	—	3.8	V
LCD output voltage range	V_{LCD}	Current source mode, No external LCD capacitor	2.0	—	V_{LCDIN}-0.4	V
		Step-down mode with external LCD capacitor	2.0	—	V_{LCDIN}	V
		Charge pump mode with external LCD capacitor	2.0	—	Min of 3.8 and 1.9 * V_{LCDIN}	V
Contrast control step size	$STEP_{CONTRAST}$	Current source mode	—	64	—	mV
		Charge pump or Step-down mode	—	43	—	mV
Contrast control step accuracy[1]	$ACC_{CONTRAST}$		—	+/-4	—	%

Note:

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.
2. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.

4.1.19 Pulse Counter (PCNT)

Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

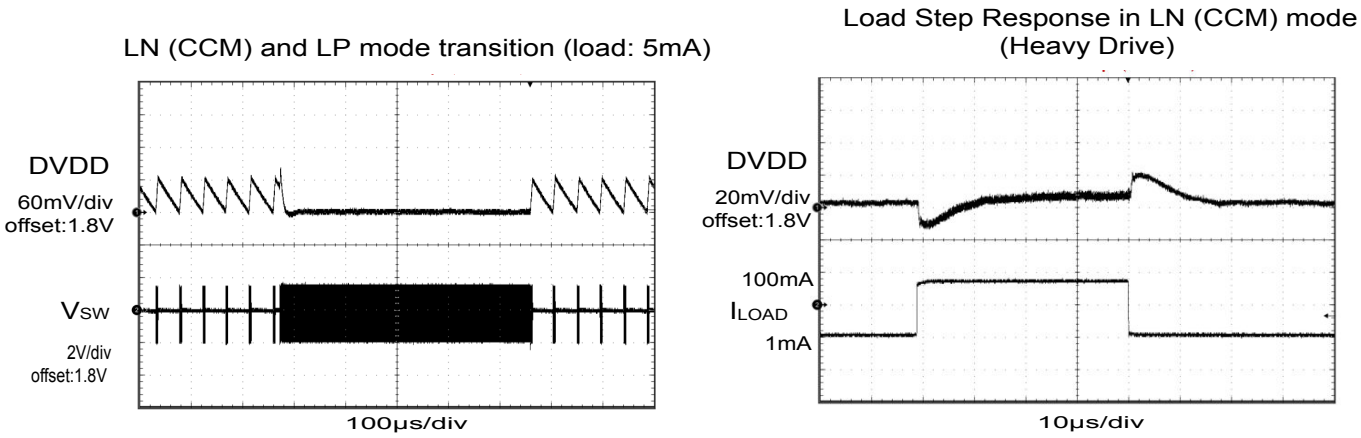

Figure 4.9. DC-DC Converter Transition Waveforms

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB4	10	GPIO	PB5	11	GPIO
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.13 EFM32TG11B1xx in QFN32 Device Pinout

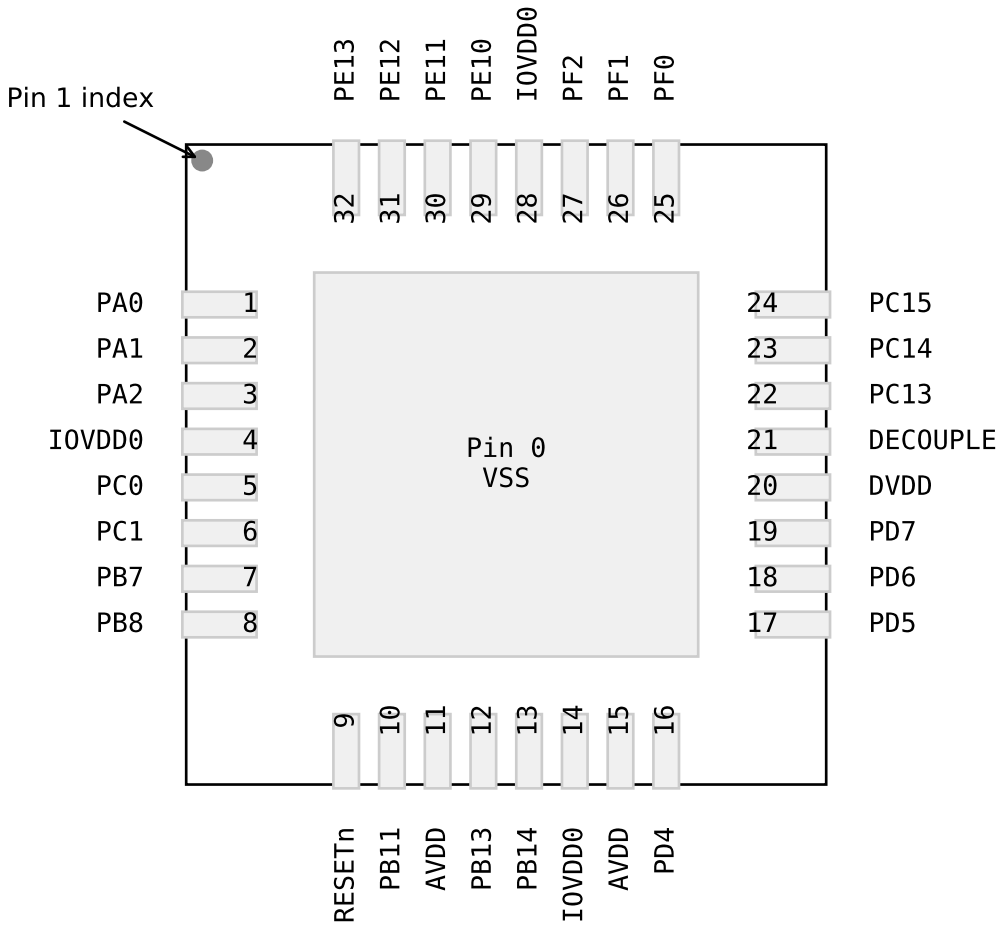

Figure 5.13. EFM32TG11B1xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.13. EFM32TG11B1xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 28	Digital IO power supply 0.	PC0	5	GPIO (5V)
PC1	6	GPIO (5V)	PB7	7	GPIO

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PD5	BUSADC0Y BUSADC0X OPA2_OUT	WTIM0_CDTI1 #4 WTIM1_CC3 #1	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT OPA1_P	TIM1_CC0 #4 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_AL-TEX0 PRS_CH5 #2 ACMP0_O #2
PD7	BUSADC0Y BUSADC0X ADC0_EXTN OPA1_N	TIM1_CC1 #4 WTIM1_CC1 #2 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_AL-TEX1 ACMP1_O #2
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1
PC6	BUSACMP0Y BU-SACMP0X OPA3_P LCD_SEG32	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 I2C0_SDA #2	LES_CH6
PC7	BUSACMP0Y BU-SACMP0X OPA3_N LCD_SEG33	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 I2C0_SCL #2	LES_CH7
PE4	BUSDY BUSCX LCD_COM0	WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 I2C0_SDA #7	
PE5	BUSCY BUSDX LCD_COM1	WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 I2C0_SCL #7	
PE6	BUSDY BUSCX LCD_COM2	WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2
PE7	BUSCY BUSDX LCD_COM3	WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2
PC8	BUSACMP1Y BU-SACMP1X LCD_SEG34		US0_CS #2	LES_CH8 PRS_CH4 #0
PC9	BUSACMP1Y BU-SACMP1X LCD_SEG35		US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC10	BUSACMP1Y BU-SACMP1X		US0_RX #2	LES_CH10
PC11	BUSACMP1Y BU-SACMP1X		US0_TX #2 I2C1_SDA #4	LES_CH11
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BU-SACMP1Y BUSACMP1X	TIM1_CC3 #0	US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3	CMU_CLK0 #1 LES_CH12
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BU-SACMP1Y BUSACMP1X	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3	LES_CH13
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BU-SACMP1Y BUSACMP1X	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 LEU0_TX #5	LES_CH14 PRS_CH0 #2

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions

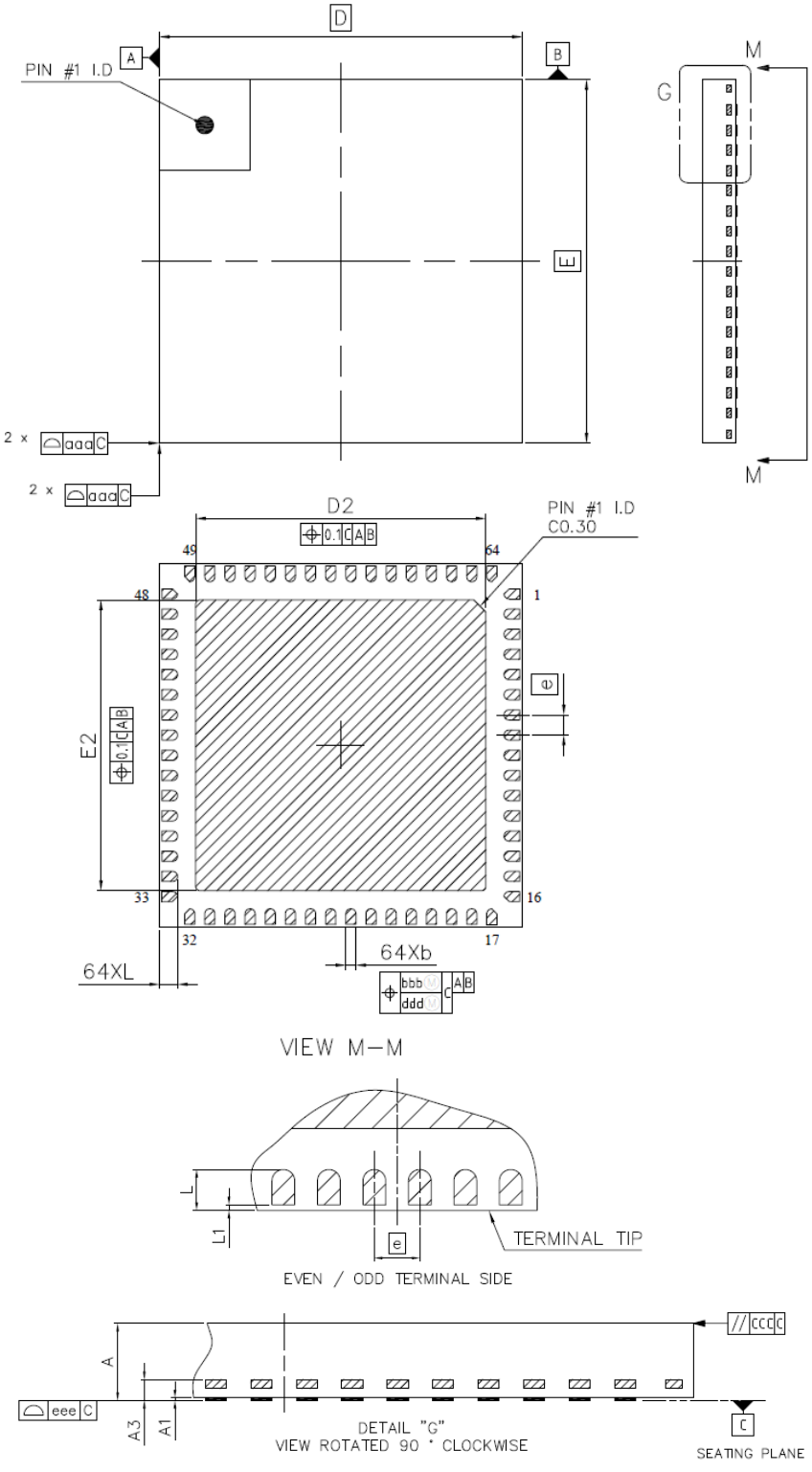

Figure 9.1. QFN64 Package Drawing

Table 10.1. TQFP48 Package Dimensions

Dimension	Min	Typ	Max
A		7.00 BSC	
A1		3.50 BSC	
B		7.00 BSC	
B1		3.50 BSC	
C	1.00	—	1.20
D	0.17	—	0.27
E	0.95	—	1.05
F	0.17	—	0.23
G		0.50 BSC	
H	0.05	—	0.15
J	0.09	—	0.20
K	0.50	—	0.70
L	0	—	7
M		12 REF	
N	0.09	—	0.16
P		0.25 BSC	
R	0.150	—	0.250
S		9.00 BSC	
S1		4.50 BSC	
V		9.00 BSC	
V1		4.50 BSC	
W		0.20 BSC	
AA		1.00 BSC	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10.3 TQFP48 Package Marking

Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.