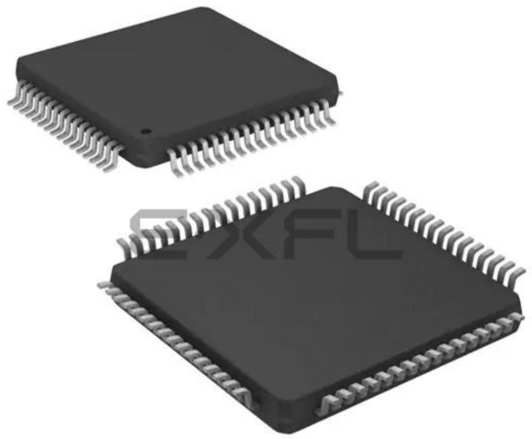

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b120f128iq64-a

1. Feature List

The EFM32TG11 highlighted features are listed below.

- **ARM Cortex-M0+ CPU platform**
  - High performance 32-bit processor @ up to 48 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 37 µA/MHz in Active Mode (EM0)
  - 1.30 µA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power absent/ insufficient
- **Up to 128 kB flash program memory**
- **Up to 32 kB RAM data memory**
- **Communication Interfaces**
  - CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (24 MHz) operation on one instance
  - 1 × Universal Asynchronous Receiver/ Transmitter
  - 1 × Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2 × I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 67 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 8 Channel DMA Controller**
- **Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 × 32 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Up to 2 × Analog Comparator (ACMP)
  - Up to 4 × Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
  - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

Table of Contents

3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

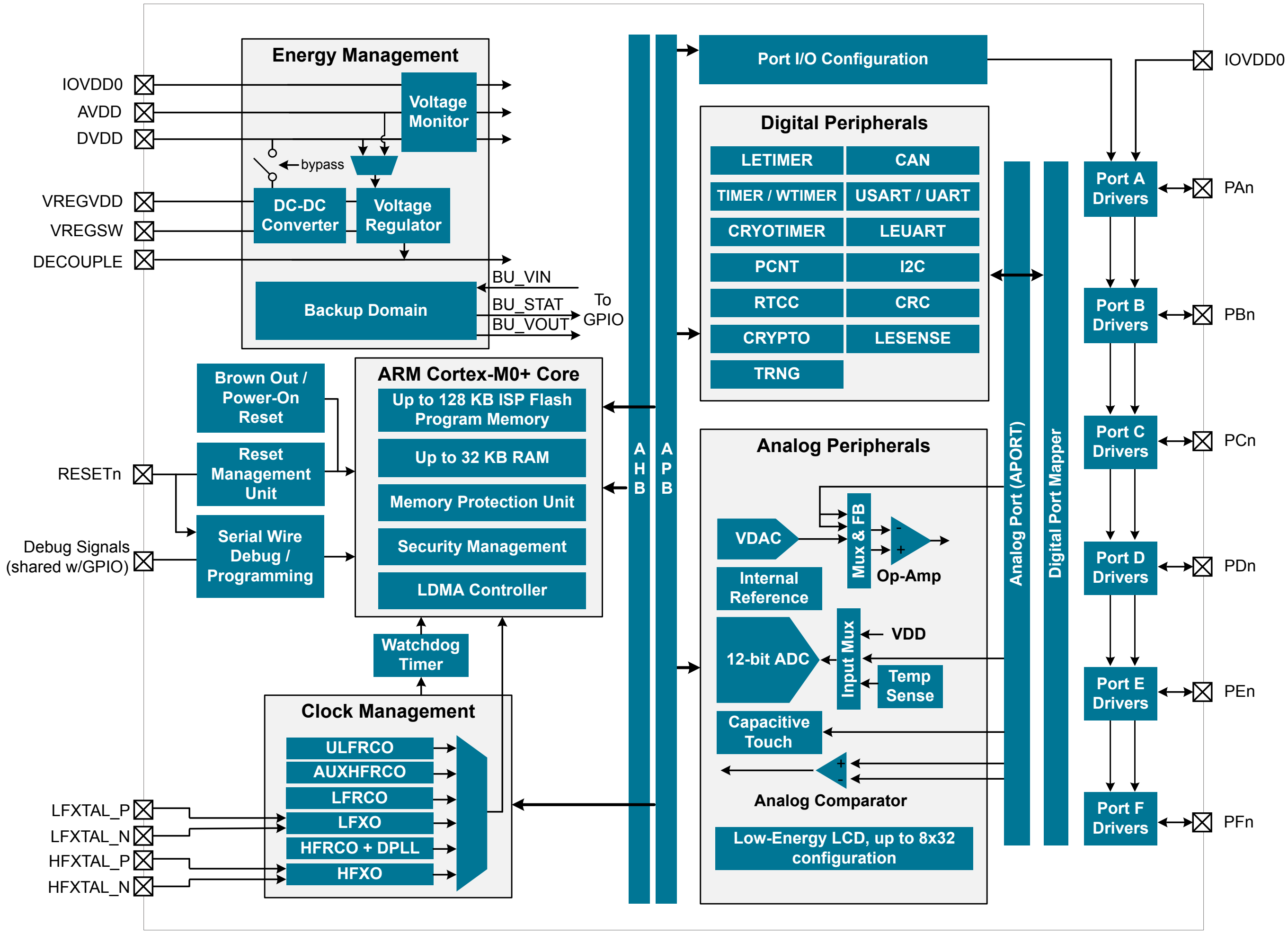


Figure 3.1. Detailed EFM32TG11 Block Diagram

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM} provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	—	°C/W
Thermal resistance, TQFP48 Package	$THETA_{JA\_TQFP48}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	43.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	—	°C/W
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	37.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	35.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	—	°C/W
Thermal resistance, QFN80 Package	$THETA_{JA\_QFN80}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP80 Package	$THETA_{JA\_TQFP80}$	4-Layer PCB, Air velocity = 0 m/s	—	49.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	44.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.6	—	°C/W

4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.13. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	TBD	32.768	TBD	kHz
		ENVREF[2] = 1, T > 85 °C	TBD	32.768	TBD	kHz
		ENVREF[2] = 0	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.20. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	μA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	μA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	166	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[5]	SR	DRIVESTRENGTH = 3, INCBW=1[3]	—	4.7	—	V/μs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/μs
		DRIVESTRENGTH = 2, INCBW=1[3]	—	1.27	—	V/μs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/μs
		DRIVESTRENGTH = 1, INCBW=1[3]	—	0.17	—	V/μs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/μs
		DRIVESTRENGTH = 0, INCBW=1[3]	—	0.044	—	V/μs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/μs
Startup time[6]	T_{START}	DRIVESTRENGTH = 2	—	—	TBD	μs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

4.1.21.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.30. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

5.2 EFM32TG11B5xx in QFN80 Device Pinout

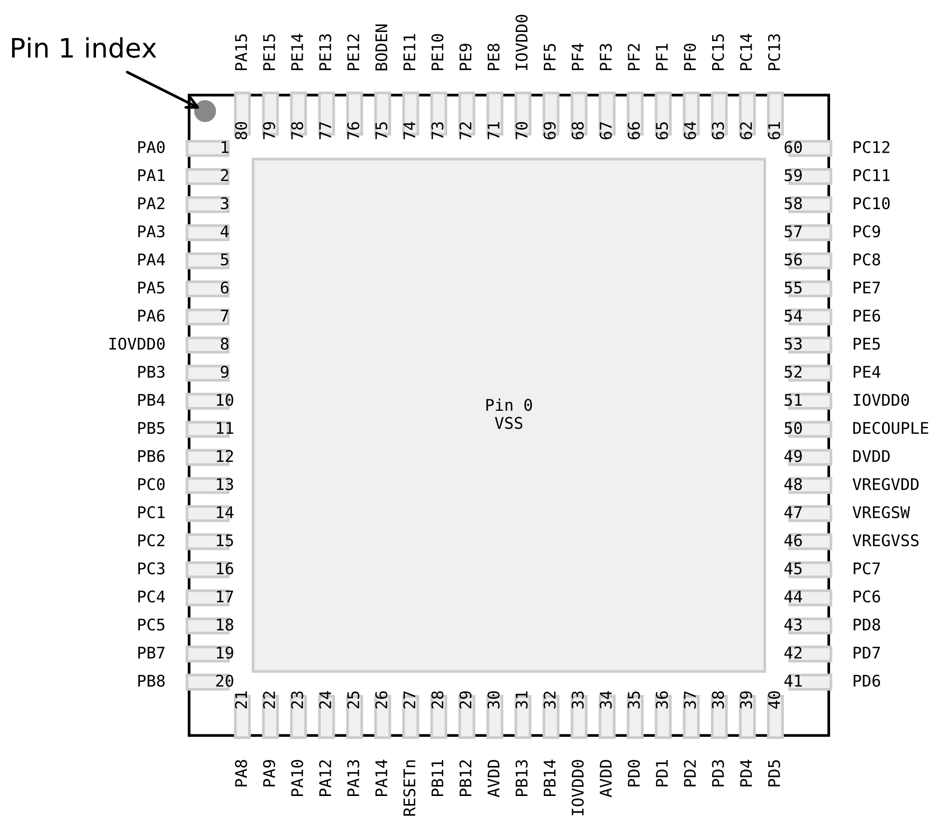


Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.2. EFM32TG11B5xx in QFN80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	79	GPIO	PA15	80	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB4	10	GPIO	PB5	11	GPIO
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11 15	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	16	GPIO	PD5	17	GPIO
PD6	18	GPIO	PD7	19	GPIO
DVDD	20	Digital power supply.	DECOUPLE	21	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC13	22	GPIO (5V)	PC14	23	GPIO (5V)
PC15	24	GPIO (5V)	PF0	25	GPIO (5V)
PF1	26	GPIO (5V)	PF2	27	GPIO
PE10	29	GPIO	PE11	30	GPIO
PE12	31	GPIO	PE13	32	GPIO

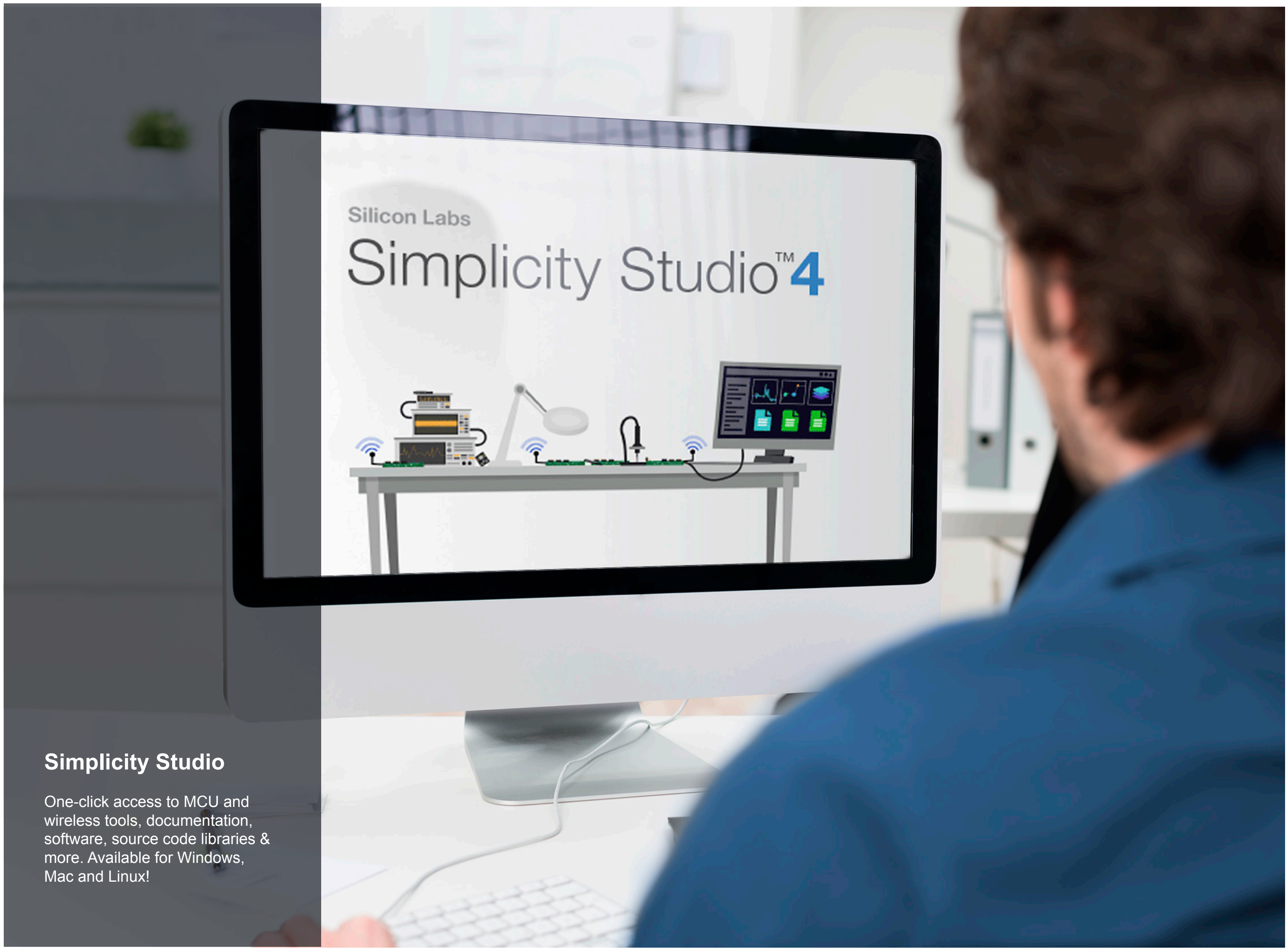
Note:
1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG9	0: PE13		LCD segment line 9.
LCD_SEG10	0: PE14		LCD segment line 10.
LCD_SEG11	0: PE15		LCD segment line 11.
LCD_SEG12	0: PA15		LCD segment line 12.
LCD_SEG13	0: PA0		LCD segment line 13.
LCD_SEG14	0: PA1		LCD segment line 14.
LCD_SEG15	0: PA2		LCD segment line 15.
LCD_SEG16	0: PA3		LCD segment line 16.
LCD_SEG17	0: PA4		LCD segment line 17.
LCD_SEG18	0: PA5		LCD segment line 18.
LCD_SEG19	0: PA6		LCD segment line 19.
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PC4		LCD segment line 24.
LCD_SEG25	0: PC5		LCD segment line 25.
LCD_SEG26	0: PA9		LCD segment line 26.
LCD_SEG27	0: PA10		LCD segment line 27.
LCD_SEG28	0: PB11		LCD segment line 28.
LCD_SEG29	0: PB12		LCD segment line 29.
LCD_SEG30	0: PD3		LCD segment line 30.
LCD_SEG31	0: PD4		LCD segment line 31.
LCD_SEG32	0: PC6		LCD segment line 32.
LCD_SEG33	0: PC7		LCD segment line 33.
LCD_SEG34	0: PC8		LCD segment line 34.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM0_CC0	0: PA0 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 2: PD3 3: PC1	4: PF2 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 3: PB7	4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 3: PB8	4: PD7 5: PF3	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 3: PB11	4: PC13 5: PF4	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 6: PF5	Timer 1 Capture Compare input / output channel 3.
U0_CTS	 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.



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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com