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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b140f64gm64-a

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3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	12C0
APORT	I2C1
-	IDAC
-	LCD

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Max load current	ILOAD_MAX	Low noise (LN) mode, Heavy Drive ² , T ≤ 85 °C	_	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , T > 85 °C	—	_	100	mA
		Low noise (LN) mode, Medium Drive ²	_	_	100	mA
		Low noise (LN) mode, Light Drive ²	_	_	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	_	_	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	_	_	10	mA
DCDC nominal output ca- pacitor ⁵	C _{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output induc- tor	L _{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R _{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.

- 2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=15.
- 3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.

4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.

5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frequency accuracy	fhfrco_acc	At production calibrated frequen- cies, across supply voltage and temperature	TBD	_	TBD	%
Start-up time	t _{HFRCO}	f _{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f _{HFRCO} < 19 MHz	_	1	—	μs
		f _{HFRCO} ≤ 4 MHz	—	2.5	—	μs
Current consumption on all	I _{HFRCO}	f _{HFRCO} = 48 MHz	—	258	TBD	μA
supplies		f _{HFRCO} = 38 MHz	_	218	TBD	μA
		f _{HFRCO} = 32 MHz	_	182	TBD	μA
		f _{HFRCO} = 26 MHz	_	156	TBD	μA
		f _{HFRCO} = 19 MHz	_	130	TBD	μA
		f _{HFRCO} = 16 MHz	_	112	TBD	μA
		f _{HFRCO} = 13 MHz	_	101	TBD	μA
		f _{HFRCO} = 7 MHz	_	80	TBD	μA
		f _{HFRCO} = 4 MHz	_	29	TBD	μA
		f _{HFRCO} = 2 MHz	_	26	TBD	μA
		f _{HFRCO} = 1 MHz	_	24	TBD	μA
		f _{HFRCO} = 40 MHz, DPLL enabled	—	393	TBD	μA
		f _{HFRCO} = 32 MHz, DPLL enabled	—	313	TBD	μA
		f _{HFRCO} = 16 MHz, DPLL enabled	—	180	TBD	μA
		f _{HFRCO} = 4 MHz, DPLL enabled	_	46	TBD	μA
		f _{HFRCO} = 1 MHz, DPLL enabled	—	33	TBD	μA
Coarse trim step size (% of period)	SS _{HFRCO_COARS}		—	0.8	_	%
Fine trim step size (% of pe- riod)	SS _{HFRCO_FINE}			0.1		%
Period jitter	PJ _{HFRCO}			0.2		% RMS

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output fall time, From 70%	t _{IOOF}	C _L = 50 pF,	—	1.8	_	ns
		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE ¹ = 0x6				
		C _L = 50 pF,	_	4.5	_	ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Output rise time, From 30%	t _{IOOR}	C _L = 50 pF,	_	2.2	_	ns
to 70% of V _{IO}		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE = 0x6 ¹				
		C _L = 50 pF,	—	7.4	_	ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Note:	-1		1	1	1	
1. In GPIO_Pn_CTRL regis	iter.					

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.20. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Resolution	VRESOLUTION		6	_	12	Bits
Input voltage range ⁵	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2		V _{FS} /2	V
Input range of external refer- ence voltage, single ended and differential	Vadcrefin_p		1	—	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	_	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	_	80	_	dB
Current from all supplies, us- ing internal reference buffer.	I _{ADC_CONTI-} NOUS_LP	1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	270	TBD	μA
MUPMODE ⁴ = KEEPADC- WARM		250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 1 ³	_	125	_	μA
		62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 1 ³	_	80	-	μA
Current from all supplies, us- ing internal reference buffer.	IADC_NORMAL_LP	35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	—	45	_	μA
MUPMODE ⁴ = NORMAL		5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 1 ³	_	8	_	μA
Current from all supplies, using internal reference buffer.	IADC_STAND- BY_LP	125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	105	-	μA
AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC		35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	70	_	μA
Current from all supplies, us- ing internal reference buffer.	IADC_CONTI- NOUS_HP	1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³		325	-	μA
MUPMODE ⁴ = KEEPADC- WARM		250 ksps / 4 MHz ADCCLK, BIA-SPROG = 6, GPBIASACC = 0 3	_	175	_	μA
		62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 0 ³	_	125	-	μA
Current from all supplies, us- ing internal reference buffer.	IADC_NORMAL_HP	35 ksps / 16 MHz ADCCLK, BIA-SPROG = 0, GPBIASACC = 0 3	_	85	_	μA
Duty-cycled operation. WAR- MUPMODE ⁴ = NORMAL		5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 0 ³	_	16	_	μA
Current from all supplies, us- ing internal reference buffer.	I _{ADC_STAND-} BY_HP	125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³	_	160	-	μA
AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC		35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³	_	125	-	μA
Current from HFPERCLK	IADC_CLK	HFPERCLK = 16 MHz	_	166	_	μA

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Slew rate ⁵	SR	DRIVESTRENGTH = 3, INCBW=1 ³	_	4.7	_	V/µs
		DRIVESTRENGTH = 3, INCBW=0	_	1.5	_	V/µs
		DRIVESTRENGTH = 2, INCBW=1 ³	_	1.27	_	V/µs
		DRIVESTRENGTH = 2, INCBW=0	_	0.42		V/µs
		DRIVESTRENGTH = 1, INCBW=1 ³	_	0.17	_	V/µs
		DRIVESTRENGTH = 1, INCBW=0	_	0.058		V/µs
		DRIVESTRENGTH = 0, INCBW=1 ³	_	0.044	_	V/µs
		DRIVESTRENGTH = 0, INCBW=0	_	0.015	_	V/µs
Startup time ⁶	T _{START}	DRIVESTRENGTH = 2	_	_	TBD	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	_	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	_	TBD	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	_	70	_	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	_	70	_	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90	_	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90		dB

4.1.21.2 I2C Fast-mode (Fm)¹

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCL clock frequency ²	f _{SCL}		0	_	400	kHz
SCL clock low time	t _{LOW}		1.3	—	_	μs
SCL clock high time	t _{HIGH}		0.6	_	_	μs
SDA set-up time	t _{SU_DAT}		100	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	_	900	ns
Repeated START condition set-up time	t _{SU_STA}		0.6	_	_	μs
(Repeated) START condition hold time	t _{HD_STA}		0.6		_	μs
STOP condition set-up time	t _{SU_STO}		0.6		_	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3			μs

Table 4.29. I2C Fast-mode (Fm)¹

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.

2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.

3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	9 24 51 70	Ground	PB3	10	GPIO
PB4	11	GPIO	PB5	12	GPIO
PB6	13	GPIO	PC1	14	GPIO (5V)
PC2	15	GPIO (5V)	PC3	16	GPIO (5V)
PC4	17	GPIO	PC5	18	GPIO
PB7	19	GPIO	PB8	20	GPIO
PA8	21	GPIO	PA9	22	GPIO
PA10	23	GPIO	PA12	25	GPIO
PA14	26	GPIO	RESETn	27	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	28	GPIO	PB12	29	GPIO
AVDD	30 34	Analog power supply.	PB13	31	GPIO
PB14	32	GPIO	PD0	35	GPIO (5V)
PD1	36	GPIO	PD3	37	GPIO
PD4	38	GPIO	PD5	39	GPIO
PD6	40	GPIO	PD7	41	GPIO
PD8	42	GPIO	PC6	43	GPIO
PC7	44	GPIO	VREGVSS	45	Voltage regulator VSS
VREGSW	46	DCDC regulator switching node	VREGVDD	47	Voltage regulator VDD input
DVDD	48	Digital power supply.	DECOUPLE	49	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	52	GPIO	PE5	53	GPIO
PE6	54	GPIO	PE7	55	GPIO
PC8	56	GPIO	PC9	57	GPIO
PC10	58	GPIO (5V)	PC11	59	GPIO (5V)
PC13	60	GPIO (5V)	PC14	61	GPIO (5V)
PC15	62	GPIO (5V)	PF0	63	GPIO (5V)
PF1	64	GPIO (5V)	PF2	65	GPIO
PF3	66	GPIO	PF4	67	GPIO
PF5	68	GPIO	PE8	71	GPIO
PE9	72	GPIO	PE10	73	GPIO
PE11	74	GPIO	BODEN	75	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.



Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.2. E	EFM32TG11B5xx ir	1 QFN80	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO



Figure 5.11. EFM32TG11B1xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 22 43	Digital IO power supply 0.
VSS	5 18 44	Ground	PC0	6	GPIO (5V)
PC1	7	GPIO (5V)	PC2	8	GPIO (5V)
PC3	9	GPIO (5V)	PC4	10	GPIO

Alternate	LOCA	TION	
Functionality	0 - 3	4 - 7	Description
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PC4		LCD segment line 24.
LCD_SEG25	0: PC5		LCD segment line 25.
LCD_SEG26	0: PA9		LCD segment line 26.
LCD_SEG27	0: PA10		LCD segment line 27.
LCD_SEG28	0: PB11		LCD segment line 28.
LCD_SEG29	0: PB12		LCD segment line 29.
LCD_SEG30	0: PD3		LCD segment line 30.
LCD_SEG31	0: PD4		LCD segment line 31.
LCD_SEG32	0: PC6		LCD segment line 32.
LCD_SEG33	0: PC7		LCD segment line 33.
LCD_SEG34	0: PC8		LCD segment line 34.

Alternate	LOCA	ATION										
Functionality	0 - 3	4 - 7	Description									
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.									
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.									
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.									
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.									
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.									
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.									
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.									
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.									
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.									
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.									
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.									
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.									
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.									

5.16 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.14 APORT Connection Diagram on page 119 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.





Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 5.17. ACMP1 Bus and Pin Mapping

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
ОР	A1_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OPA1_P																																	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OP	A2_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

6. TQFP80 Package Specifications

6.1 TQFP80 Package Dimensions



Figure 6.1. TQFP80 Package Drawing



Figure 7.3. QFN80 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

8.2 TQFP64 PCB Land Pattern



Figure 8.2. TQFP64 PCB Land Pattern Drawing

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions

