What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b140f64gm64-ar

1. Feature List

The EFM32TG11 highlighted features are listed below.

- **ARM Cortex-M0+ CPU platform**
  - High performance 32-bit processor @ up to 48 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 37 µA/MHz in Active Mode (EM0)
  - 1.30 µA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power absent/ insufficient
- **Up to 128 kB flash program memory**
- **Up to 32 kB RAM data memory**
- **Communication Interfaces**
  - CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (24 MHz) operation on one instance
  - 1 × Universal Asynchronous Receiver/ Transmitter
  - 1 × Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2 × I^{2}C Interface with SMBus support
    - Address recognition in EM3 Stop Mode

- **Up to 67 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 8 Channel DMA Controller**
- **Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 × 32 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Up to 2 × Analog Comparator (ACMP)
  - Up to 4 × Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
  - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.
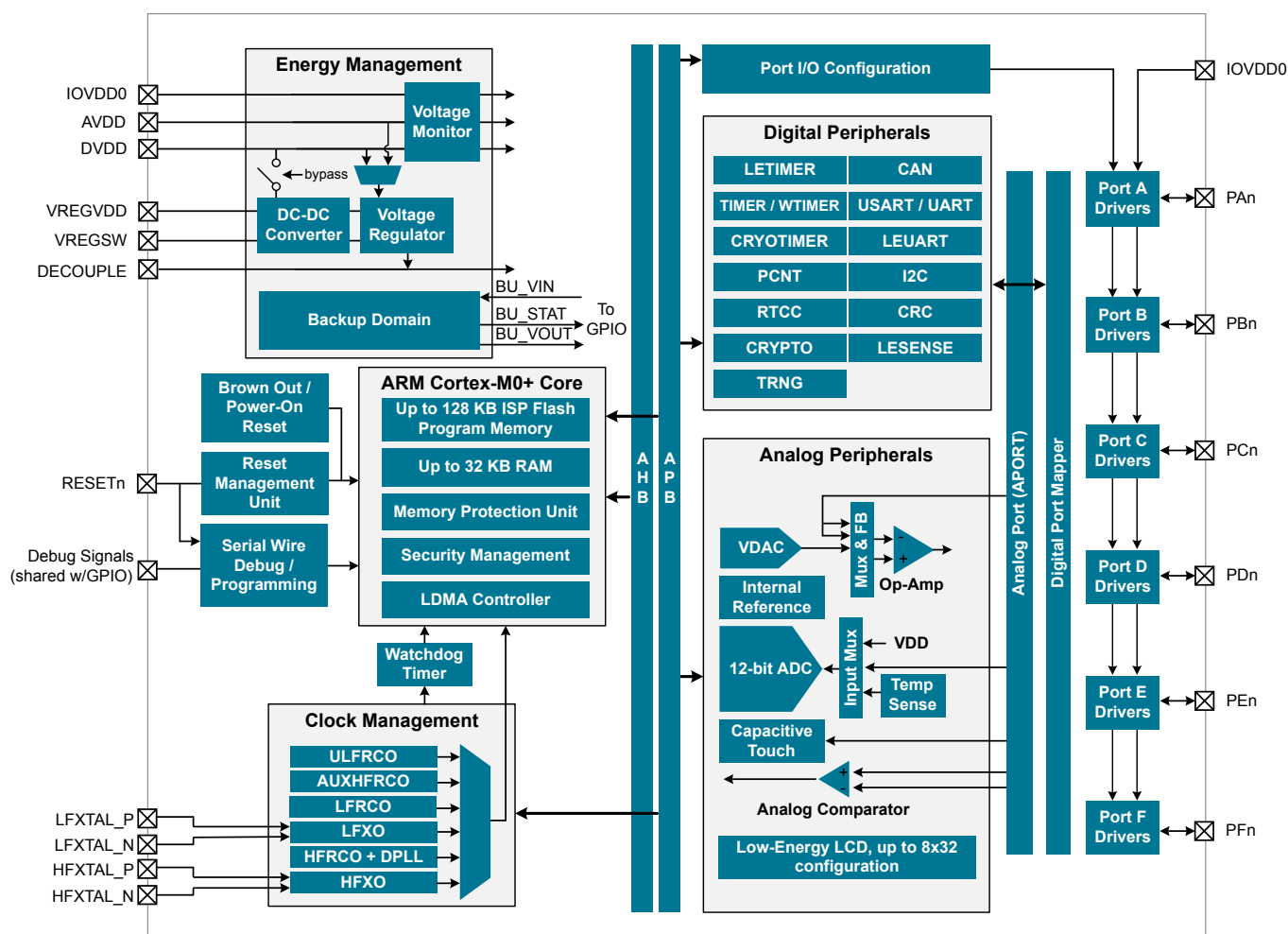
Figure 3.1. Detailed EFM32TG11 Block Diagram

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.6.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{ACTIVE_DCM}	48 MHz crystal, CPU running while loop from flash	—	38	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	37	—	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	45	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	53	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	43	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	47	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	61	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	587	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]	I_{ACTIVE_CCM}	48 MHz crystal, CPU running while loop from flash	—	49	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	48	—	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	55	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	63	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	60	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	68	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	96	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1157	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	32	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	33	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	36	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	156	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[4]	—	0.18	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[4]	—	0.18	—	µA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	$f_{HFRCO} = 48$ MHz	—	258	TBD	µA
		$f_{HFRCO} = 38$ MHz	—	218	TBD	µA
		$f_{HFRCO} = 32$ MHz	—	182	TBD	µA
		$f_{HFRCO} = 26$ MHz	—	156	TBD	µA
		$f_{HFRCO} = 19$ MHz	—	130	TBD	µA
		$f_{HFRCO} = 16$ MHz	—	112	TBD	µA
		$f_{HFRCO} = 13$ MHz	—	101	TBD	µA
		$f_{HFRCO} = 7$ MHz	—	80	TBD	µA
		$f_{HFRCO} = 4$ MHz	—	29	TBD	µA
		$f_{HFRCO} = 2$ MHz	—	26	TBD	µA
		$f_{HFRCO} = 1$ MHz	—	24	TBD	µA
		$f_{HFRCO} = 40$ MHz, DPLL enabled	—	393	TBD	µA
		$f_{HFRCO} = 32$ MHz, DPLL enabled	—	313	TBD	µA
		$f_{HFRCO} = 16$ MHz, DPLL enabled	—	180	TBD	µA
		$f_{HFRCO} = 4$ MHz, DPLL enabled	—	46	TBD	µA
		$f_{HFRCO} = 1$ MHz, DPLL enabled	—	33	TBD	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.21.2 I2C Fast-mode (Fm)[1]

Table 4.29. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

SPI Slave Timing

Table 4.32. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		$6 * t_{HFPERCLK}$	—	—	ns
SCLK high time[1] [3] [2]	t_{SCLK_HI}		$2.5 * t_{HFPERCLK}$	—	—	ns
SCLK low time[1] [3] [2]	t_{SCLK_LO}		$2.5 * t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		20	—	70	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		15	—	150	ns
MOSI setup time [1] [3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		7	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		$14 + 1.5 * t_{HFPERCLK}$	—	$40 + 2.5 * t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
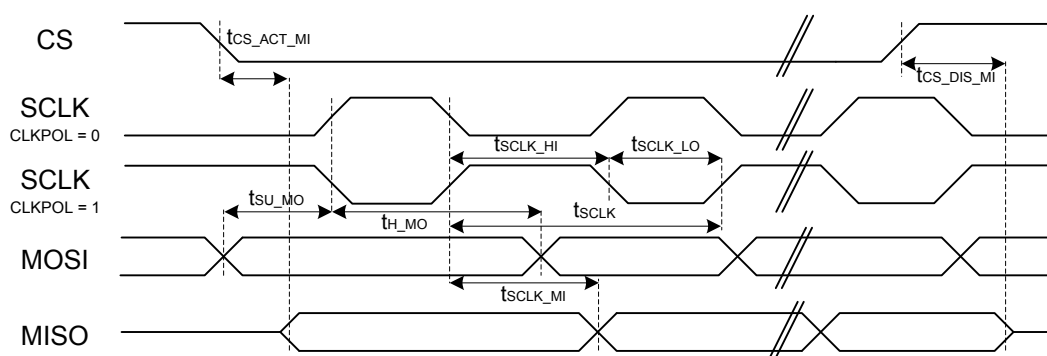
Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.
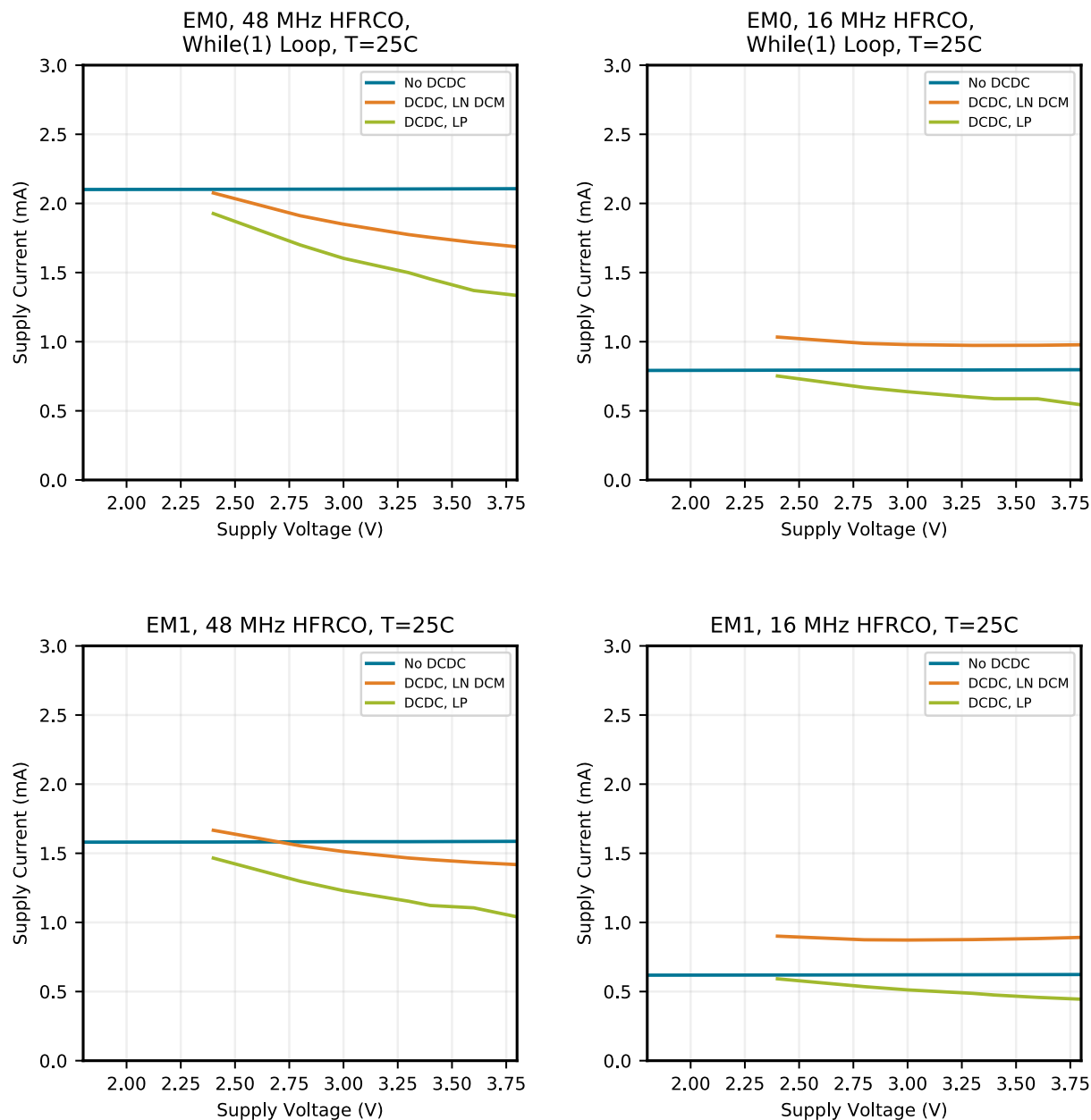
Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGVSS	38	Voltage regulator VSS	VREGSW	39	DCDC regulator switching node
VREGVDD	40	Voltage regulator VDD input	DVDD	41	Digital power supply.
DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	43	GPIO
PE5	44	GPIO	PE6	45	GPIO
PE7	46	GPIO	PC12	47	GPIO (5V)
PC13	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.7 EFM32TG11B3xx in QFN64 Device Pinout
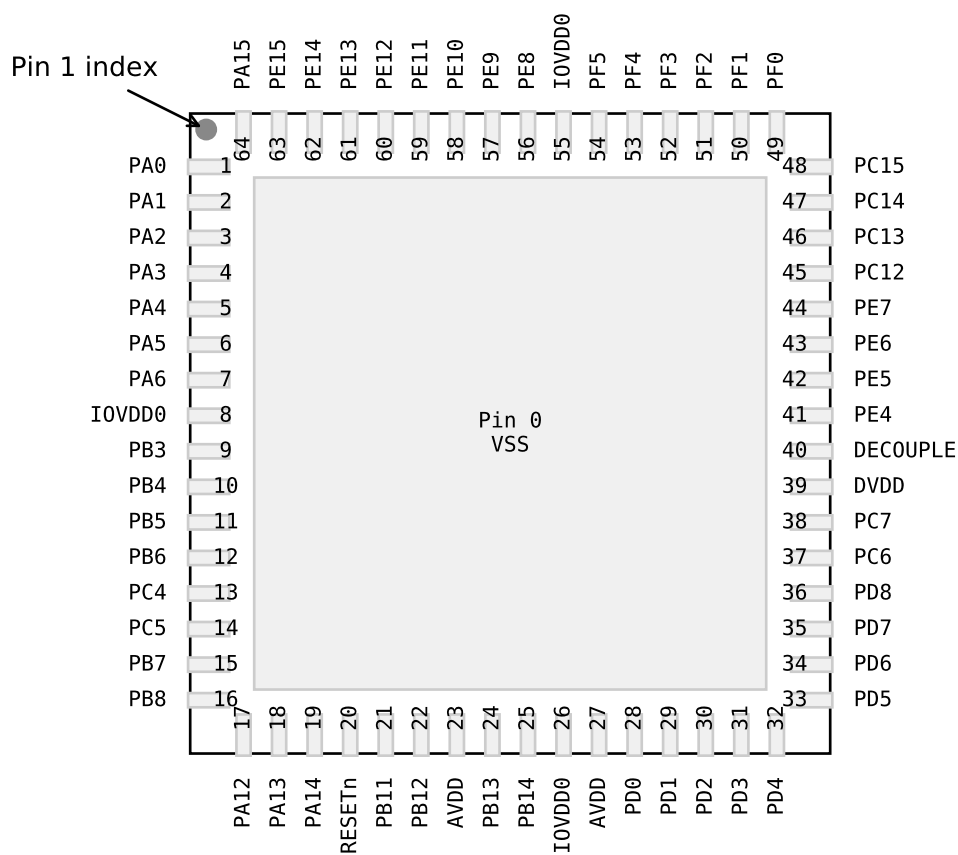
Figure 5.7. EFM32TG11B3xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.7. EFM32TG11B3xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	11	GPIO	PA8	12	GPIO
PA12	13	GPIO	PA14	14	GPIO
RESETn	15	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	16	GPIO
AVDD	18 22	Analog power supply.	PB13	19	GPIO
PB14	20	GPIO	PD4	23	GPIO
PD5	24	GPIO	PD6	25	GPIO
PD7	26	GPIO	PD8	27	GPIO
VREGVSS	28	Voltage regulator VSS	VREGSW	29	DCDC regulator switching node
VREGVDD	30	Voltage regulator VDD input	DVDD	31	Digital power supply.
DECOUPLE	32	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	33	GPIO
PE5	34	GPIO	PE6	35	GPIO
PE7	36	GPIO	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:
1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PE10		Pin can be used to wake the system up from EM4
HFXTAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1 1: PD7 2: PC7	4: PC1 5: PF1 6: PE13 7: PE5	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PD6 2: PC6	4: PC0 5: PF0 6: PE12 7: PE4	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12 3: PD5	4: PF2	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11 3: PD4	4: PC11	I2C1 Serial Data input / output.
LCD_BEXT	0: PA14		LCD external supply bypass in step down or charge pump mode. If using the LCD in step-down or charge pump mode, a 1 uF (minimum) capacitor between this pin and VSS is required. To reduce supply ripple, a larger capcitor of approximately 1000 times the total LCD segment capacitance may be used. If using the LCD with the internal supply source, this pin may be left unconnected or used as a GPIO.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13	USART0 chip select input / output.
US0_CTS	0: PE14 2: PC7 3: PC13	4: PB6 5: PB11	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 2: PC6 3: PC12	4: PB5 5: PD6	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4	USART1 chip select input / output.
US1_CTS	1: PD4 2: PF3 3: PC6	4: PC12 5: PB13	USART1 Clear To Send hardware flow control input.
US1_RTS	1: PD5 2: PF4 3: PC7	4: PC13 5: PB14	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OPA1_P																																	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OPA2_N																																	
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

6. TQFP80 Package Specifications
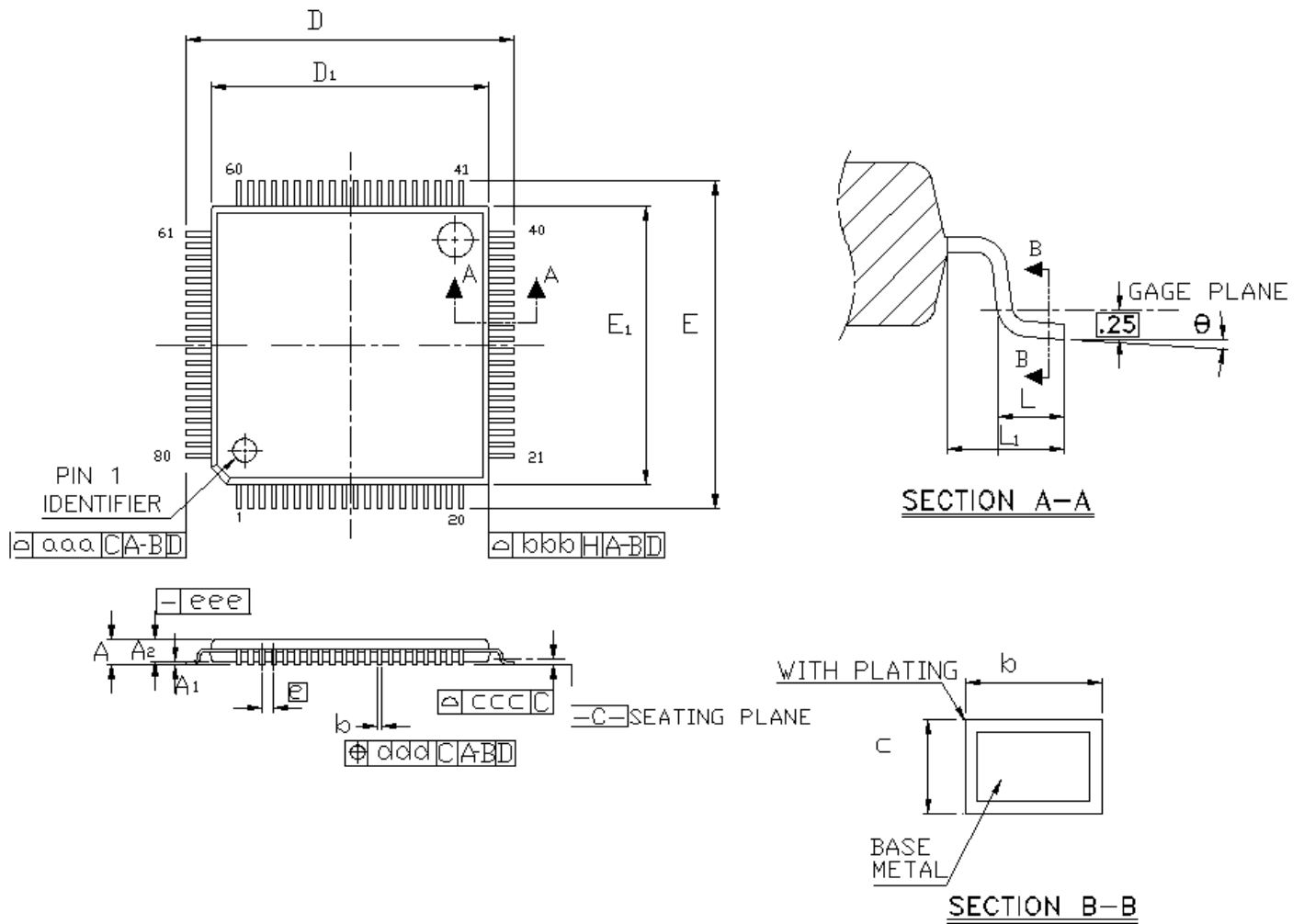
6.1 TQFP80 Package Dimensions

Figure 6.1. TQFP80 Package Drawing
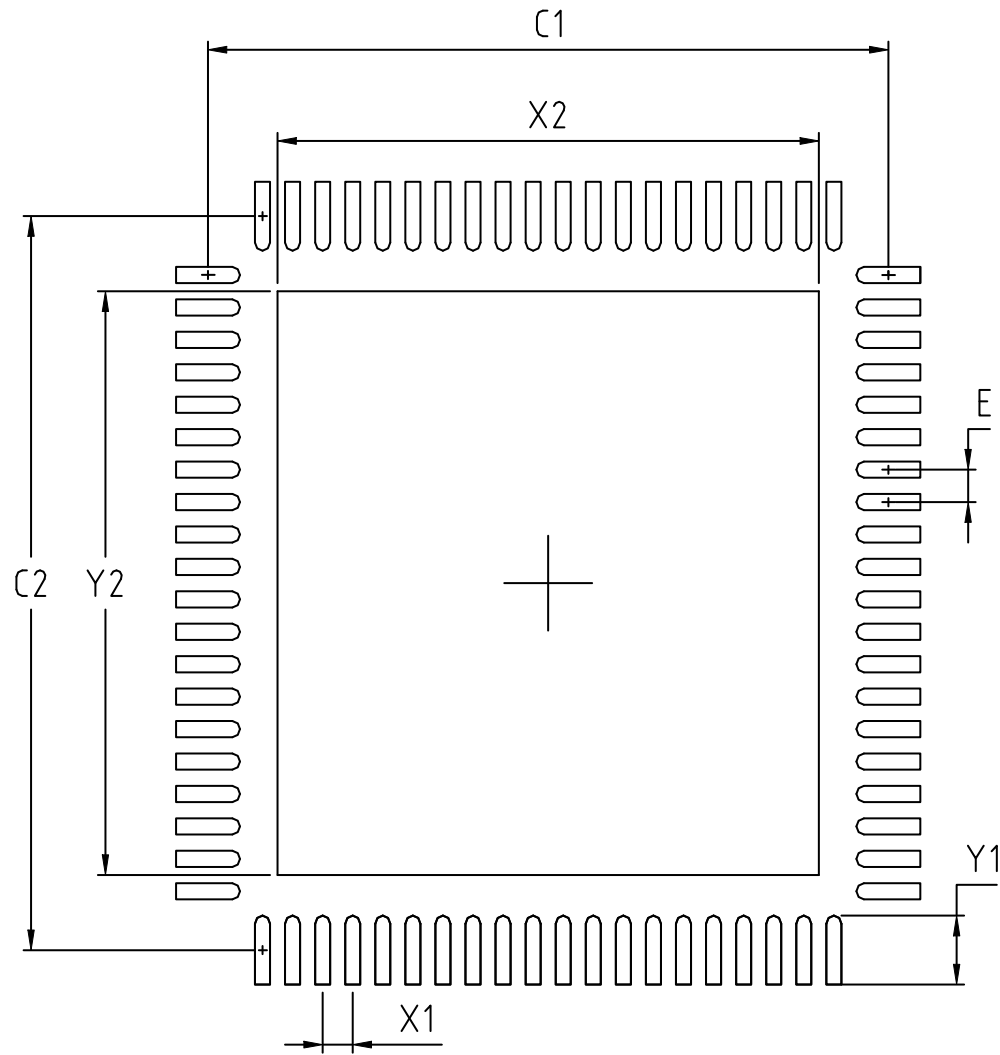
7.2 QFN80 PCB Land Pattern

Figure 7.2. QFN80 PCB Land Pattern Drawing

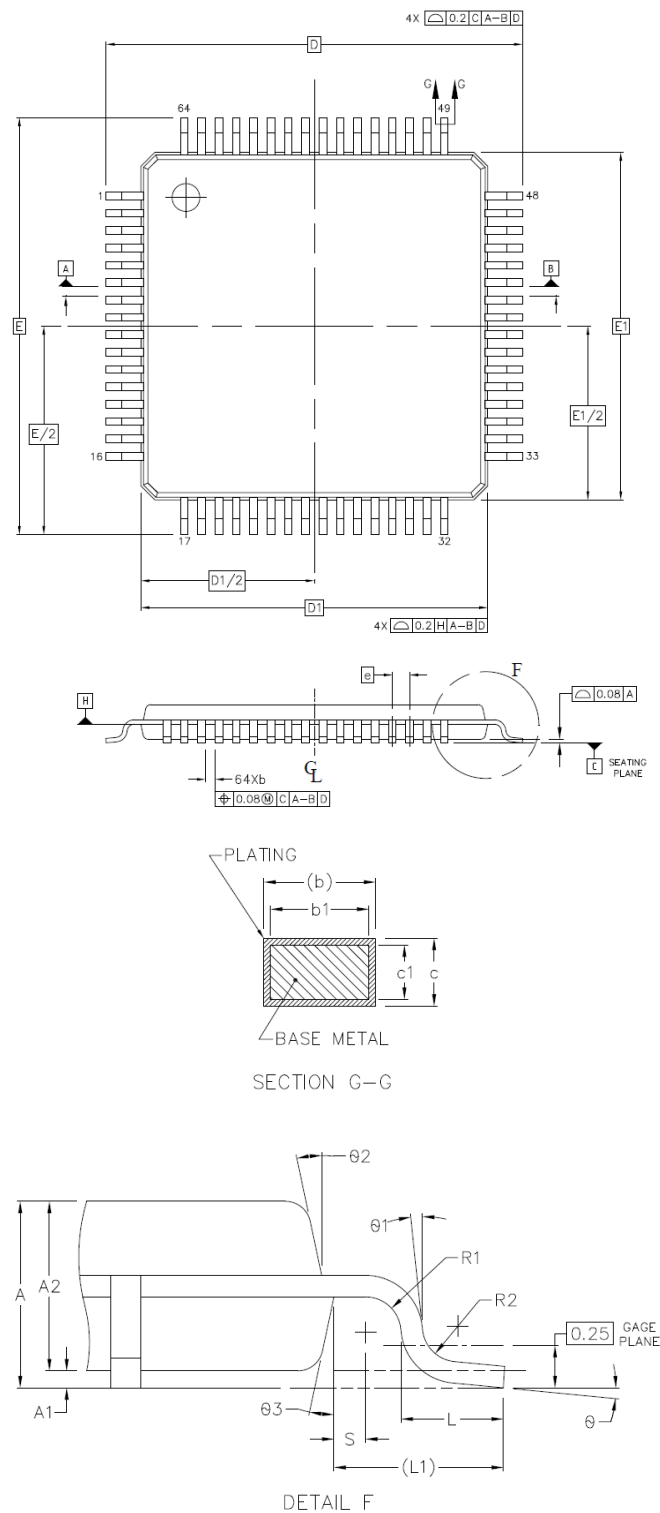# 8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions

Figure 8.1. TQFP64 Package Drawing

10.3 TQFP48 Package Marking

Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.