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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b140f64im64-ar

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1. Feature List

The EFM32TG11 highlighted features are listed below.

ARM Cortex-M0+ CPU platform

- High performance 32-bit processor @ up to 48 MHz
- Memory Protection Unit
- Wake-up Interrupt Controller
- Flexible Energy Management System
 - 37 µA/MHz in Active Mode (EM0)
 - 1.30 µA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- Integrated DC-DC buck converter
- Backup Power Domain
 - RTCC and retention registers in a separate power domain, available in all energy modes
 - Operation from backup battery when main power absent/ insufficient
- Up to 128 kB flash program memory
- Up to 32 kB RAM data memory
- Communication Interfaces
 - CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (24 MHz) operation on one instance
 - 1 × Universal Asynchronous Receiver/ Transmitter
 - 1 × Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - $2 \times I^2C$ Interface with SMBus support
 - Address recognition in EM3 Stop Mode

Up to 67 General Purpose I/O Pins

- Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
- Configurable peripheral I/O locations
- · 5 V tolerance on select pins
- Asynchronous external interrupts
- Output state retention and wake-up from Shutoff Mode
- Up to 8 Channel DMA Controller
- Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware Cryptography
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- Hardware CRC engine
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- Security Management Unit (SMU)
 - Fine-grained access control for on-chip peripherals
- Integrated Low-energy LCD Controller with up to 8 × 32 segments
 - Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- Ultra Low-Power Precision Analog Peripherals
 - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - On-chip temperature sensor
 - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Up to 2 × Analog Comparator (ACMP)
 - Up to 4 × Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
 - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

Timers/Counters

- 2 × 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
 - Dead-Time Insertion on one timer instance
- 2 × 32-bit Timer/Counter
- 32-bit Real Time Counter and Calendar (RTCC)
- 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
- 16-bit Low Energy Timer for waveform generation
- 16-bit Pulse Counter with asynchronous operation
- Watchdog Timer with dedicated RC oscillator
- Low Energy Sensor Interface (LESENSE)
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
 - Up to 16 inputs
- Ultra efficient Power-on Reset and Brown-Out Detector
- Debug Interface
 - 2-pin Serial Wire Debug interface
 - 4-pin JTAG interface
 - Micro Trace Buffer (MTB)

Pre-Programmed UART Bootloader

Wide Operating Range

- 1.8 V to 3.8 V single power supply
- Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
- Standard (-40 $^\circ C$ to 85 $^\circ C$ $T_A)$ and Extended (-40 $^\circ C$ to 125 $^\circ C$ $T_J)$ temperature grades available
- Packages
 - QFN32 (5x5 mm)
 - TQFP48 (7x7 mm)
 - QFN64 (9x9 mm)
 - TQFP64 (10x10 mm)
 - QFN80 (9x9 mm)
 - TQFP80 (12x12 mm)

3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.



Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Current consumption of pe- ripheral power domain 1, with voltage scaling enabled, DCDC in LP mode ³	IPD1_VS	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ⁴		0.18		μA
Current consumption of pe- ripheral power domain 2, with voltage scaling enabled, DCDC in LP mode ³	IPD2_VS	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ⁴		0.18		μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.

2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.

3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIM-SEL=1, ANASW=DVDD.

4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.

5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Frequency limits	f _{HFRCO_BAND}	FREQRANGE = 0, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 3, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 6, FINETUNIN- GEN = 0	TBD	_	TBD	MHz
		FREQRANGE = 7, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 8, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 10, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 11, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 12, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 13, FINETUNIN- GEN = 0	TBD		TBD	MHz



Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.



Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

Table 5.2. E	EFM32TG11B5xx ir	1 QFN80	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGVSS	38	Voltage regulator VSS	VREGSW	39	DCDC regulator switching node
VREGVDD	40	Voltage regulator VDD input	DVDD	41	Digital power supply.
DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	43	GPIO
PE5	44	GPIO	PE6	45	GPIO
PE7	46	GPIO	PC12	47	GPIO (5V)
PC13	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.4. EFM32TG11B3xx in QFP64 Device Pinout

Table 5.4. E	FM32TG11B3xx in	QFP64	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO



Figure 5.7. EFM32TG11B3xx in QFN64 Device Pinout

Table 5.7. E	EFM32TG11B3xx i	n QFN64	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO



Figure 5.10. EFM32TG11B3xx in QFP48 Device Pinout

Table 5.10. EFM32TG11B3xx in QFP48 Device Pinou

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 22 43	Digital IO power supply 0.
VSS	5 18 44	Ground	PB3	6	GPIO
PB4	7	GPIO	PB5	8	GPIO
PB6	9	GPIO	PC4	10	GPIO

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU- SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1
PE9	BUSCY BUSDX LCD_SEG5			
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE- TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL- TEX6 PRS_CH1 #3
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE- TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2	
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2	
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3	

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
LCD_SEG9	0: PE13		LCD segment line 9.
LCD_SEG10	0: PE14		LCD segment line 10.
LCD_SEG11	0: PE15		LCD segment line 11.
LCD_SEG12	0: PA15		LCD segment line 12.
LCD_SEG13	0: PA0		LCD segment line 13.
LCD_SEG14	0: PA1		LCD segment line 14.
LCD_SEG15	0: PA2		LCD segment line 15.
LCD_SEG16	0: PA3		LCD segment line 16.
LCD_SEG17	0: PA4		LCD segment line 17.
LCD_SEG18	0: PA5		LCD segment line 18.
LCD_SEG19	0: PA6		LCD segment line 19.
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5

Alternate	LOC	ATION		
Functionality	0 - 3	4 - 7	Description	
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9	Low Energy Timer LETIM0, output channel 1.	
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.	
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.	
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional ex- ternal clock input pin.	
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.	
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.	
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.	
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.	
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.	
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.	
OPA2_OUT	0: PD5		Operational Amplifier 2 output.	
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.	
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.	

Dimension	Min	Тур	Мах	
A	0.70	0.75	0.80	
A1	0.00	—	0.05	
b	0.20	0.25	0.30	
A3	0.203 REF			
D	9.00 BSC			
е	0.50 BSC			
E	9.00 BSC			
D2	7.10	7.20	7.30	
E2	7.10	7.20	7.30	
L	0.40	0.45	0.50	
L1	0.00	—	0.10	
ааа	0.10			
bbb	0.10			
ссс	0.10			
ddd	0.05			
eee	0.08			

Table 9.1. QFN64 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 QFN64 PCB Land Pattern



Figure 9.2. QFN64 PCB Land Pattern Drawing

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions



Dimension	Min	Тур	Мах	
A	7.00 BSC			
A1	3.50 BSC			
В	7.00 BSC			
B1	3.50 BSC			
С	1.00		1.20	
D	0.17	_	0.27	
E	0.95	_	1.05	
F	0.17	_	0.23	
G	0.50 BSC			
н	0.05	_	0.15	
J	0.09	_	0.20	
К	0.50	_	0.70	
L	0	_	7	
Μ	12 REF			
Ν	0.09	_	0.16	
Р	0.25 BSC			
R	0.150	_	0.250	
S	9.00 BSC			
S1	4.50 BSC			
V	9.00 BSC			
V1	4.50 BSC			
W	0.20 BSC			
AA	1.00 BSC			

Table 10.1. TQFP48 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.