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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b140f64iq64-a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.8	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V out- put, I_{DCDC_LOAD} = 10 mA	2.4	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I _{DCDC_LOAD} = 200 mA	2.6	_	V _{VREGVDD} MAX	V
Output voltage programma- ble range ¹	V _{DCDC_0}		1.8	_	V _{VREGVDD}	V
Regulation DC accuracy	ACC _{DC}	Low Noise (LN) mode, 1.8 V tar- get output	TBD		TBD	V
Regulation window ⁴	WIN _{REG}	Low Power (LP) mode, LPCMPBIASEMxx ³ = 0, 1.8 V tar- get output, I _{DCDC_LOAD} ≤ 75 µA	TBD	_	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx ³ = 3, 1.8 V tar- get output, I _{DCDC_LOAD} ≤ 10 mA	TBD	_	TBD	V
Steady-state output ripple	V _R		_	3	—	mVpp
Output voltage under/over- shoot	V _{OV}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	_	25	TBD	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	_	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions com- pared to DC level in LN mode	_	200	_	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	_	40	_	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode		100	_	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	_	0.1	_	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	_	0.1	—	%

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Max load current	ILOAD_MAX	Low noise (LN) mode, Heavy Drive ² , T ≤ 85 °C	_	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , T > 85 °C	—	_	100	mA
		Low noise (LN) mode, Medium Drive ²	_	_	100	mA
		Low noise (LN) mode, Light Drive ²	_	_	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	_	_	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	_	_	10	mA
DCDC nominal output ca- pacitor ⁵	C _{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output induc- tor	L _{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R _{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.

- 2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=15.
- 3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.

4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.

5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

4.1.8 Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
DVDD BOD threshold	V _{DVDDBOD}	DVDD rising	_	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	—	_	V
		DVDD falling (EM2/EM3)	TBD	_	_	V
DVDD BOD hysteresis	V _{DVDDBOD_HYST}		_	18	_	mV
DVDD BOD response time	tDVDDBOD_DELAY	Supply drops at 0.1V/µs rate	_	2.4	_	μs
AVDD BOD threshold	V _{AVDDBOD}	AVDD rising	_	_	TBD	V
		AVDD falling (EM0/EM1)	TBD		_	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	V _{AVDDBOD_HYST}		_	20	_	mV
AVDD BOD response time	t _{AVDDBOD_DELAY}	Supply drops at 0.1V/µs rate	_	2.4		μs
EM4 BOD threshold	V _{EM4DBOD}	AVDD rising	_	_	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V _{EM4BOD_HYST}		_	25	_	mV
EM4 BOD response time	t _{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	_	300	_	μs

Table 4.10. Brown Out Detector (BOD)

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal frequency	f _{HFXO}		4	—	48	MHz
Supported crystal equivalent	ESR _{HFXO}	48 MHz crystal	_	_	50	Ω
series resistance (ESR)		24 MHz crystal	_	_	150	Ω
		4 MHz crystal	—	—	180	Ω
Supported range of crystal load capacitance ¹	C _{HFXO_CL}		TBD	_	TBD	pF
Nominal on-chip tuning cap range ²	C _{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	8.7	_	51.7	pF
On-chip tuning capacitance step	SS _{HFXO}		_	0.08		pF
Startup time	t _{HFXO}	48 MHz crystal, ESR = 50 Ohm, C_L = 8 pF	_	350		μs
		24 MHz crystal, ESR = 150 Ohm, C_L = 6 pF	_	700	—	μs
		4 MHz crystal, ESR = 180 Ohm, C_L = 18 pF	_	3	_	ms
Current consumption after	I _{HFXO}	48 MHz crystal	—	880	_	μA
startup		24 MHz crystal		420	_	μA
		4 MHz crystal	_	80		μA

Table 4.12. High-Frequency Crystal Oscillator (HFXO)

Note:

1. Total load capacitance as seen by the crystal.

2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Hysteresis (V _{CM} = 1.25 V,	V _{ACMPHYST}	HYSTSEL ⁵ = HYST0	TBD	0	TBD	mV
$BIASPROG^{4} = 0x10, FULL-$ $BIAS^{4} = 1)$		HYSTSEL ⁵ = HYST1	TBD	18	TBD	mV
		HYSTSEL ⁵ = HYST2	TBD	33	TBD	mV
		HYSTSEL ⁵ = HYST3	TBD	46	TBD	mV
		HYSTSEL ⁵ = HYST4	TBD	57	TBD	mV
		HYSTSEL ⁵ = HYST5	TBD	68	TBD	mV
		HYSTSEL ⁵ = HYST6	TBD	79	TBD	mV
		HYSTSEL ⁵ = HYST7	TBD	90	TBD	mV
		HYSTSEL ⁵ = HYST8	TBD	0	TBD	mV
		HYSTSEL ⁵ = HYST9	TBD	-18	TBD	mV
		HYSTSEL ⁵ = HYST10	TBD	-33	TBD	mV
		HYSTSEL ⁵ = HYST11	TBD	-45	TBD	mV
		HYSTSEL ⁵ = HYST12	TBD	-57	TBD	mV
		HYSTSEL ⁵ = HYST13	TBD	-67	TBD	mV
		HYSTSEL ⁵ = HYST14	TBD	-78	TBD	mV
		HYSTSEL ⁵ = HYST15	TBD	-88	TBD	mV
Comparator delay ³	t _{ACMPDELAY}	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	_	30	_	μs
		$BIASPROG^4 = 0x10, FULLBIAS^4 = 0$	_	3.7	_	μs
		$BIASPROG^4 = 0x02, FULLBIAS^4 = 1$	_	360	_	ns
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	_	35	_	ns
Offset voltage	VACMPOFFSET	BIASPROG ⁴ =0x10, FULLBIAS ⁴ = 1	TBD	_	TBD	mV
Reference voltage	V _{ACMPREF}	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal re-	R _{CSRES}	CSRESSEL ⁶ = 0	—	infinite	_	kΩ
		CSRESSEL ⁶ = 1	—	15	—	kΩ
		CSRESSEL ⁶ = 2	—	27	—	kΩ
		CSRESSEL ⁶ = 3	—	39	_	kΩ
		CSRESSEL ⁶ = 4	—	51		kΩ
		CSRESSEL ⁶ = 5	—	100	—	kΩ
		CSRESSEL ⁶ = 6	—	162	—	kΩ
		CSRESSEL ⁶ = 7		235		kΩ

4.1.21.3 I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
SCL clock frequency ²	f _{SCL}		0	_	1000	kHz
SCL clock low time	t _{LOW}		0.5	_	_	μs
SCL clock high time	t _{HIGH}		0.26	_	_	μs
SDA set-up time	t _{SU_DAT}		50	_	—	ns
SDA hold time	t _{HD_DAT}		100	_	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	_	_	μs
(Repeated) START condition hold time	t _{HD_STA}		0.26	_	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	_	_	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Table 4.30. I2C Fast-mode Plus (Fm+)¹

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.

2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.



Figure 4.7. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz



Figure 4.8. DC-DC Converter Typical Performance Characteristics



Figure 5.6. EFM32TG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.6.	EFM32TG11B5xx	in QFN64	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 38	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO



Figure 5.11. EFM32TG11B1xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 22 43	Digital IO power supply 0.
VSS	5 18 44	Ground	PC0	6	GPIO (5V)
PC1	7	GPIO (5V)	PC2	8	GPIO (5V)
PC3	9	GPIO (5V)	PC4	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB7	11	GPIO	PB8	12	GPIO
PA8	13	GPIO	PA9	14	GPIO
PA10	15	GPIO	RESETn	16	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	17	GPIO	AVDD	19 23	Analog power supply.
PB13	20	GPIO	PB14	21	GPIO
PD4	24	GPIO	PD5	25	GPIO
PD6	26	GPIO	PD7	27	GPIO
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC8	30	GPIO	PC9	31	GPIO
PC10	32	GPIO (5V)	PC11	33	GPIO (5V)
PC13	34	GPIO (5V)	PC14	35	GPIO (5V)
PC15	36	GPIO (5V)	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			
Note:		·			·

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description												
	Analog	Timers	Communication	Other									
PC4	BUSACMP0Y BU- SACMP0X OPA0_P LCD_SEG24	TIM0_CC0 #5 TIM0_CDTI2 #3 LE- TIM0_OUT0 #3	US2_CLK #0 U0_TX #4 I2C1_SDA #0	LES_CH4 GPIO_EM4WU6									
PC5	BUSACMP0Y BU- SACMP0X OPA0_N LCD_SEG25	TIM0_CC1 #5 LE- TIM0_OUT1 #3	US2_CS #0 U0_RX #4 I2C1_SCL #0	LES_CH5									
PB7	LFXTAL_P	TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 U0_CTS #4										
PB8	LFXTAL_N	TIM0_CDTI1 #4 TIM1_CC1 #3	US0_RX #4 US1_CS #0 U0_RTS #4	CMU_CLKI0 #2									
PA8	BU_STAT	TIM0_CC0 #6 LE- TIM0_OUT0 #6	US2_RX #2										
PA9	BUSAY BUSBX LCD_SEG26	TIM0_CC1 #6 LE- TIM0_OUT1 #6	US2_CLK #2										
PA10	BUSBY BUSAX LCD_SEG27	TIM0_CC2 #6	US2_CS #2										
PA12	BU_VOUT	WTIM0_CDTI0 #2	US0_CLK #5 US2_RTS #2	CMU_CLK0 #5 ACMP1_O #3									
PA13	BUSAY BUSBX	TIM0_CC2 #7 WTIM0_CDTI1 #2	US0_CS #5 US2_TX #3										
PA14	BUSBY BUSAX LCD_BEXT	WTIM0_CDTI2 #2	US1_TX #6 US2_RX #3 US3_RTS #2	ACMP1_O #4									
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT LCD_SEG28	TIM0_CDTI2 #4 TIM1_CC2 #3 LE- TIM0_OUT0 #1 PCNT0_S1IN #7	US0_CTS #5 US1_CLK #5 US2_CS #3 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLKI0 #7 ACMP0_O #3 GPIO_EM4WU7									
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT LCD_SEG29	TIM1_CC3 #3 LE- TIM0_OUT1 #1 PCNT0_S0IN #7	US2_CTS #1 I2C1_SCL #1										
PB13	BUSAY BUSBX HFXTAL_P	WTIM1_CC0 #0	US0_CLK #4 US1_CTS #5 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0									
PB14	BUSBY BUSAX HFXTAL_N	WTIM1_CC1 #0	US0_CS #4 US1_RTS #5 LEU0_RX #1	PRS_CH6 #1									
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU- SADC0Y BUSADC0X	WTIM1_CC2 #0	CAN0_RX #2 US1_TX #1										
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BU- SADC0Y BUSADC0X OPA3_OUT	TIM0_CC0 #2 WTIM1_CC3 #0	CAN0_TX #2 US1_RX #1										
PD2	BUSADC0Y BUSADC0X	TIM0_CC1 #2 WTIM1_CC0 #1	US1_CLK #1										
PD3	BUSADC0Y BUSADC0X OPA2_N LCD_SEG30	TIM0_CC2 #2 WTIM1_CC1 #1	US1_CS #1										
PD4	BUSADC0Y BUSADC0X OPA2_P LCD_SEG31	WTIM0_CDTI0 #4 WTIM1_CC2 #1	US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0									

Alternate	LOC	ATION										
Functionality	0 - 3	4 - 7	Description									
U0_TX	2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.									
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12	USART0 clock input / output.									
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13	USART0 chip select input / output.									
US0_CTS	0: PE14 2: PC7 3: PC13	4: PB6 5: PB11	USART0 Clear To Send hardware flow control input.									
US0_RTS	0: PE15 2: PC6 3: PC12	4: PB5 5: PD6	USART0 Request To Send hardware flow control output.									
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).									
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0	USART0 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART0 Synchronous mode Master Output / Slave Input (MOSI).									
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.									
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4	USART1 chip select input / output.									
US1_CTS	1: PD4 2: PF3 3: PC6	4: PC12 5: PB13	USART1 Clear To Send hardware flow control input.									
US1_RTS	1: PD5 2: PF4 3: PC7	4: PC13 5: PB14	USART1 Request To Send hardware flow control output.									
US1_RX	0: PC1 1: PD1 2: PD6	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).									
US1_TX	0: PC0 1: PD0 2: PD7	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART1 Synchronous mode Master Output / Slave Input (MOSI).									

Alternate	LOCA	ATION									
Functionality	0 - 3	4 - 7	Description								
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.								
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.								
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.								
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.								
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.								
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.								
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.								
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.								
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.								
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.								
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.								
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.								
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.								

Alternate	LOCA	ATION	
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
ОР	A2_	<u>_</u> OU [.]	Г																														
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	βUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
ОР	A2_	<u>P</u>																															
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OP	A3_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PFO		PE14		PE12		PE10		PE8		PE6		PE4				

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
OP	A3_	00	Г																														
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OP	A3_	<u></u> P																															
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
VD	AC	0_0	JT0	/ 0	PA0	_οι	JT																										
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

6.2 TQFP80 PCB Land Pattern



Figure 6.2. TQFP80 PCB Land Pattern Drawing

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions



Figure 8.1. TQFP64 Package Drawing