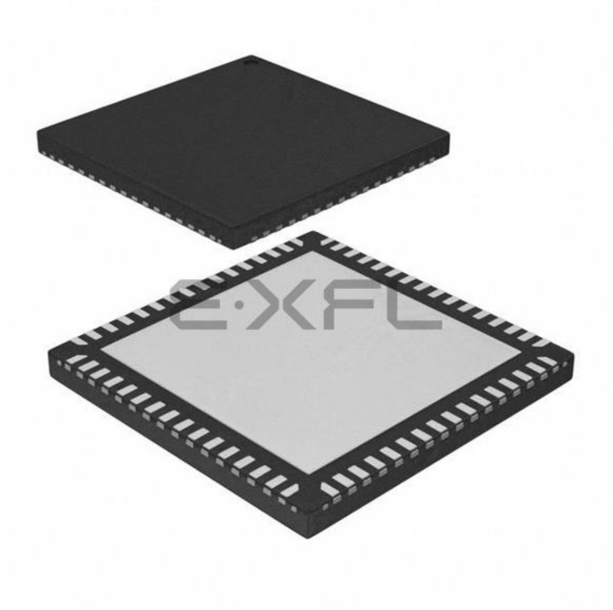
Silicon Labs - EFM32TG11B320F128GM64-AR Datasheet



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Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b320f128gm64-ar

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128IQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

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3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

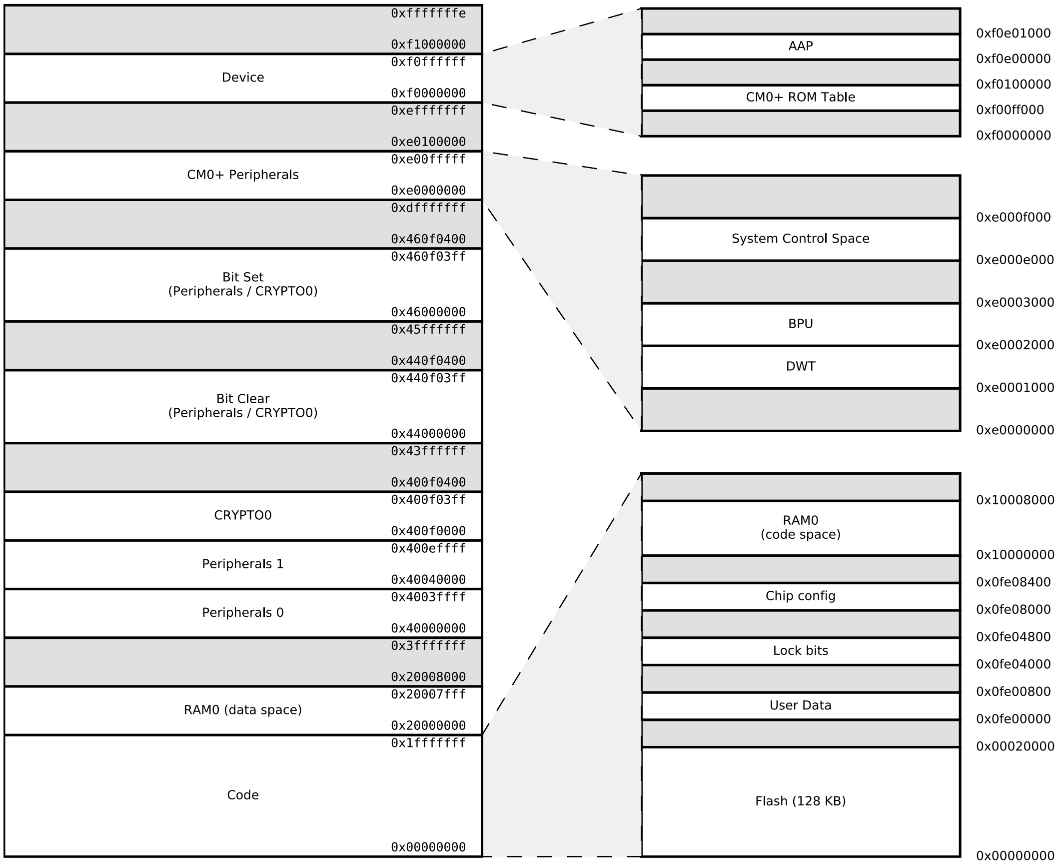


Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$. 2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate. 3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias. 4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor). 5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD. 6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.						

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	—	°C/W
Thermal resistance, TQFP48 Package	$THETA_{JA\_TQFP48}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	43.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	—	°C/W
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	37.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	35.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	—	°C/W
Thermal resistance, QFN80 Package	$THETA_{JA\_QFN80}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP80 Package	$THETA_{JA\_TQFP80}$	4-Layer PCB, Air velocity = 0 m/s	—	49.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	44.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.6	—	°C/W

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	10	TBD	nA
		BU_VIN powering backup domain[1]	—	450	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 48 MHz	—	258	TBD	µA
		f_{HFRCO} = 38 MHz	—	218	TBD	µA
		f_{HFRCO} = 32 MHz	—	182	TBD	µA
		f_{HFRCO} = 26 MHz	—	156	TBD	µA
		f_{HFRCO} = 19 MHz	—	130	TBD	µA
		f_{HFRCO} = 16 MHz	—	112	TBD	µA
		f_{HFRCO} = 13 MHz	—	101	TBD	µA
		f_{HFRCO} = 7 MHz	—	80	TBD	µA
		f_{HFRCO} = 4 MHz	—	29	TBD	µA
		f_{HFRCO} = 2 MHz	—	26	TBD	µA
		f_{HFRCO} = 1 MHz	—	24	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	393	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	313	TBD	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	180	TBD	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	46	TBD	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	33	TBD	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.11 General-Purpose I/O (GPIO)

Table 4.18. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns

4.1.12 Voltage Monitor (VMON)

Table 4.19. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.3	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	12.5	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.19 Pulse Counter (PCNT)

Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

4.1.21.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.30. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

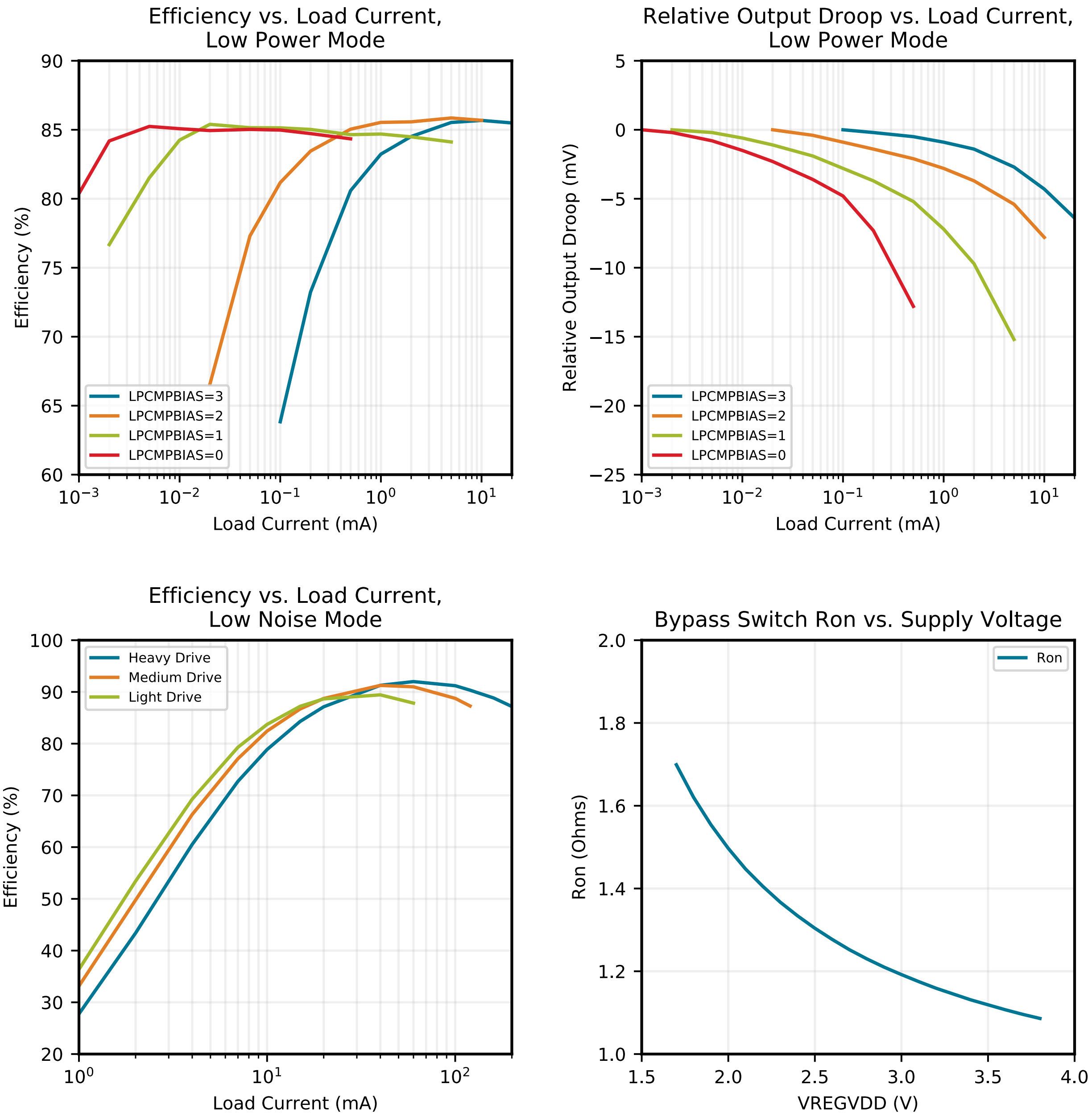


Figure 4.8. DC-DC Converter Typical Performance Characteristics

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB4	10	GPIO	PB5	11	GPIO
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.7 EFM32TG11B3xx in QFN64 Device Pinout

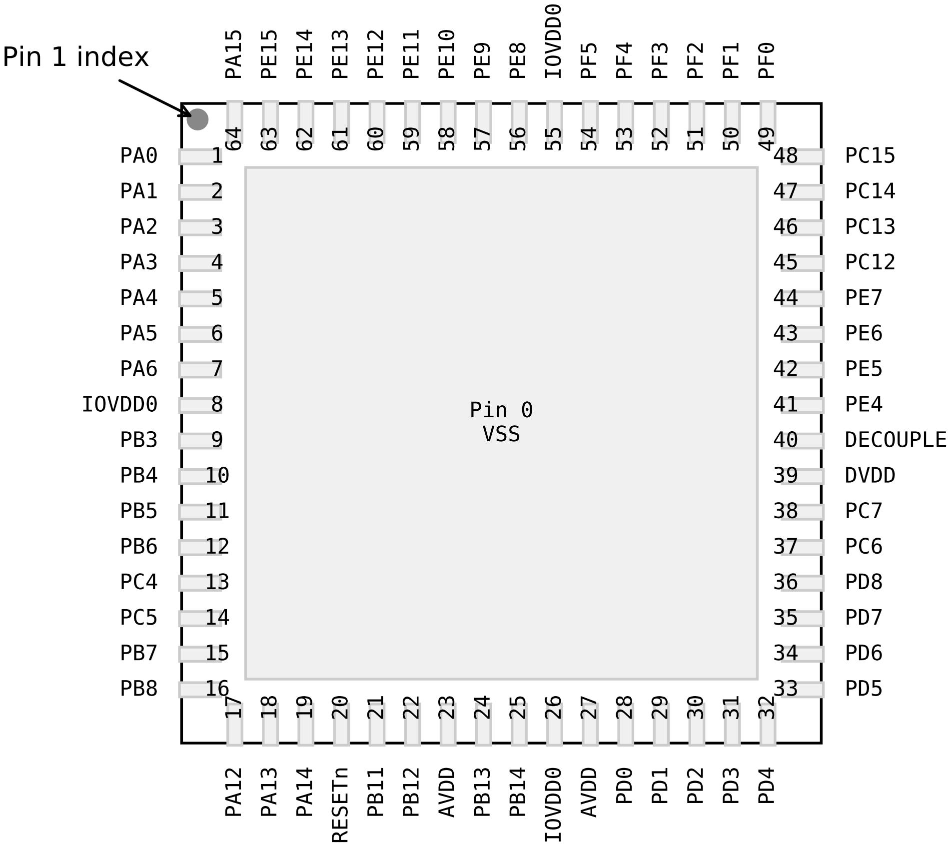


Figure 5.7. EFM32TG11B3xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.7. EFM32TG11B3xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

5.12 EFM32TG11B5xx in QFN32 Device Pinout

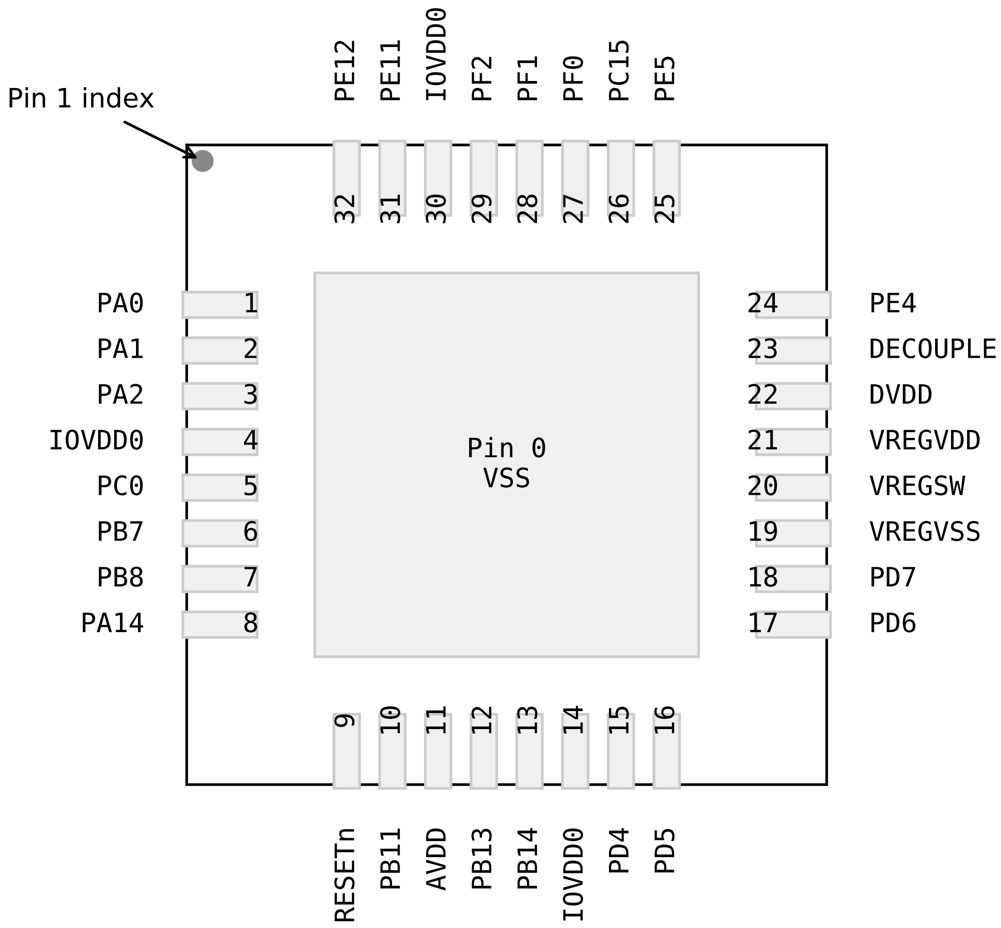


Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 3: PA13	5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4		USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0		USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6		USART3 Clear To Send hardware flow control input.
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15		USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7		USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3		USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

7.3 QFN80 Package Marking

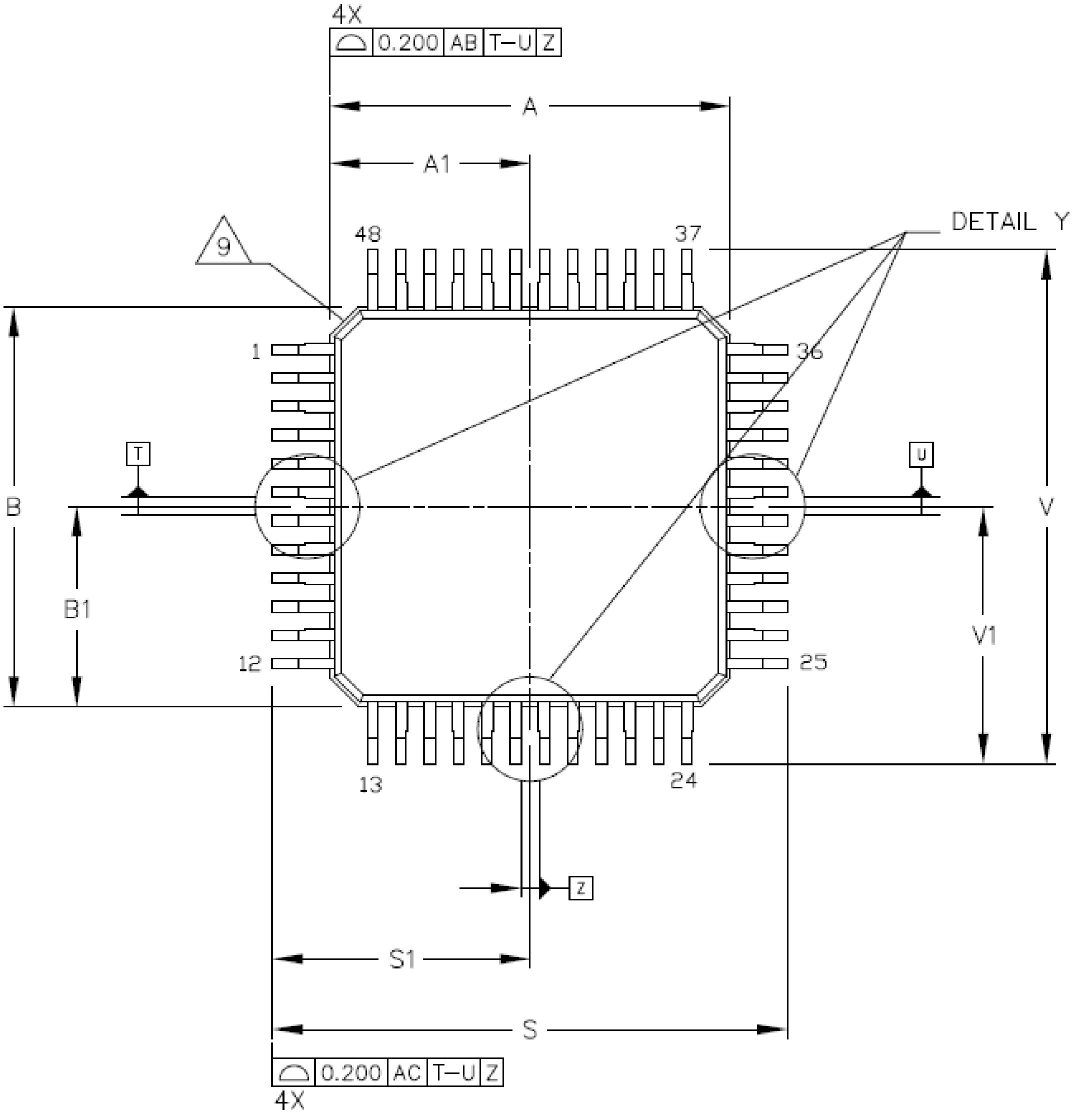
Figure 7.3. QFN80 Package Marking

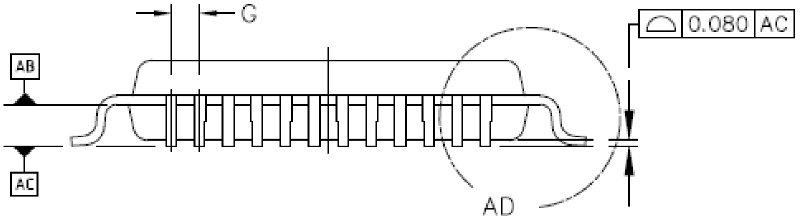
The package marking consists of:

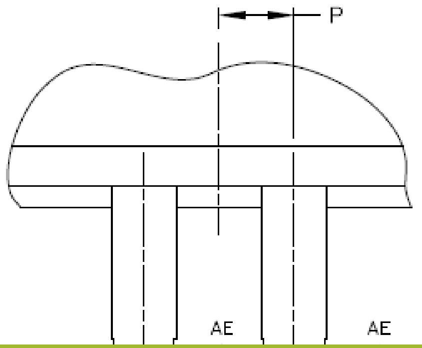
- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions







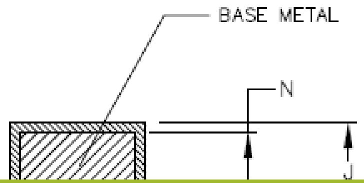


Table 11.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	5.0 BSC		
D2/E2	3.60	3.70	3.80
E	5.0 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Revision History

Revision 0.5

February, 2018

- 4.1 Electrical Characteristics updated with latest characterization data and production test limits.
- Added 4.1.3 Thermal Characteristics.
- Added 4.2 Typical Performance Curves section.
- Corrected OPA / VDAC output connections in Figure 5.14 APORT Connection Diagram on page 119.

Revision 0.1

May 1st, 2017

Initial release.