# E·XFL



#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b320f128iq48-ar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 2.1. Ordering Code Key

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit		
Note:								
1. The minimum voltage req other loads can be calcula	<ol> <li>The minimum voltage required in bypass mode is calculated using R<sub>BYP</sub> from the DCDC specification table. Requirements for other loads can be calculated as V<sub>DVDD min</sub>+I<sub>LOAD</sub> * R<sub>BYP max</sub>.</li> </ol>							
2. VREGVDD must be tied t	o AVDD. Both VRI	EGVDD and AVDD minimum voltage	es must be sa	tisfied for the	part to operat	e.		
<ol> <li>The system designer sho ue stays within the specifi</li> </ol>	uld consult the cha ied bounds across	racteristic specs of the capacitor use temperature and DC bias.	ed on DECOL	JPLE to ensur	e its capacita	nce val-		
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transi- tion, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).								
5. When the CSEN peripher	al is used with cho	pping enabled (CSEN_CTRL_CHOF	PEN = ENABI	LE), IOVDD m	ust be equal	to AVDD.		
6. The maximum limit on $T_A$ may be lower due to device self-heating, which depends on the power dissipation of the specific appli- cation. $T_A$ (max) = $T_J$ (max) - (THETA <sub>JA</sub> x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for $T_J$ and THETA <sub>JA</sub> .								

# 4.1.3 Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Thermal resistance, QFN32	THETA <sub>JA_QFN32</sub>	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	23.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	_	°C/W
Thermal resistance, TQFP48	THE-	4-Layer PCB, Air velocity = 0 m/s	—	44.1	_	°C/W
Раскаде	IAJA_TQFP48	4-Layer PCB, Air velocity = 1 m/s	—	43.5	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	_	°C/W
Thermal resistance, QFN64	THETA <sub>JA_QFN64</sub>	4-Layer PCB, Air velocity = 0 m/s	—	20.9	_	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	18.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	_	°C/W
Thermal resistance, TQFP64	THE-	4-Layer PCB, Air velocity = 0 m/s	—	37.3	_	°C/W
Раскаде	IAJA_TQFP64	4-Layer PCB, Air velocity = 1 m/s	—	35.6	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	_	°C/W
Thermal resistance, QFN80	THETA <sub>JA_QFN80</sub>	4-Layer PCB, Air velocity = 0 m/s	—	20.9	_	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	18.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	_	°C/W
Thermal resistance, TQFP80	THE-	4-Layer PCB, Air velocity = 0 m/s	—	49.3	_	°C/W
Раскаде	IAJA_TQFP80	4-Layer PCB, Air velocity = 1 m/s	—	44.5	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s		42.6		°C/W

# Table 4.3. Thermal Characteristics

# 4.1.10 Flash Memory Characteristics<sup>5</sup>

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Flash erase cycles before failure	EC <sub>FLASH</sub>		10000	—		cycles
Flash data retention	RET <sub>FLASH</sub>	T ≤ 85 °C	10	—	_	years
		T ≤ 125 °C	10	—	_	years
Word (32-bit) programming time	t <sub>W_PROG</sub>	Burst write, 128 words, average time per word	20	26	32	μs
		Single word	59	68	83	μs
Page erase time <sup>4</sup>	t <sub>PERASE</sub>		20	27	35	ms
Mass erase time <sup>1</sup>	t <sub>MERASE</sub>		20	27	35	ms
Device erase time <sup>2 3</sup>	t <sub>DERASE</sub>	T ≤ 85 °C	—	54	70	ms
		T ≤ 125 °C	—	54	75	ms
Erase current <sup>6</sup>	I <sub>ERASE</sub>	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.0	mA
Write current <sup>6</sup>	I <sub>WRITE</sub>		_	_	3.5	mA
Supply voltage during flash erase and write	V <sub>FLASH</sub>		1.62		3.6	V

# Table 4.17. Flash Memory Characteristics<sup>5</sup>

# Note:

- 1. Mass erase is issued by the CPU and erases all flash.
- 2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
- 3. From setting the DEVICEERASE bit in AAP\_CMD to 1 until the ERASEBUSY bit in AAP\_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- 4. From setting the ERASEPAGE bit in MSC\_WRITECMD to 1 until the BUSY bit in MSC\_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- 5. Flash data retention information is published in the Quarterly Quality and Reliability Report.

6. Measured at 25 °C.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Note:								
<ol> <li>Supply current specification the load.</li> </ol>	1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.							
2. In differential mode, the o limited to the single-ender	utput is defined as d range.	the difference between two single-e	nded outputs	. Absolute vol	tage on each	output is		
3. Entire range is monotonic	and has no missir	ng codes.						
<ol> <li>Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.</li> </ol>								
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale with the measured gain.								
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$ , VDAC output at 90% of full scale								

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
SCLK period <sup>1 3 2</sup>	t <sub>SCLK</sub>		6 * t <sub>HFPERCLK</sub>	—	_	ns
SCLK high time <sup>1 3 2</sup>	t <sub>SCLK_HI</sub>		2.5 * t <sub>HFPERCLK</sub>	_	_	ns
SCLK low time <sup>1 3 2</sup>	t <sub>SCLK_LO</sub>		2.5 * t <sub>HFPERCLK</sub>	—	—	ns
CS active to MISO <sup>1 3</sup>	t <sub>CS_ACT_MI</sub>		20	_	70	ns
CS disable to MISO <sup>1 3</sup>	t <sub>CS_DIS_MI</sub>		15		150	ns
MOSI setup time <sup>1 3</sup>	t <sub>SU_MO</sub>		4		_	ns
MOSI hold time <sup>1 3 2</sup>	t <sub>H_MO</sub>		7	_	_	ns
SCLK to MISO <sup>1 3 2</sup>	t <sub>SCLK_MI</sub>		14 + 1.5 * t <sub>HFPERCLK</sub>	_	40 + 2.5 * t <sub>HFPERCLK</sub>	ns

# Table 4.32. SPI Slave Timing

### Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2.  $t_{\mbox{\scriptsize HFPERCLK}}$  is one period of the selected  $\mbox{\scriptsize HFPERCLK}.$ 

3. Measurement done with 8 pF output loading at 10% and 90% of  $V_{DD}$  (figure shows 50% of  $V_{DD}$ ).



Figure 4.2. SPI Slave Timing Diagram

# 4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.



Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description	
PE15	79	GPIO	PA15	80	GPIO	
Note: 1. GPIO with 5V tolerance are indicated by (5V).						



#### Figure 5.6. EFM32TG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.6.	EFM32TG11B5xx	in QFN64	Device	Pinout
------------	---------------	----------	--------	--------

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 38	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:					

1. GPIO with 5V tolerance are indicated by (5V).



#### Figure 5.8. EFM32TG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)



## Figure 5.13. EFM32TG11B1xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.13. EFM32TG1	1B1xx in QFN32	<b>Device Pinout</b>
----------------------	----------------	----------------------

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 28	Digital IO power supply 0.	PC0	5	GPIO (5V)
PC1	6	GPIO (5V)	PB7	7	GPIO

#### 5.15 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.14 GPIO Functionality Table for a list of functions available on each GPIO pin.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Alternate	LOC	ATION	
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 2: PD6 3: PB11	4: PA6 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 2: PD7 3: PA12	4: PA14 7: PA5	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.
BU_STAT	0: PA8		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PA12		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0		CAN0 RX.

#### Table 5.15. Alternate Functionality Overview

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
LCD_SEG9	0: PE13		LCD segment line 9.
LCD_SEG10	0: PE14		LCD segment line 10.
LCD_SEG11	0: PE15		LCD segment line 11.
LCD_SEG12	0: PA15		LCD segment line 12.
LCD_SEG13	0: PA0		LCD segment line 13.
LCD_SEG14	0: PA1		LCD segment line 14.
LCD_SEG15	0: PA2		LCD segment line 15.
LCD_SEG16	0: PA3		LCD segment line 16.
LCD_SEG17	0: PA4		LCD segment line 17.
LCD_SEG18	0: PA5		LCD segment line 18.
LCD_SEG19	0: PA6		LCD segment line 19.
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5

Alternate	LOC	ATION								
Functionality	0 - 3	0-3 4-7 Description								
U0_TX	2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.							
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12	USART0 clock input / output.							
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13	USART0 chip select input / output.							
US0_CTS	0: PE14 2: PC7 3: PC13	4: PB6 5: PB11	USART0 Clear To Send hardware flow control input.							
US0_RTS	0: PE15 2: PC6 3: PC12	4: PB5 5: PD6	USART0 Request To Send hardware flow control output.							
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).							
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0	USART0 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART0 Synchronous mode Master Output / Slave Input (MOSI).							
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.							
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4	USART1 chip select input / output.							
US1_CTS	1: PD4 2: PF3 3: PC6	4: PC12 5: PB13	USART1 Clear To Send hardware flow control input.							
US1_RTS	1: PD5 2: PF4 3: PC7	4: PC13 5: PB14	USART1 Request To Send hardware flow control output.							
US1_RX	0: PC1 1: PD1 2: PD6	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).							
US1_TX	0: PC0 1: PD0 2: PD7	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART1 Synchronous mode Master Output / Slave Input (MOSI).							

Alternate	LOCA	ATION						
Functionality	0 - 3	4 - 7	Description					
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	5: PF2	USART2 clock input / output.					
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	5: PF5	USART2 chip select input / output.					
US2_CTS	0: PC1 1: PB12	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.					
US2_RTS	0: PC0 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.					
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).					
US2_TX	0: PC2 1: PB3	5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communica- tion.					
	3: PA13		USART2 Synchronous mode Master Output / Slave Input (MOSI).					
US3_CLK	0: PA2 1: PD7 2: PD4		USART3 clock input / output.					
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0		USART3 chip select input / output.					
US3_CTS	0: PA4 1: PE5 2: PD6		USART3 Clear To Send hardware flow control input.					
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15		USART3 Request To Send hardware flow control output.					
US3_RX	0: PA1 1: PE7 2: PB7		USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).					
US3_TX	0: PA0 1: PE6 2: PB3		USART3 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART3 Synchronous mode Master Output / Slave Input (MOSI).					
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.					

Port	Bus	CH31	СНЗС	CH26	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH16	CH18	CH17	CH16	CH1	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	9HC	CH5	CH4	СНЗ	CH2	CH1	СНО
CE	CEXT																																
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
<b>APORT1Y</b>	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
<b>APORT3X</b>	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
<b>APORT3Y</b>	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
CE	хт_	SEN	ISE																														
<b>APORT2X</b>	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
<b>APORT2Y</b>	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

# Table 5.19. CSEN Bus and Pin Mapping

# 6. TQFP80 Package Specifications

# 6.1 TQFP80 Package Dimensions



Figure 6.1. TQFP80 Package Drawing

#### Table 8.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max						
C1	11.30	11.40						
C2	11.30	11.40						
E	0.50 BSC							
x	0.20	0.30						
Y	1.40	1.50						

#### Note:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.
- 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
- 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

#### 8.3 TQFP64 Package Marking



Figure 8.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.



Figure 9.3. QFN64 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.



Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.