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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b320f128iq64-ar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con- verter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128lQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Max load current	ILOAD_MAX	Low noise (LN) mode, Heavy Drive ² , T ≤ 85 °C	_	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , T > 85 °C	—	_	100	mA
		Low noise (LN) mode, Medium Drive ²	_		100	mA
		Low noise (LN) mode, Light Drive ²	_	_	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	_	_	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	_	_	10	mA
DCDC nominal output ca- pacitor ⁵	C _{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output induc- tor	L _{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R _{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.

- 2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=15.
- 3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.

4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.

5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frequency accuracy	fhfrco_acc	At production calibrated frequen- cies, across supply voltage and temperature	TBD	_	TBD	%
Start-up time	t _{HFRCO}	f _{HFRCO} ≥ 19 MHz	—	300	—	ns
		4 < f _{HFRCO} < 19 MHz	_	1	—	μs
		f _{HFRCO} ≤ 4 MHz	—	2.5	—	μs
Current consumption on all	I _{HFRCO}	f _{HFRCO} = 48 MHz	—	258	TBD	μA
supplies		f _{HFRCO} = 38 MHz	_	218	TBD	μA
		f _{HFRCO} = 32 MHz	_	182	TBD	μA
		f _{HFRCO} = 26 MHz	_	156	TBD	μA
		f _{HFRCO} = 19 MHz	_	130	TBD	μA
		f _{HFRCO} = 16 MHz	_	112	TBD	μA
		f _{HFRCO} = 13 MHz	_	101	TBD	μA
		f _{HFRCO} = 7 MHz	_	80	TBD	μA
		f _{HFRCO} = 4 MHz	_	29	TBD	μA
		f _{HFRCO} = 2 MHz	_	26	TBD	μA
		f _{HFRCO} = 1 MHz	_	24	TBD	μA
		f _{HFRCO} = 40 MHz, DPLL enabled	—	393	TBD	μA
		f _{HFRCO} = 32 MHz, DPLL enabled	—	313	TBD	μA
		f _{HFRCO} = 16 MHz, DPLL enabled	—	180	TBD	μA
		f _{HFRCO} = 4 MHz, DPLL enabled	_	46	TBD	μA
		f _{HFRCO} = 1 MHz, DPLL enabled	—	33	TBD	μA
Coarse trim step size (% of period)	SS _{HFRCO_COARS}		—	0.8	_	%
Fine trim step size (% of pe- riod)	SS _{HFRCO_FINE}			0.1		%
Period jitter	PJ _{HFRCO}			0.2		% RMS

Table 4.14. High-Frequency RC Oscillator (HFRCO)

4.1.16 Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Single conversion time (1x	t _{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	_	μs
		Delta Modulation Conversion (sin- gle comparison)		1.55	-	μs
Maximum external capacitive load	C _{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics		68	_	pF
		CS0CG=0 (Gain = 10x), including routing parasitics		680	_	pF
Maximum external series impedance	R _{EXTMAX}		—	1	-	kΩ
Supply current, EM2 bonded conversions, WARMUP- MODE=NORMAL, WAR- MUPCNT=0	ICSEN_BOND	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	_	326	_	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	_	226	_	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹		33	_	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 chan- nels bonded (total capacitance of 330 pF) ¹	_	25	_	nA
Supply current, EM2 scan conversions, WARMUP- MODE=NORMAL, WAR-	ICSEN_EM2	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹		690	_	nA
MUPCNT=0		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 sam- ples per scan ¹	_	515	_	nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹	_	79	_	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹	_	57		nA

Table 4.23. Capacitive Sense (CSEN)

4.1.19 Pulse Counter (PCNT)

Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input frequency	F _{IN}	Asynchronous Single and Quad- rature Modes		_	20	MHz
		Sampled Modes with Debounce filter set to 0.	_	_	8	kHz

4.1.20 Analog Port (APORT)

Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current ^{2 1}	I _{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	_	915	_	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

4.1.21 I2C

4.1.21.1 I2C Standard-mode (Sm)¹

Table 4.28. I2C Standard-mode (Sm

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCL clock frequency ²	f _{SCL}		0	_	100	kHz
SCL clock low time	t _{LOW}		4.7	_	_	μs
SCL clock high time	t _{HIGH}		4	—	—	μs
SDA set-up time	t _{SU_DAT}		250	_	_	ns
SDA hold time ³	t _{HD_DAT}		100	_	3450	ns
Repeated START condition set-up time	t _{SU_STA}		4.7	_	_	μs
(Repeated) START condition hold time	t _{HD_STA}		4	_	_	μs
STOP condition set-up time	t _{SU_STO}		4	_	_	μs
Bus free time between a STOP and START condition	t _{BUF}		4.7		_	μs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.

2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.

3. The maximum SDA hold time (t_{HD DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
SCLK period ^{1 3 2}	t _{SCLK}		6 * t _{HFPERCLK}	—	_	ns
SCLK high time ^{1 3 2}	t _{SCLK_HI}		2.5 * t _{HFPERCLK}	_	_	ns
SCLK low time ^{1 3 2}	t _{SCLK_LO}		2.5 * t _{HFPERCLK}	—	—	ns
CS active to MISO ^{1 3}	t _{CS_ACT_MI}		20	_	70	ns
CS disable to MISO ^{1 3}	t _{CS_DIS_MI}		15		150	ns
MOSI setup time ^{1 3}	t _{SU_MO}		4		_	ns
MOSI hold time ^{1 3 2}	t _{H_MO}		7	_	_	ns
SCLK to MISO ^{1 3 2}	t _{SCLK_MI}		14 + 1.5 * t _{HFPERCLK}	_	40 + 2.5 * t _{HFPERCLK}	ns

Table 4.32. SPI Slave Timing

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2. $t_{\mbox{\scriptsize HFPERCLK}}$ is one period of the selected $\mbox{\scriptsize HFPERCLK}.$

3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).



Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.



Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.



Figure 4.9. DC-DC Converter Transition Waveforms

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	9 24 51 70	Ground	PB3	10	GPIO
PB4	11	GPIO	PB5	12	GPIO
PB6	13	GPIO	PC1	14	GPIO (5V)
PC2	15	GPIO (5V)	PC3	16	GPIO (5V)
PC4	17	GPIO	PC5	18	GPIO
PB7	19	GPIO	PB8	20	GPIO
PA8	21	GPIO	PA9	22	GPIO
PA10	23	GPIO	PA12	25	GPIO
PA14	26	GPIO	RESETn	27	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	28	GPIO	PB12	29	GPIO
AVDD	30 34	Analog power supply.	PB13	31	GPIO
PB14	32	GPIO	PD0	35	GPIO (5V)
PD1	36	GPIO	PD3	37	GPIO
PD4	38	GPIO	PD5	39	GPIO
PD6	40	GPIO	PD7	41	GPIO
PD8	42	GPIO	PC6	43	GPIO
PC7	44	GPIO	VREGVSS	45	Voltage regulator VSS
VREGSW	46	DCDC regulator switching node	VREGVDD	47	Voltage regulator VDD input
DVDD	48	Digital power supply.	DECOUPLE	49	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	52	GPIO	PE5	53	GPIO
PE6	54	GPIO	PE7	55	GPIO
PC8	56	GPIO	PC9	57	GPIO
PC10	58	GPIO (5V)	PC11	59	GPIO (5V)
PC13	60	GPIO (5V)	PC14	61	GPIO (5V)
PC15	62	GPIO (5V)	PF0	63	GPIO (5V)
PF1	64	GPIO (5V)	PF2	65	GPIO
PF3	66	GPIO	PF4	67	GPIO
PF5	68	GPIO	PE8	71	GPIO
PE9	72	GPIO	PE10	73	GPIO
PE11	74	GPIO	BODEN	75	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB4	10	GPIO	PB5	11	GPIO
PB6	12	GPIO	PC0	13	GPIO (5V)
PC1	14	GPIO (5V)	PC2	15	GPIO (5V)
PC3	16	GPIO (5V)	PC4	17	GPIO
PC5	18	GPIO	PB7	19	GPIO
PB8	20	GPIO	PA8	21	GPIO
PA9	22	GPIO	PA10	23	GPIO
PA12	24	GPIO	PA13	25	GPIO (5V)
PA14	26	GPIO	RESETn	27	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	28	GPIO	PB12	29	GPIO
AVDD	30 34	Analog power supply.	PB13	31	GPIO
PB14	32	GPIO	PD0	35	GPIO (5V)
PD1	36	GPIO	PD2	37	GPIO (5V)
PD3	38	GPIO	PD4	39	GPIO
PD5	40	GPIO	PD6	41	GPIO
PD7	42	GPIO	PD8	43	GPIO
PC6	44	GPIO	PC7	45	GPIO
VREGSW	47	DCDC regulator switching node	VREGVDD	48	Voltage regulator VDD input
DVDD	49	Digital power supply.	DECOUPLE	50	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	52	GPIO	PE5	53	GPIO
PE6	54	GPIO	PE7	55	GPIO
PC8	56	GPIO	PC9	57	GPIO
PC10	58	GPIO (5V)	PC11	59	GPIO (5V)
PC12	60	GPIO (5V)	PC13	61	GPIO (5V)
PC14	62	GPIO (5V)	PC15	63	GPIO (5V)
PF0	64	GPIO (5V)	PF1	65	GPIO (5V)
PF2	66	GPIO	PF3	67	GPIO
PF4	68	GPIO	PF5	69	GPIO
PE8	71	GPIO	PE9	72	GPIO
PE10	73	GPIO	PE11	74	GPIO
BODEN	75	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	PE12	76	GPIO
PE13	77	GPIO	PE14	78	GPIO



Figure 5.3. EFM32TG11B5xx in QFP64 Device Pinout

Table 5.3. EFM32TO	11B5xx in QF	P64 Device Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO



Figure 5.8. EFM32TG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:	-			-	

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.9. EFM32TG11B5xx in QFP48 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 21 43	Digital IO power supply 0.
VSS	5 17 44	Ground	PB3	6	GPIO
PB4	7	GPIO	PB5	8	GPIO
PB6	9	GPIO	PB7	10	GPIO



Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO



Figure 5.13. EFM32TG11B1xx in QFN32 Device Pinout

Table 5.13. EFM32TG1	1B1xx in QFN32	Device Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 28	Digital IO power supply 0.	PC0	5	GPIO (5V)
PC1	6	GPIO (5V)	PB7	7	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is re- ceived, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is re- ceived.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4

6.2 TQFP80 PCB Land Pattern



Figure 6.2. TQFP80 PCB Land Pattern Drawing