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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64gm64-a">https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64gm64-a</a>

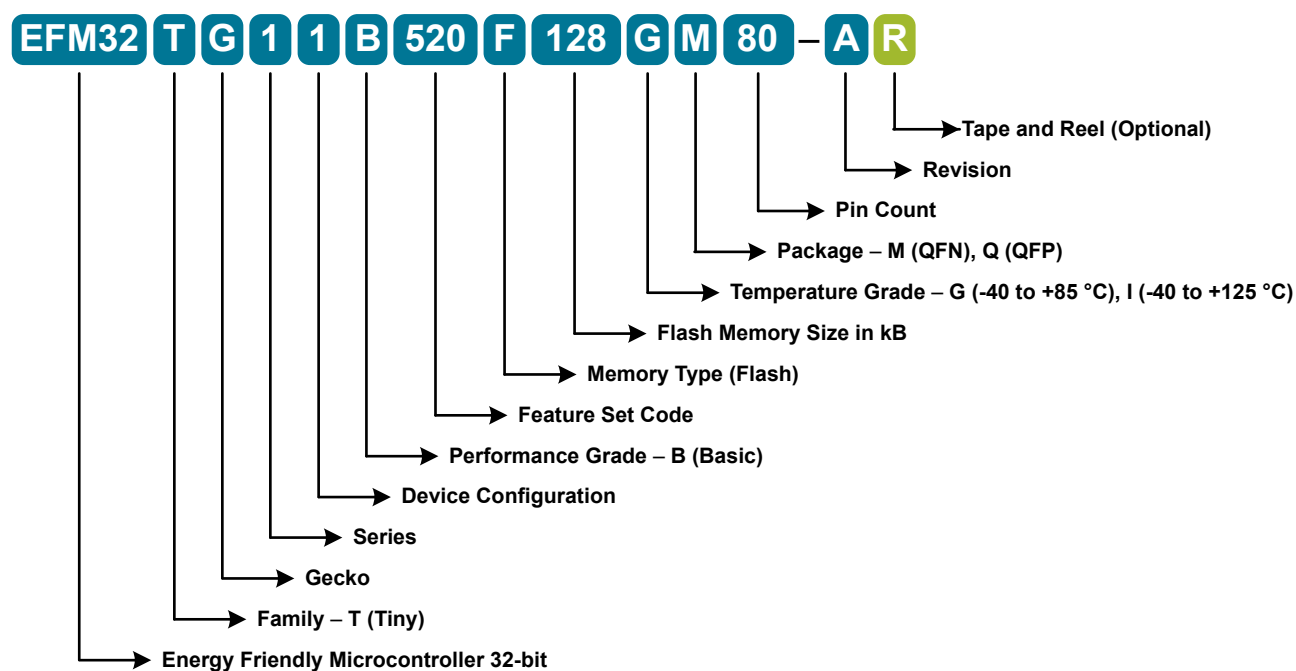


Figure 2.1. Ordering Code Key

## 3. System Overview

### 3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

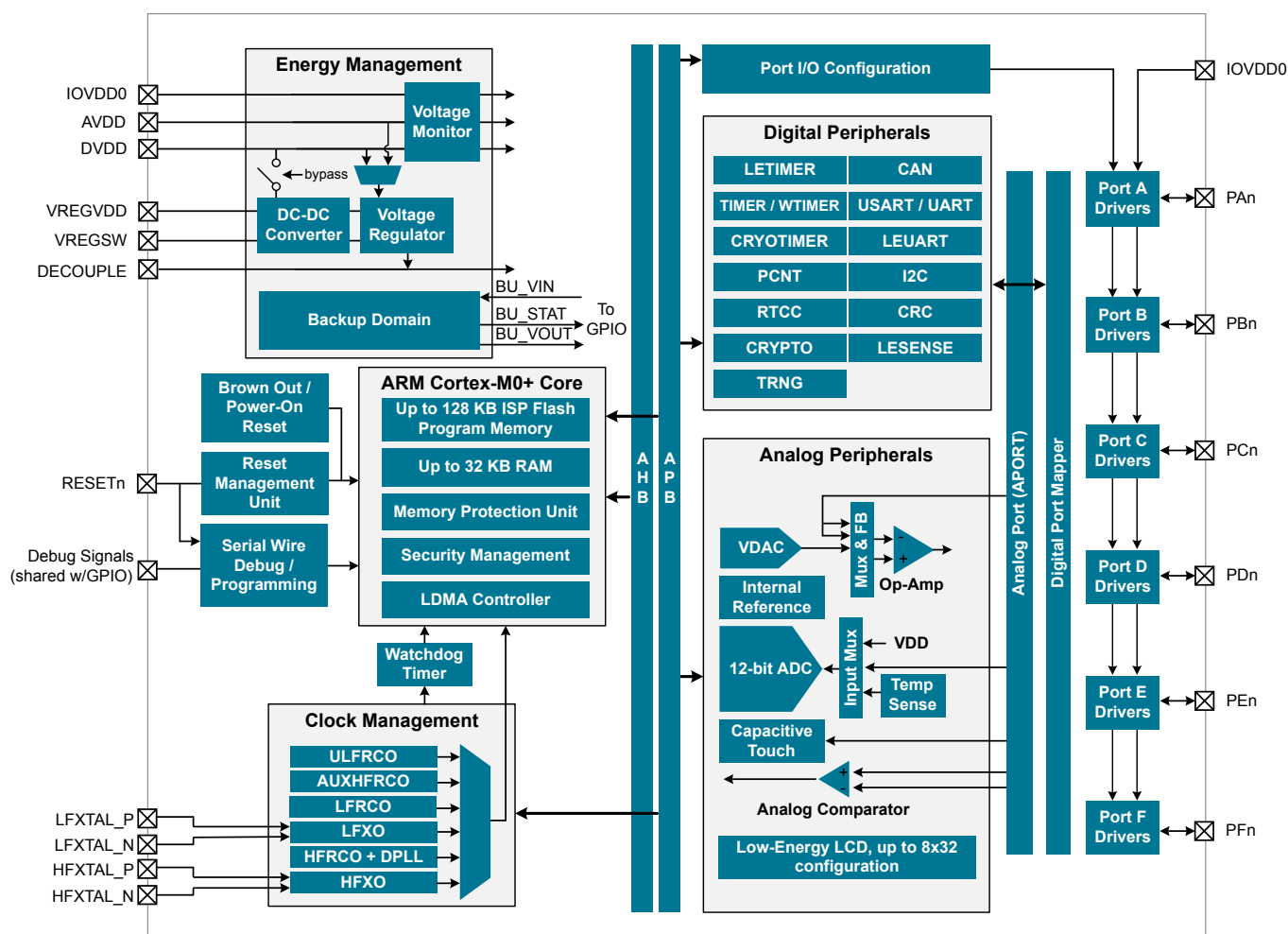


Figure 3.1. Detailed EFM32TG11 Block Diagram

### 3.6.5 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmission may be disabled in order to support Time Triggered CAN applications.

### 3.6.6 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

### 3.6.7 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

## 3.7 Security Features

### 3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Tiny Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2<sup>m</sup>), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

### 3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

### 3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

## 3.8 Analog

### 3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

### 3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

### 3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

### 3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

### 3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

## 3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

#### 4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range <sup>6</sup>	$T_A$	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage <sup>2</sup>	$V_{AVDD}$		1.8	3.3	3.8	V
VREGVDD operating supply voltage <sup>2 1</sup>	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, $T \leq 85^\circ\text{C}$	—	—	200	mA
		DCDC in bypass, $T > 85^\circ\text{C}$	—	—	100	mA
DVDD operating supply voltage	$V_{DVDD}$		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	$V_{IOVDD}$	All IOVDD pins <sup>5</sup>	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor <sup>3 4</sup>	$C_{DECOUPLE}$		0.75	1.0	2.75	μF
HFCORECLK frequency	$f_{CORE}$	VSCALE2, MODE = WS1	—	—	48	MHz
		VSCALE2, MODE = WS0	—	—	25	MHz
		VSCALE0, MODE = WS1	—	—	20	MHz
		VSCALE0, MODE = WS0	—	—	10	MHz
HFCLK frequency	$f_{HFCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz

#### 4.1.6.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

**Table 4.8. Current Consumption 1.8 V without DC-DC Converter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I <sub>ACTIVE</sub>	48 MHz crystal, CPU running while loop from flash	—	45	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	44	—	μA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	57	—	μA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	71	—	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	45	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	46	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	49	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	158	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I <sub>ACTIVE_VS</sub>	19 MHz HFRCO, CPU running while loop from flash	—	41	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	142	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I <sub>EM1</sub>	48 MHz crystal	—	34	—	μA/MHz
		48 MHz HFRCO	—	33	—	μA/MHz
		32 MHz HFRCO	—	34	—	μA/MHz
		26 MHz HFRCO	—	35	—	μA/MHz
		16 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	147	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I <sub>EM1_VS</sub>	19 MHz HFRCO	—	32	—	μA/MHz
		1 MHz HFRCO	—	133	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I <sub>EM2_VS</sub>	Full 32 kB RAM retention and RTCC running from LFXO	—	1.39	—	μA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.63	—	μA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO <sup>2</sup>	—	1.37	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I <sub>EM3_VS</sub>	Full 32 kB RAM retention and CRYOTIMER running from ULFR-CO	—	1.10	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I <sub>EM4H_VS</sub>	128 byte RAM retention, RTCC running from LFXO	—	0.75	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.37	—	μA
		128 byte RAM retention, no RTCC	—	0.37	—	μA
Current consumption in EM4S mode	I <sub>EM4S</sub>	No RAM retention, no RTCC	—	0.05	—	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I <sub>PD1_VS</sub>	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled <sup>1</sup>	—	0.18	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I <sub>PD2_VS</sub>	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled <sup>1</sup>	—	0.18	—	μA

**Note:**

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.3 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.
2. CMU\_LFRCOCTRL\_ENVREF = 1, CMU\_LFRCOCTRL\_VREFUPDATE = 1



Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V <sub>IO</sub>	t <sub>IOOF</sub>	C <sub>L</sub> = 50 pF, DRIVESTRENGTH <sup>1</sup> = STRONG, SLEWRATE <sup>1</sup> = 0x6	—	1.8	—	ns
		C <sub>L</sub> = 50 pF, DRIVESTRENGTH <sup>1</sup> = WEAK, SLEWRATE <sup>1</sup> = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V <sub>IO</sub>	t <sub>IOOR</sub>	C <sub>L</sub> = 50 pF, DRIVESTRENGTH <sup>1</sup> = STRONG, SLEWRATE = 0x6 <sup>1</sup>	—	2.2	—	ns
		C <sub>L</sub> = 50 pF, DRIVESTRENGTH <sup>1</sup> = WEAK, SLEWRATE <sup>1</sup> = 0x6	—	7.4	—	ns
<b>Note:</b> 1. In GPIO_Pn_CTRL register.						

#### 4.1.12 Voltage Monitor (VMON)

**Table 4.19. Voltage Monitor (VMON)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I <sub>SENSE</sub> )	I <sub>VMON</sub>	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.3	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	12.5	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I <sub>SENSE</sub>	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V <sub>VMON_RANGE</sub>		1.62	—	3.4	V
Threshold step size	N <sub>VMON_STESP</sub>	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t <sub>VMON_RES</sub>	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V <sub>VMON_HYST</sub>		—	26	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	$f_{\text{ADCCLK}}$		—	—	16	MHz
Throughput rate	$f_{\text{ADCRATE}}$		—	—	1	Msp/s
Conversion time <sup>1</sup>	$t_{\text{ADCCONV}}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{\text{ADCSTART}}$	WARMUPMODE <sup>4</sup> = NORMAL	—	—	5	μs
		WARMUPMODE <sup>4</sup> = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE <sup>4</sup> = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$	$\text{SNDR}_{\text{ADC}}$	Internal reference <sup>7</sup> , differential measurement	TBD	67	—	dB
		External reference <sup>6</sup> , differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$\text{SFDR}_{\text{ADC}}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	$\text{DNL}_{\text{ADC}}$	12 bit resolution, No missing codes	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	$\text{INL}_{\text{ADC}}$	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{\text{ADCOFFSETERR}}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{\text{ADCGAIN}}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	$V_{\text{TS\_SLOPE}}$		—	-1.84	—	mV/°C

**Note:**

- Derived from ADCCLK.
- PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU\_PWRCTRL.
- In ADCn\_BIASPROG register.
- In ADCn\_CNTL register.
- The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU\_PWRCTRL\_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
- External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL\_REF or SCANCTRL\_REF register field and VREFP in the SINGLECTRLX\_VREFSEL or SCANCTRLX\_VREFSEL field. The differential input range with this configuration is  $\pm 1.25\text{ V}$ .
- Internal reference option used corresponds to selection 2V5 in the SINGLECTRL\_REF or SCANCTRL\_REF register field. The differential input range with this configuration is  $\pm 1.25\text{ V}$ . Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

## 4.1.21 I2C

### 4.1.21.1 I2C Standard-mode (Sm)<sup>1</sup>

**Table 4.28. I2C Standard-mode (Sm)<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	100	kHz
SCL clock low time	t <sub>LOW</sub>		4.7	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		4	—	—	μs
SDA set-up time	t <sub>SU_DAT</sub>		250	—	—	ns
SDA hold time <sup>3</sup>	t <sub>HD_DAT</sub>		100	—	3450	ns
Repeated START condition set-up time	t <sub>SU_STA</sub>		4.7	—	—	μs
(Repeated) START condition hold time	t <sub>HD_STA</sub>		4	—	—	μs
STOP condition set-up time	t <sub>SU_STO</sub>		4	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		4.7	—	—	μs

**Note:**

1. For CLHR set to 0 in the I2Cn\_CTRL register.
2. For the minimum HPPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t<sub>HD\_DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>).

### 4.1.21.3 I2C Fast-mode Plus (Fm+)<sup>1</sup>

**Table 4.30. I2C Fast-mode Plus (Fm+)<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	1000	kHz
SCL clock low time	t <sub>LOW</sub>		0.5	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		0.26	—	—	μs
SDA set-up time	t <sub>SU_DAT</sub>		50	—	—	ns
SDA hold time	t <sub>HD_DAT</sub>		100	—	—	ns
Repeated START condition set-up time	t <sub>SU_STA</sub>		0.26	—	—	μs
(Repeated) START condition hold time	t <sub>HD_STA</sub>		0.26	—	—	μs
STOP condition set-up time	t <sub>SU_STO</sub>		0.26	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		0.5	—	—	μs

**Note:**

1. For CLHR set to 0 or 1 in the I2Cn\_CTRL register.
2. For the minimum HPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

## 4.2.1 Supply Current

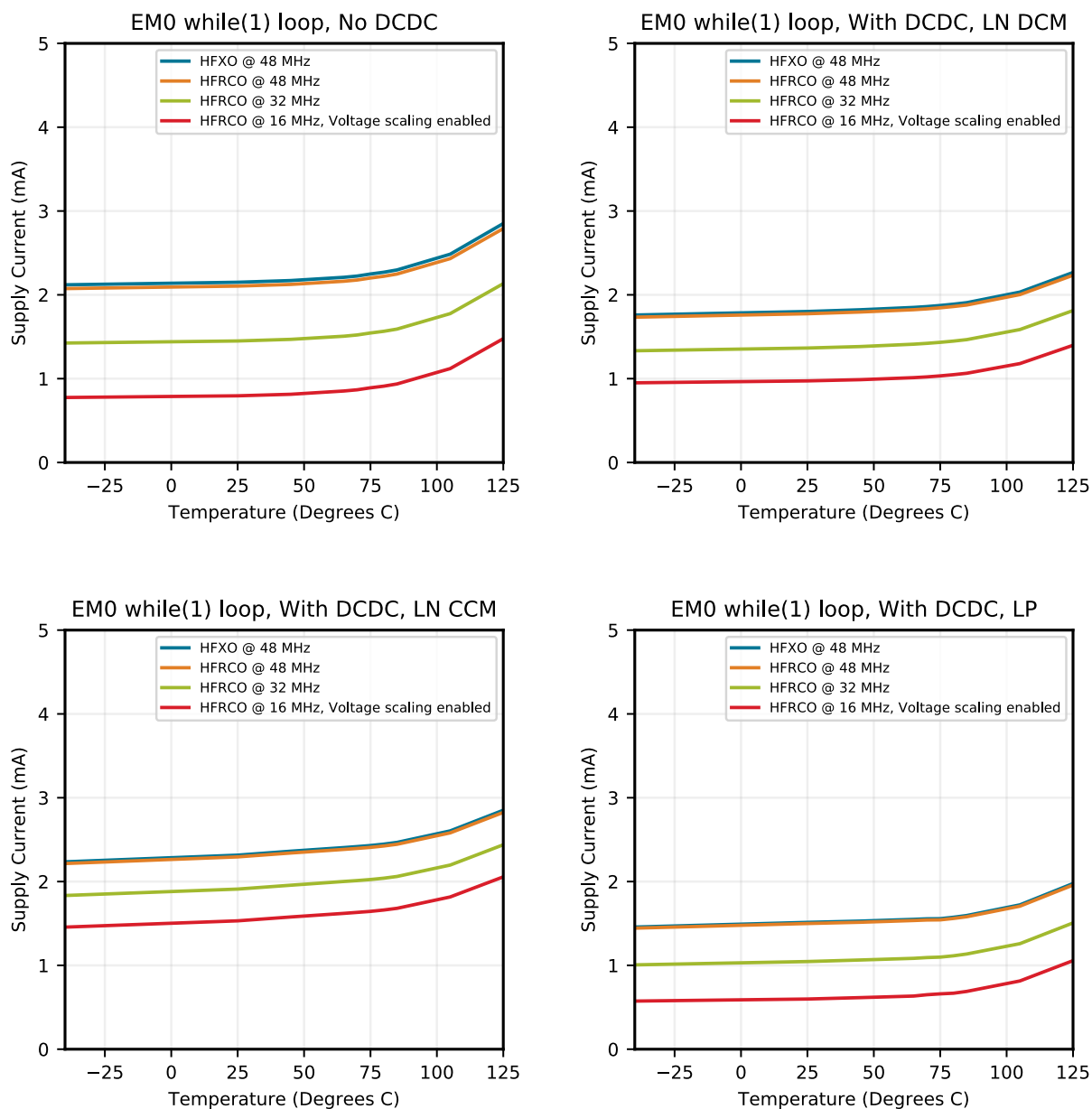
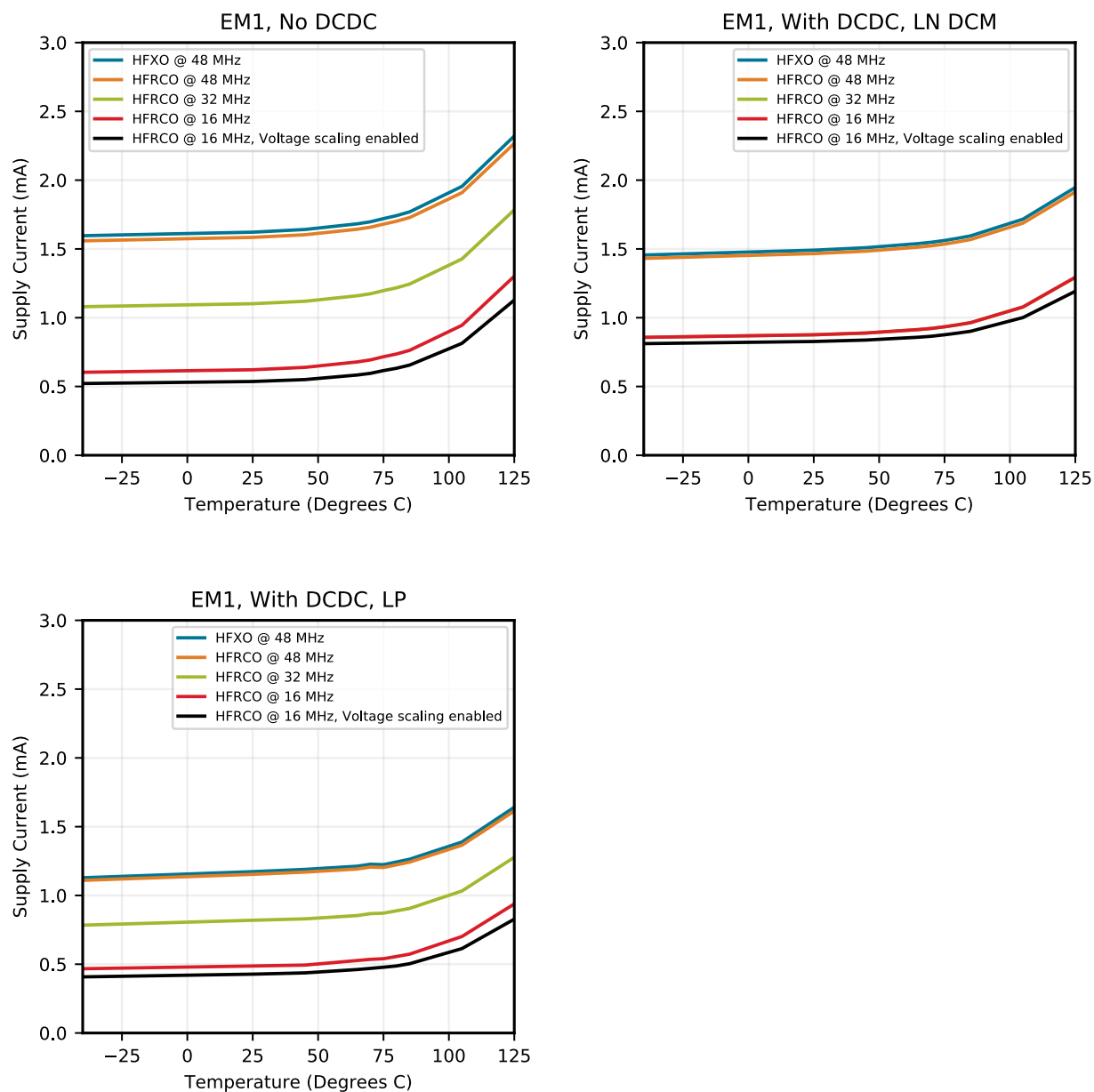


Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature



**Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature**

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	79	GPIO	PA15	80	GPIO

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).



GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PD5	BUSADC0Y BUSADC0X OPA2_OUT	WTIM0_CDT11 #4 WTIM1_CC3 #1	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT OPA1_P	TIM1_CC0 #4 WTIM0_CDT12 #4 WTIM1_CC0 #2 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_AL- TEX0 PRS_CH5 #2 ACMP0_O #2
PD7	BUSADC0Y BUSADC0X ADC0_EXTN OPA1_N	TIM1_CC1 #4 WTIM1_CC1 #2 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_AL- TEX1 ACMP1_O #2
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1
PC6	BUSACMP0Y BU- SACMP0X OPA3_P LCD_SEG32	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 I2C0_SDA #2	LES_CH6
PC7	BUSACMP0Y BU- SACMP0X OPA3_N LCD_SEG33	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 I2C0_SCL #2	LES_CH7
PE4	BUSDY BUSCX LCD_COM0	WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 I2C0_SDA #7	
PE5	BUSCY BUSDX LCD_COM1	WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 I2C0_SCL #7	
PE6	BUSDY BUSCX LCD_COM2	WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2
PE7	BUSCY BUSDX LCD_COM3	WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2
PC8	BUSACMP1Y BU- SACMP1X LCD_SEG34		US0_CS #2	LES_CH8 PRS_CH4 #0
PC9	BUSACMP1Y BU- SACMP1X LCD_SEG35		US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC10	BUSACMP1Y BU- SACMP1X		US0_RX #2	LES_CH10
PC11	BUSACMP1Y BU- SACMP1X		US0_TX #2 I2C1_SDA #4	LES_CH11
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BU- SACMP1Y BUSACMP1X	TIM1_CC3 #0	US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3	CMU_CLK0 #1 LES_CH12
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BU- SACMP1Y BUSACMP1X	TIM0_CDT10 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3	LES_CH13
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BU- SACMP1Y BUSACMP1X	TIM0_CDT11 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 LEU0_TX #5	LES_CH14 PRS_CH0 #2

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PE10		Pin can be used to wake the system up from EM4
HFX TAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1 1: PD7 2: PC7	4: PC1 5: PF1 6: PE13 7: PE5	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PD6 2: PC6	4: PC0 5: PF0 6: PE12 7: PE4	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12  3: PD5	4: PF2	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11  3: PD4	4: PC11	I2C1 Serial Data input / output.
LCD_BEXT	0: PA14		<p>LCD external supply bypass in step down or charge pump mode. If using the LCD in step-down or charge pump mode, a 1 uF (minimum) capacitor between this pin and VSS is required.</p> <p>To reduce supply ripple, a larger capcitor of approximately 1000 times the total LCD segment capacitance may be used.</p> <p>If using the LCD with the internal supply source, this pin may be left unconnected or used as a GPIO.</p>

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8	Low Energy Timer LETIM0, output channel 0.



### 9.3 QFN64 Package Marking



Figure 9.3. QFN64 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.