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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64gq48-a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

### 3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

### 3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

#### 3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	12C0
APORT	I2C1
-	IDAC
-	LCD

#### Table 3.1. EM2 and EM3 Peripheral Power Subdomains

### 3.10 Core and Memory

### 3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M0+ RISC processor
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Micro-Trace Buffer (MTB)
- Up to 128 kB flash program memory
- · Up to 32 kB RAM data memory
- · Configuration and event handling of all modules
- · 2-pin Serial-Wire debug interface

### 3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

### 3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling so-phisticated operations to be implemented.

#### 3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

### 4.1.9.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frequency accuracy	f <sub>AUXHFRCO_ACC</sub>	At production calibrated frequen- cies, across supply voltage and temperature	TBD	_	TBD	%
Start-up time	t <sub>AUXHFRCO</sub>	f <sub>AUXHFRCO</sub> ≥ 19 MHz	_	400	_	ns
		4 < f <sub>AUXHFRCO</sub> < 19 MHz	_	1.4	_	μs
		f <sub>AUXHFRCO</sub> ≤ 4 MHz	_	2.5		μs
Current consumption on all	IAUXHFRCO	f <sub>AUXHFRCO</sub> = 48 MHz	_	238	TBD	μA
supplies		f <sub>AUXHFRCO</sub> = 38 MHz	—	196	TBD	μA
		f <sub>AUXHFRCO</sub> = 32 MHz		160	TBD	μA
		f <sub>AUXHFRCO</sub> = 26 MHz	_	137	TBD	μA
		f <sub>AUXHFRCO</sub> = 19 MHz	—	110	TBD	μA
		f <sub>AUXHFRCO</sub> = 16 MHz	_	101	TBD	μA
		f <sub>AUXHFRCO</sub> = 13 MHz	_	78	TBD	μA
		f <sub>AUXHFRCO</sub> = 7 MHz	—	54	TBD	μA
		f <sub>AUXHFRCO</sub> = 4 MHz	_	30	TBD	μA
		f <sub>AUXHFRCO</sub> = 2 MHz	_	27	TBD	μA
		f <sub>AUXHFRCO</sub> = 1 MHz	_	25	TBD	μA
Coarse trim step size (% of period)	SS <sub>AUXHFR-</sub> CO_COARSE		_	0.8	_	%
Fine trim step size (% of pe- riod)	SS <sub>AUXHFR-</sub> CO_FINE		—	0.1	_	%
Period jitter	PJ <sub>AUXHFRCO</sub>		—	0.2	—	% RMS

## Table 4.15. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

# 4.1.9.6 Ultra-low Frequency RC Oscillator (ULFRCO)

### Table 4.16. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Oscillation frequency	f <sub>ULFRCO</sub>		TBD	1	TBD	kHz

# 4.1.14 Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V <sub>ACMPIN</sub>	ACMPVDD = ACMPn_CTRL_PWRSEL <sup>1</sup>	—	—	V <sub>ACMPVDD</sub>	V
Supply voltage	VACMPVDD	$BIASPROG^4 \le 0x10 \text{ or } FULL-BIAS^4 = 0$	1.8	—	V <sub>VREGVDD</sub> MAX	V
		$0x10 < BIASPROG^4 \le 0x20$ and FULLBIAS <sup>4</sup> = 1	2.1	_	V <sub>VREGVDD</sub> MAX	V
Active current not including voltage reference <sup>2</sup>	I <sub>ACMP</sub>	$BIASPROG^4 = 1$ , $FULLBIAS^4 = 0$	—	50	_	nA
		$BIASPROG^4 = 0x10, FULLBIAS^4 = 0$		306	_	nA
		$BIASPROG^4 = 0x02, FULLBIAS^4$ $= 1$	_	6.5	_	μA
		BIASPROG <sup>4</sup> = 0x20, FULLBIAS <sup>4</sup> = 1	_	74	TBD	μA
Current consumption of inter- nal voltage reference <sup>2</sup>	IACMPREF	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	_	50	_	nA
		VLP selected as input using VDD	—	20	_	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	_	μA
		VADIV selected as input using VDD/1		2.4	_	μA

# Table 4.21. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Note: 1. ACMPVDD is a supply ch 2. The total ACMP current is I <sub>ACMPREF</sub> . 3. ± 100 mV differential drive 4. In ACMPn_CTRL register 5. In ACMPn_HYSTERESIS 6. In ACMPn_INPUTSEL reg	osen by the s the sum of the e. Fregisters. gister.	etting in ACMPn_CTRL_PWRS ne contributions from the ACMP	EL and may be IOVDE and its internal voltage	), AVDD or D\ e reference. I₄	VDD. CMPTOTAL = I	ACMP +

## 4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.22.	Digital to	Analog Converter	(VDAC)
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Output voltage	V <sub>DACOUT</sub>	Single-Ended	0	_	V <sub>VREF</sub>	V
		Differential <sup>2</sup>	-V <sub>VREF</sub>	—	V <sub>VREF</sub>	V
Current consumption includ- ing references (2 channels) <sup>1</sup>	I <sub>DAC</sub>	500 ksps, 12-bit, DRIVES- TRENGTH = 2, REFSEL = 4	_	396	_	μΑ
		44.1 ksps, 12-bit, DRIVES- TRENGTH = 1, REFSEL = 4	—	72	—	μA
		200 Hz refresh rate, 12-bit Sam- ple-Off mode in EM2, DRIVES- TRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WAR- MUPTIME = 0x02	_	2	_	μA
Current from HFPERCLK <sup>4</sup>	IDAC_CLK		_	5.8		µA/MHz
Sample rate	SR <sub>DAC</sub>		—	—	500	ksps
DAC clock frequency	f <sub>DAC</sub>		—	—	1	MHz
Conversion time	t <sub>DACCONV</sub>	f <sub>DAC</sub> = 1MHz	2	_		μs
Settling time	t <sub>DACSETTLE</sub>	50% fs step settling to 5 LSB		2.5		μs
Startup time	t <sub>DACSTARTUP</sub>	Enable to 90% fs output, settling to 10 LSB	—	—	12	μs
Output impedance	R <sub>OUT</sub>	$\label{eq:output} \begin{array}{l} DRIVESTRENGTH = 2,\ 0.4\ V \leq \\ V_{OUT} \leq V_{OPA} - 0.4\ V, -8\ mA < \\ I_{OUT} < 8\ mA, \ Full \ supply \ range \end{array}$	_	2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V $\leq V_{OUT} \leq V_{OPA} - 0.4 V$ , -400 µA < $I_{OUT} < 400$ µA, Full supply range	_	2	_	Ω
		$\begin{array}{l} DRIVESTRENGTH = 2, \ 0.1 \ V \leq \\ V_{OUT} \leq V_{OPA} \ \text{-} \ 0.1 \ V, \ \text{-} 2 \ mA < \\ I_{OUT} < 2 \ mA, \ Full \ supply \ range \end{array}$		2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$ , -100 µA < $I_{OUT} < 100$ µA, Full supply range	_	2	_	Ω
Power supply rejection ratio <sup>6</sup>	PSRR	Vout = 50% fs. DC		65.5	_	dB

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Note:						
1. Specified configuration fo V. Nominal voltage gain is	r 3X-Gain configu s 3.	uration is: INCBW = 1, HCMDIS = 1, I	RESINSEL = '	/SS, V <sub>INPUT</sub> =	= 0.5 V, V <sub>OUT</sub>	<sub>PUT</sub> = 1.5
2. If the maximum C <sub>LOAD</sub> is	exceeded, an iso	lation resistor is required for stability.	See AN0038	for more infor	mation.	
3. When INCBW is set to 1 or the OPAMP may not b	the OPAMP band e stable.	width is increased. This is allowed or	nly when the n	on-inverting c	lose-loop gai	n is ≥ 3,
4. Current into the load resist drive the resistor feedbac another ~10 μA current w	stor is excluded. V k network. The in hen the OPAMP	When the OPAMP is connected with on ternal resistor feedback network has drives 1.5 V between output and grout drives 1.5 V between	closed-loop ga total resistand und.	ain > 1, there v ce of 143.5 kC	will be extra c )hm, which wi	urrent to ill cause
5. Step between 0.2V and V	/ <sub>OPA</sub> -0.2V, 10%-9	0% rising/falling range.				
6. From enable to output se	ttled. In sample-a	nd-off mode, RC network after OPAN	IP will contrib	ute extra dela	y. Settling err	or < 1mV.
7. In unit gain connection, U product of the OPAMP ar	IGF is the gain-band 1/3 attenuation	andwidth product of the OPAMP. In 32 of the feedback network.	x Gain conneo	tion, UGF is t	he gain-band	width
8. Specified configuration fo V <sub>OUTPUT</sub> = 0.5 V.	r Unit gain buffer	configuration is: INCBW = 0, HCMDI	S = 0, RESIN	SEL = DISAB	LE. V <sub>INPUT</sub> =	0.5 V,
9. When HCMDIS=1 and inp and CMRR specifications	put common mode do not apply to th	e transitions the region from V <sub>OPA</sub> -1.4 his transition region.	4V to V <sub>OPA</sub> -1\	/, input offset	will change. F	PSRR
4.1.18 LCD Driver						

### Table 4.25. LCD Driver

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Frame rate	f <sub>LCDFR</sub>		TBD	_	TBD	Hz
LCD supply range <sup>2</sup>	V <sub>LCDIN</sub>		1.8		3.8	V
LCD output voltage range	V <sub>LCD</sub>	Current source mode, No external LCD capacitor	2.0		V <sub>LCDIN</sub> -0.4	V
		Step-down mode with external LCD capacitor	2.0		V <sub>LCDIN</sub>	V
		Charge pump mode with external LCD capacitor	2.0	_	Min of 3.8 and 1.9 * V <sub>LCDIN</sub>	V
Contrast control step size	STEP <sub>CONTRAST</sub>	Current source mode	_	64	—	mV
		Charge pump or Step-down mode	_	43	—	mV
Contrast control step accura- cy <sup>1</sup>	ACC <sub>CONTRAST</sub>		_	+/-4	_	%

## Note:

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

2.  $V_{LCDIN}$  is selectable between the AVDD or DVDD supply pins, depending on EMU\_PWRCTRL\_ANASW.

### 4.1.19 Pulse Counter (PCNT)

### Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input frequency	F <sub>IN</sub>	Asynchronous Single and Quad- rature Modes	_	_	20	MHz
		Sampled Modes with Debounce filter set to 0.	_	_	8	kHz

### 4.1.20 Analog Port (APORT)

### Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current <sup>2 1</sup>	I <sub>APORT</sub>	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	_	915	_	nA

#### Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.



Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	9 24 51 70	Ground	PB3	10	GPIO
PB4	11	GPIO	PB5	12	GPIO
PB6	13	GPIO	PC1	14	GPIO (5V)
PC2	15	GPIO (5V)	PC3	16	GPIO (5V)
PC4	17	GPIO	PC5	18	GPIO
PB7	19	GPIO	PB8	20	GPIO
PA8	21	GPIO	PA9	22	GPIO
PA10	23	GPIO	PA12	25	GPIO
PA14	26	GPIO	RESETn	27	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	28	GPIO	PB12	29	GPIO
AVDD	30 34	Analog power supply.	PB13	31	GPIO
PB14	32	GPIO	PD0	35	GPIO (5V)
PD1	36	GPIO	PD3	37	GPIO
PD4	38	GPIO	PD5	39	GPIO
PD6	40	GPIO	PD7	41	GPIO
PD8	42	GPIO	PC6	43	GPIO
PC7	44	GPIO	VREGVSS	45	Voltage regulator VSS
VREGSW	46	DCDC regulator switching node	VREGVDD	47	Voltage regulator VDD input
DVDD	48	Digital power supply.	DECOUPLE	49	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	52	GPIO	PE5	53	GPIO
PE6	54	GPIO	PE7	55	GPIO
PC8	56	GPIO	PC9	57	GPIO
PC10	58	GPIO (5V)	PC11	59	GPIO (5V)
PC13	60	GPIO (5V)	PC14	61	GPIO (5V)
PC15	62	GPIO (5V)	PF0	63	GPIO (5V)
PF1	64	GPIO (5V)	PF2	65	GPIO
PF3	66	GPIO	PF4	67	GPIO
PF5	68	GPIO	PE8	71	GPIO
PE9	72	GPIO	PE10	73	GPIO
PE11	74	GPIO	BODEN	75	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.

	1 11(3)	Description
PE13	77	GPIO
PE15	79	GPIO
	PE13 PE15	PE13 77   PE15 79

Note:

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB7	11	GPIO	PB8	12	GPIO
PA12	13	GPIO	PA13	14	GPIO (5V)
PA14	15	GPIO	RESETn	16	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	17	GPIO	AVDD	19 23	Analog power supply.
PB13	20	GPIO	PB14	21	GPIO
PD4	24	GPIO	PD5	25	GPIO
PD6	26	GPIO	PD7	27	GPIO
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	30	GPIO	PE5	31	GPIO
PE6	32	GPIO	PE7	33	GPIO
PC13	34	GPIO (5V)	PC14	35	GPIO (5V)
PC15	36	GPIO (5V)	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			
Note:	1		_	1	

GPIO Name		ionality / Description						
	Analog	Timers	Communication	Other				
PC4	BUSACMP0Y BU- SACMP0X OPA0_P LCD_SEG24	TIM0_CC0 #5 TIM0_CDTI2 #3 LE- TIM0_OUT0 #3	US2_CLK #0 U0_TX #4 I2C1_SDA #0	LES_CH4 GPIO_EM4WU6				
PC5	BUSACMP0Y BU- SACMP0X OPA0_N LCD_SEG25	TIM0_CC1 #5 LE- TIM0_OUT1 #3	US2_CS #0 U0_RX #4 I2C1_SCL #0	LES_CH5				
PB7	LFXTAL_P	TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 U0_CTS #4					
PB8	LFXTAL_N	TIM0_CDTI1 #4 TIM1_CC1 #3	US0_RX #4 US1_CS #0 U0_RTS #4	CMU_CLKI0 #2				
PA8	BU_STAT	TIM0_CC0 #6 LE- TIM0_OUT0 #6	US2_RX #2					
PA9	BUSAY BUSBX LCD_SEG26	TIM0_CC1 #6 LE- TIM0_OUT1 #6	US2_CLK #2					
PA10	BUSBY BUSAX LCD_SEG27	TIM0_CC2 #6	US2_CS #2					
PA12	BU_VOUT	WTIM0_CDTI0 #2	US0_CLK #5 US2_RTS #2	CMU_CLK0 #5 ACMP1_O #3				
PA13	BUSAY BUSBX	TIM0_CC2 #7 WTIM0_CDTI1 #2	US0_CS #5 US2_TX #3					
PA14	BUSBY BUSAX LCD_BEXT	WTIM0_CDTI2 #2	US1_TX #6 US2_RX #3 US3_RTS #2	ACMP1_O #4				
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT LCD_SEG28	TIM0_CDTI2 #4 TIM1_CC2 #3 LE- TIM0_OUT0 #1 PCNT0_S1IN #7	US0_CTS #5 US1_CLK #5 US2_CS #3 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLKI0 #7 ACMP0_O #3 GPIO_EM4WU7				
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT LCD_SEG29	TIM1_CC3 #3 LE- TIM0_OUT1 #1 PCNT0_S0IN #7	US2_CTS #1 I2C1_SCL #1					
PB13	BUSAY BUSBX HFXTAL_P	WTIM1_CC0 #0	US0_CLK #4 US1_CTS #5 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0				
PB14	BUSBY BUSAX HFXTAL_N	WTIM1_CC1 #0	US0_CS #4 US1_RTS #5 LEU0_RX #1	PRS_CH6 #1				
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU- SADC0Y BUSADC0X	WTIM1_CC2 #0	CAN0_RX #2 US1_TX #1					
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BU- SADC0Y BUSADC0X OPA3_OUT	TIM0_CC0 #2 WTIM1_CC3 #0	CAN0_TX #2 US1_RX #1					
PD2	BUSADC0Y BUSADC0X	TIM0_CC1 #2 WTIM1_CC0 #1	US1_CLK #1					
PD3	BUSADC0Y BUSADC0X OPA2_N LCD_SEG30	TIM0_CC2 #2 WTIM1_CC1 #1	US1_CS #1					
PD4	BUSADC0Y BUSADC0X OPA2_P LCD_SEG31	WTIM0_CDTI0 #4 WTIM1_CC2 #1	US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0				

Alternate	LOC	ATION	
Functionality	0 - 3	4 - 7	Description
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional ex- ternal clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	СНЗ	CH2	CH1	СНО
ОР	A0_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
<b>APORT3Y</b>	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
ОР	A0_	P		•						•											•										·		
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					

# Table 5.20. VDAC0 / OPA Bus and Pin Mapping

# 6. TQFP80 Package Specifications

### 6.1 TQFP80 Package Dimensions



Figure 6.1. TQFP80 Package Drawing



Figure 11.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

# 12. Revision History

### **Revision 0.5**

February, 2018

- 4.1 Electrical Characteristics updated with latest characterization data and production test limits.
- Added 4.1.3 Thermal Characteristics.
- Added 4.2 Typical Performance Curves section.
- Corrected OPA / VDAC output connections in Figure 5.14 APORT Connection Diagram on page 119.

### **Revision 0.1**

May 1st, 2017

Initial release.