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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64gq48-ar

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive[2], T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 µF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 µF. See Application Note AN0948 for details.

4.1.12 Voltage Monitor (VMON)

Table 4.19. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.3	TBD	µA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	12.5	TBD	µA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.20. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	µA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	166	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, V_{INPUT} = 0.5 V, V_{OUTPUT} = 1.5 V. Nominal voltage gain is 3.
2. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. Step between 0.2V and V_{OPA}-0.2V, 10%-90% rising/falling range.
6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. V_{INPUT} = 0.5 V, V_{OUTPUT} = 0.5 V.
9. When HCMDIS=1 and input common mode transitions the region from V_{OPA}-1.4V to V_{OPA}-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

4.1.18 LCD Driver

Table 4.25. LCD Driver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		TBD	—	TBD	Hz
LCD supply range[2]	V_{LCDIN}		1.8	—	3.8	V
LCD output voltage range	V_{LCD}	Current source mode, No external LCD capacitor	2.0	—	V_{LCDIN}-0.4	V
		Step-down mode with external LCD capacitor	2.0	—	V_{LCDIN}	V
		Charge pump mode with external LCD capacitor	2.0	—	Min of 3.8 and 1.9 * V_{LCDIN}	V
Contrast control step size	$STEP_{CONTRAST}$	Current source mode	—	64	—	mV
		Charge pump or Step-down mode	—	43	—	mV
Contrast control step accuracy[1]	$ACC_{CONTRAST}$		—	+/-4	—	%

Note:

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.
2. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.

4.1.19 Pulse Counter (PCNT)

Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

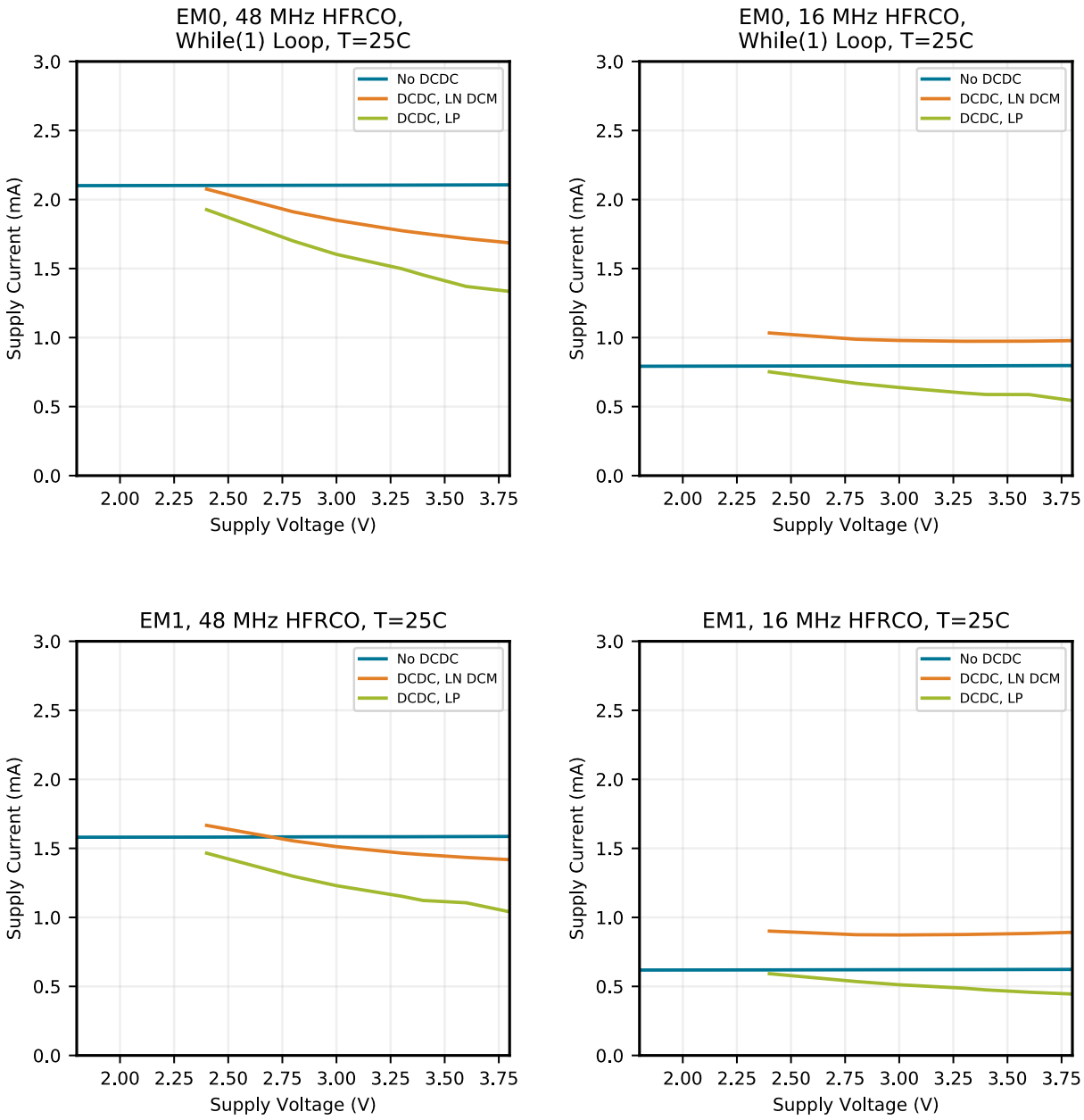

Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE12	76	GPIO	PE13	77	GPIO
PE14	78	GPIO	PE15	79	GPIO
PA15	80	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGVSS	38	Voltage regulator VSS	VREGSW	39	DCDC regulator switching node
VREGVDD	40	Voltage regulator VDD input	DVDD	41	Digital power supply.
DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	43	GPIO
PE5	44	GPIO	PE6	45	GPIO
PE7	46	GPIO	PC12	47	GPIO (5V)
PC13	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.8 EFM32TG11B1xx in QFN64 Device Pinout

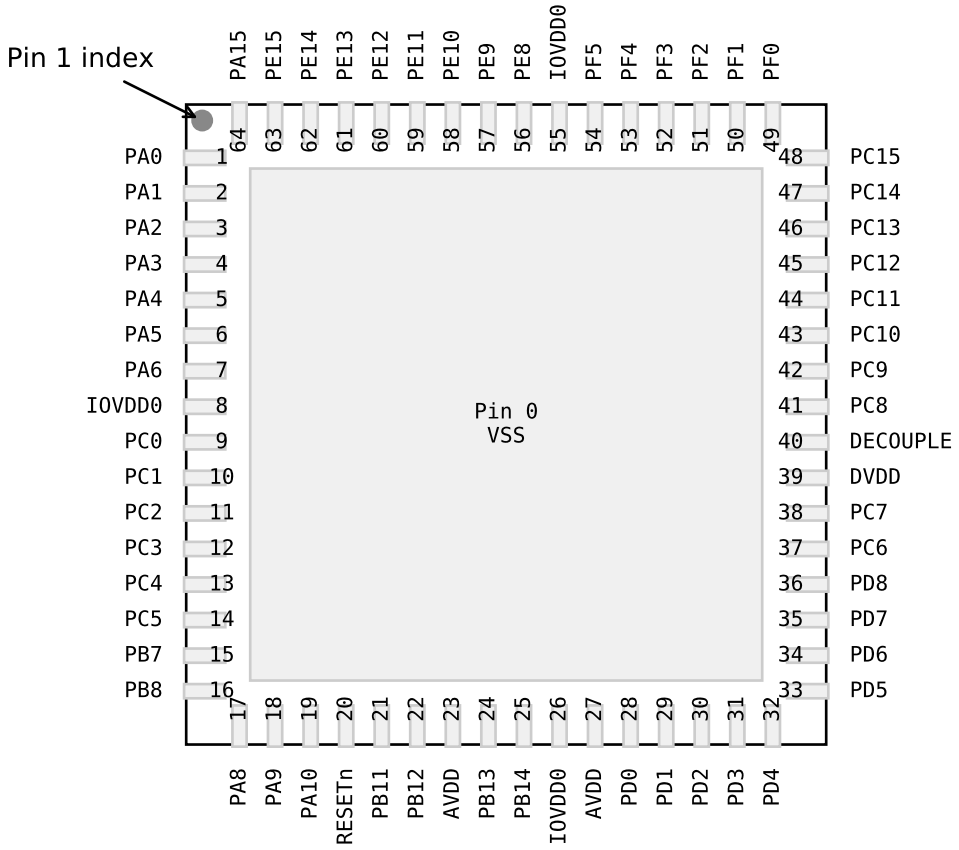

Figure 5.8. EFM32TG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.8. EFM32TG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA14	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	15	GPIO	PD5	16	GPIO
PD6	17	GPIO	PD7	18	GPIO
VREGSW	20	DCDC regulator switching node	VREGVDD	21	Voltage regulator VDD input
DVDD	22	Digital power supply.	DECOUPLE	23	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	24	GPIO	PE5	25	GPIO
PC15	26	GPIO (5V)	PF0	27	GPIO (5V)
PF1	28	GPIO (5V)	PF2	29	GPIO
PE11	31	GPIO	PE12	32	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU-SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE-TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE-TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE-TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1
PE9	BUSCY BUSDX LCD_SEG5			
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE-TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL-TEX6 PRS_CH1 #3
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE-TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2	
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2	
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG35	0: PC9		LCD segment line 35.
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.

5.16 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.14 APORT Connection Diagram on page 119 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

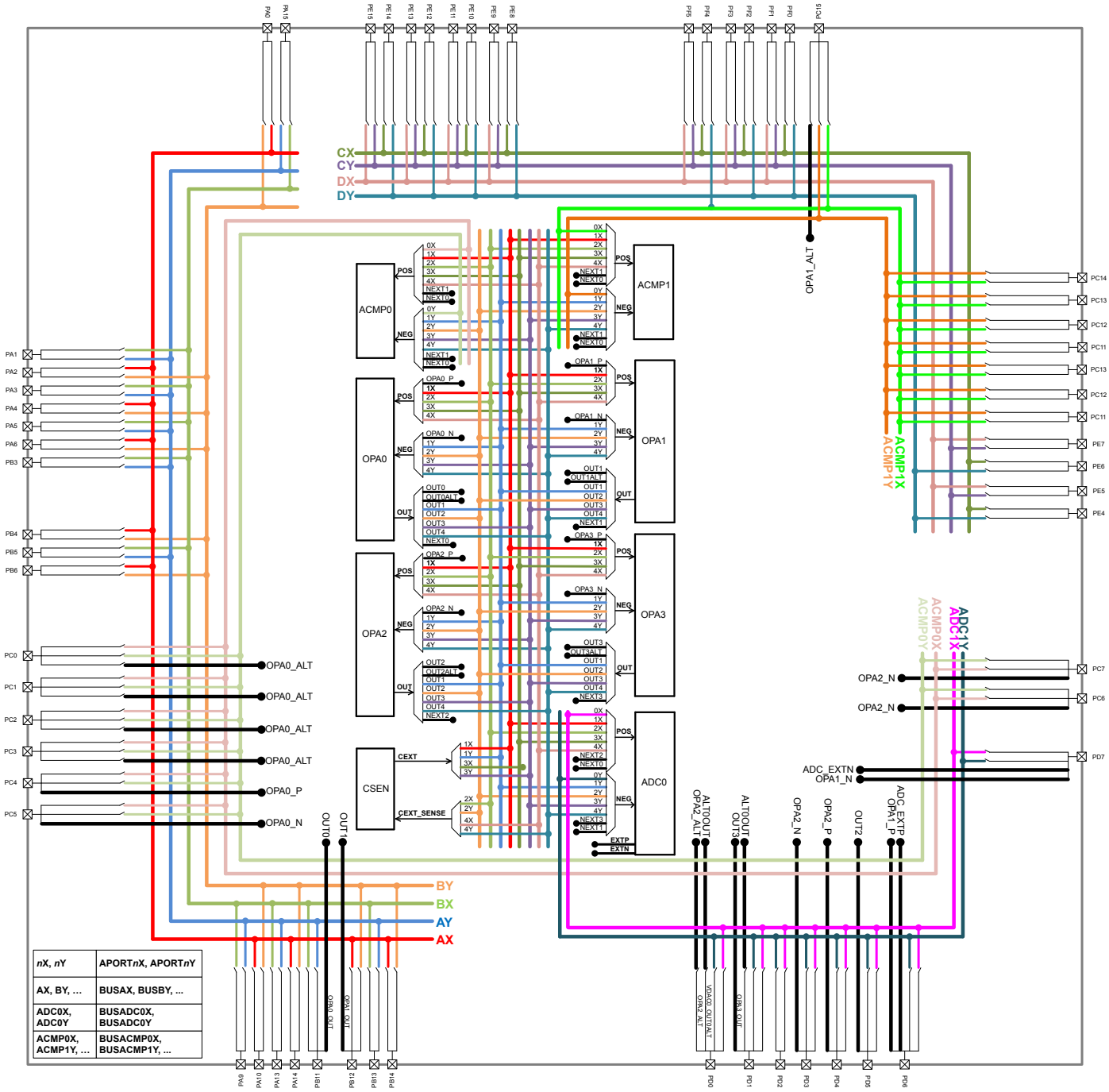

Figure 5.14. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

Table 6.2. TQFP80 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 TQFP80 Package Marking

Figure 6.3. TQFP80 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 7.1. QFN80 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions

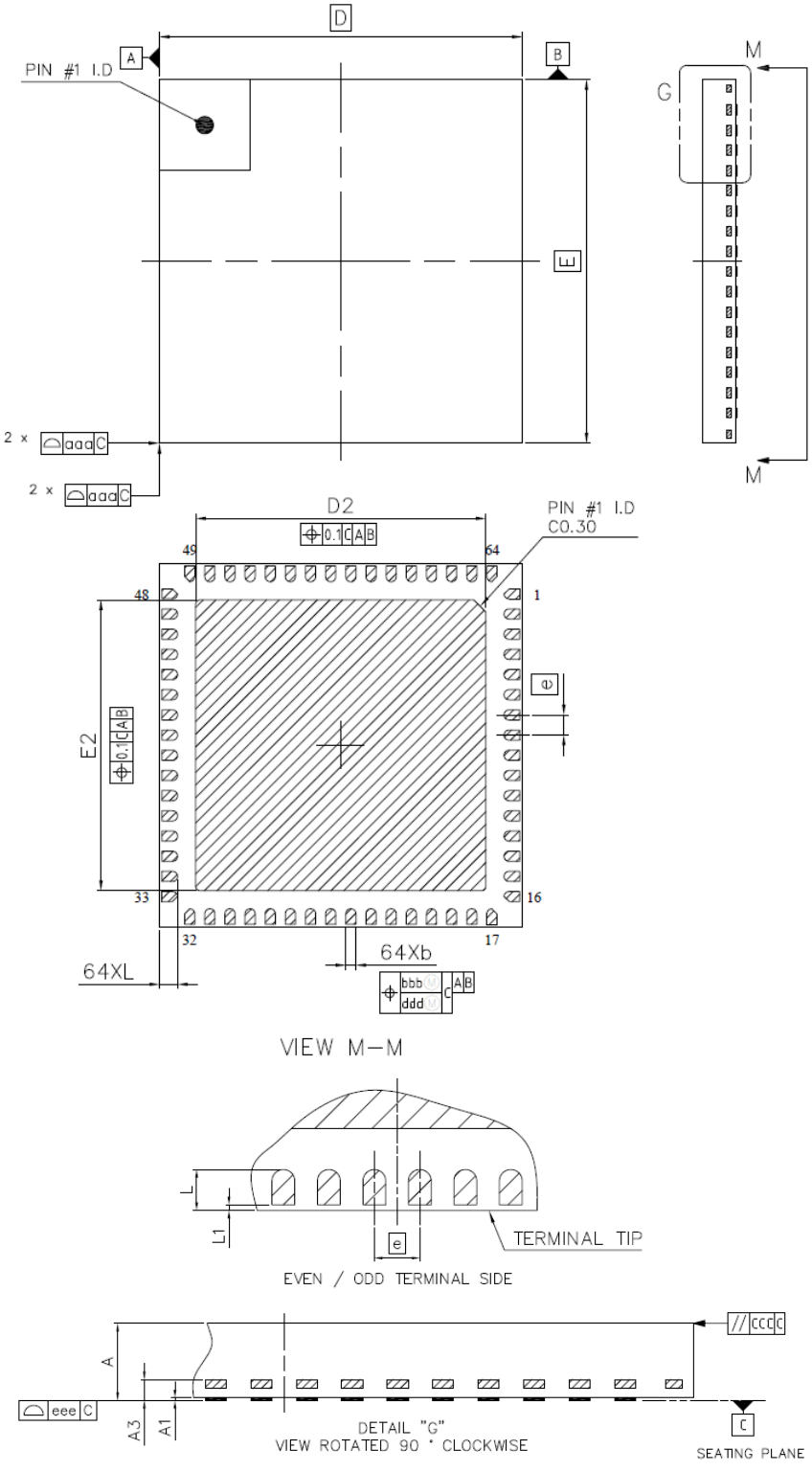

Figure 9.1. QFN64 Package Drawing

9.2 QFN64 PCB Land Pattern

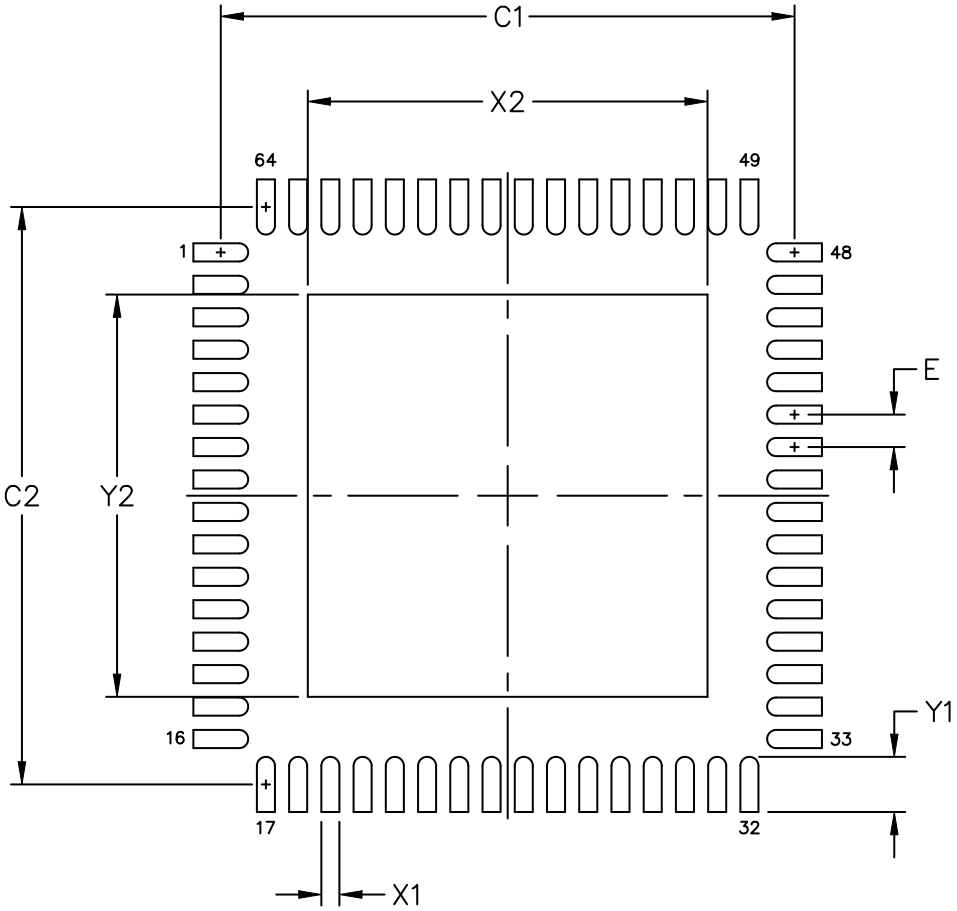

Figure 9.2. QFN64 PCB Land Pattern Drawing

10.2 TQFP48 PCB Land Pattern

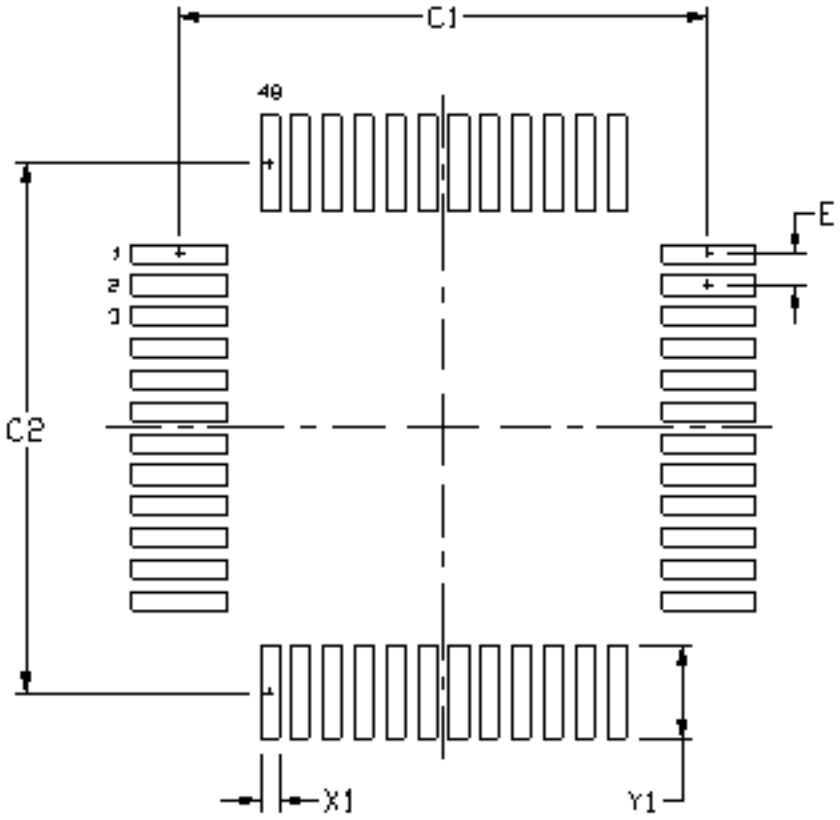

Figure 10.2. TQFP48 PCB Land Pattern Drawing

Table 10.2. TQFP48 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.50
C2	8.50
E	0.50
X	0.30
Y	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP48 Package Marking

Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.