



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64iq48-a

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128IQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

Table of Contents

1. Feature List	2
2. Ordering Information	4
3. System Overview	10
3.1 Introduction	10
3.2 Power	11
3.2.1 Energy Management Unit (EMU)	11
3.2.2 DC-DC Converter	11
3.2.3 EM2 and EM3 Power Domains	11
3.3 General Purpose Input/Output (GPIO)	12
3.4 Clocking	12
3.4.1 Clock Management Unit (CMU)	12
3.4.2 Internal and External Oscillators	12
3.5 Counters/Timers and PWM	12
3.5.1 Timer/Counter (TIMER)	12
3.5.2 Wide Timer/Counter (WTIMER)	12
3.5.3 Real Time Counter and Calendar (RTCC)	12
3.5.4 Low Energy Timer (LETIMER)	13
3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)	13
3.5.6 Pulse Counter (PCNT)	13
3.5.7 Watchdog Timer (WDOG)	13
3.6 Communications and Other Digital Peripherals	13
3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)	13
3.6.2 Universal Asynchronous Receiver/Transmitter (UART)	13
3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)	13
3.6.4 Inter-Integrated Circuit Interface (I ² C)	13
3.6.5 Controller Area Network (CAN)	14
3.6.6 Peripheral Reflex System (PRS)	14
3.6.7 Low Energy Sensor Interface (LESENSE)	14
3.7 Security Features	14
3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)	14
3.7.2 Crypto Accelerator (CRYPTO)	14
3.7.3 True Random Number Generator (TRNG)	14
3.7.4 Security Management Unit (SMU)	14
3.8 Analog	14
3.8.1 Analog Port (APORT)	15
3.8.2 Analog Comparator (ACMP)	15
3.8.3 Analog to Digital Converter (ADC)	15
3.8.4 Capacitive Sense (CSEN)	15
3.8.5 Digital to Analog Converter (VDAC)	15
3.8.6 Operational Amplifiers	15
3.8.7 Liquid Crystal Display Driver (LCD)	15
3.9 Reset Management Unit (RMU)	15

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive ² , $T \leq 85\text{ }^{\circ}\text{C}$	—	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , $T > 85\text{ }^{\circ}\text{C}$	—	—	100	mA
		Low noise (LN) mode, Medium Drive ²	—	—	100	mA
		Low noise (LN) mode, Light Drive ²	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	—	—	10	mA
DCDC nominal output capacitor ⁵	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF . Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF . See Application Note AN0948 for details.

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V _{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R _{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT ²	R _{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I _{BU_VIN}	BU_VIN not powering backup do- main	—	10	TBD	nA
		BU_VIN powering backup do- main ¹	—	450	TBD	nA

Note:
1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

4.1.6 Current Consumption

4.1.6.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	48 MHz crystal, CPU running while loop from flash	—	45	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	44	TBD	μA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	57	—	μA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	71	—	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	45	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	46	TBD	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	50	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	161	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	41	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	145	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	48 MHz crystal	—	34	—	μA/MHz
		48 MHz HFRCO	—	33	TBD	μA/MHz
		32 MHz HFRCO	—	34	—	μA/MHz
		26 MHz HFRCO	—	35	TBD	μA/MHz
		16 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	150	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	32	—	μA/MHz
		1 MHz HFRCO	—	136	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I _{EM2_VS}	Full 32 kB RAM retention and RTCC running from LFXO	—	1.48	—	μA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.86	—	μA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	1.59	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 32 kB RAM retention and CRYOTIMER running from ULFR-CO	—	1.23	TBD	μA

4.1.10 Flash Memory Characteristics⁵

Table 4.17. Flash Memory Characteristics⁵

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—	—	cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	26	32	μs
		Single word	59	68	83	μs
Page erase time ⁴	t _{PERASE}		20	27	35	ms
Mass erase time ¹	t _{MERASE}		20	27	35	ms
Device erase time ^{2 3}	t _{DERASE}	T ≤ 85 °C	—	54	70	ms
		T ≤ 125 °C	—	54	75	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.0	mA
Write current ⁶	I _{WRITE}		—	—	3.5	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.20. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	V _{RESOLUTION}		6	—	12	Bits
Input voltage range ⁵	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2	—	V _{FS} /2	V
Input range of external reference voltage, single ended and differential	V _{ADCREFIN_P}		1	—	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	—	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ⁴ = KEEPADC-WARM	I _{ADC_CONTINUOUS_LP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	270	TBD	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ³	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ³	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ⁴ = NORMAL	I _{ADC_NORMAL_LP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ³	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_LP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	70	—	μA
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ⁴ = KEEPADC-WARM	I _{ADC_CONTINUOUS_HP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ³	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ³	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ⁴ = NORMAL	I _{ADC_NORMAL_HP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ³	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_HP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	125	—	μA
Current from HFPERCLK	I _{ADC_CLK}	HFPERCLK = 16 MHz	—	166	—	μA

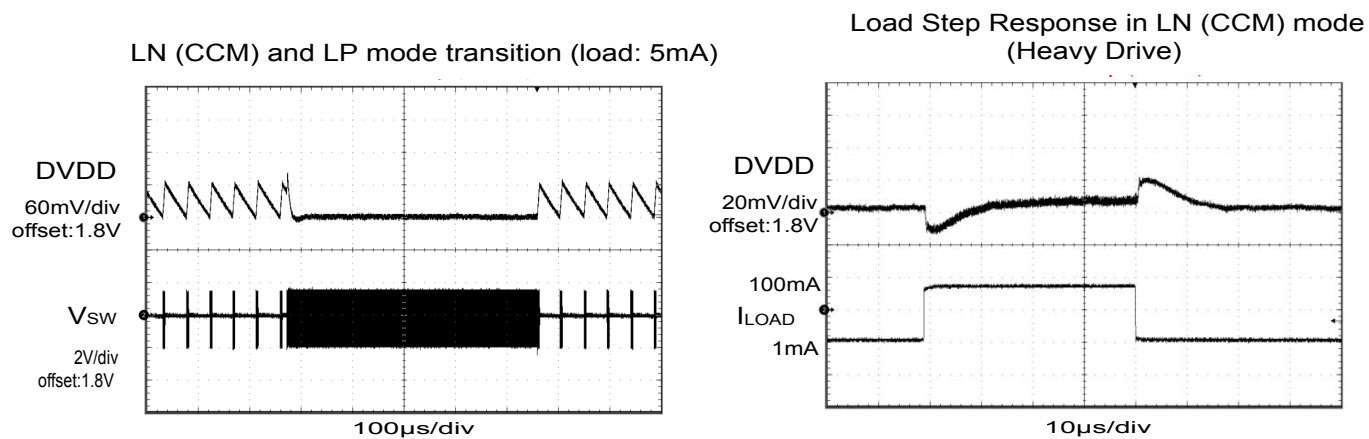


Figure 4.9. DC-DC Converter Transition Waveforms

5.2 EFM32TG11B5xx in QFN80 Device Pinout

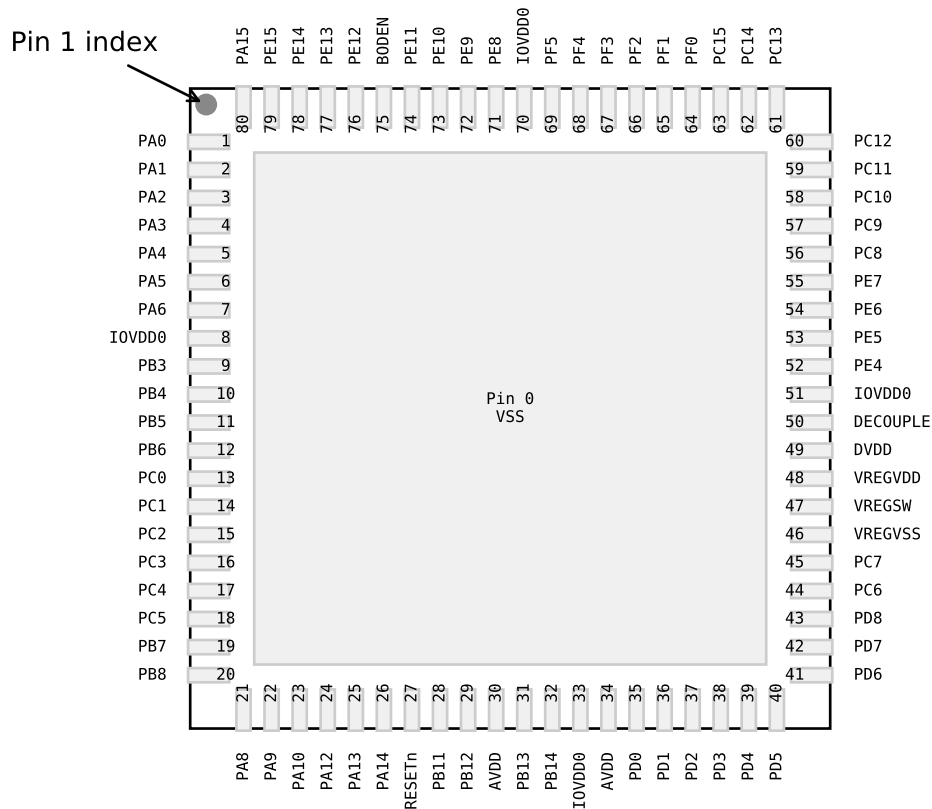


Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.2. EFM32TG11B5xx in QFN80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO

5.3 EFM32TG11B5xx in QFP64 Device Pinout

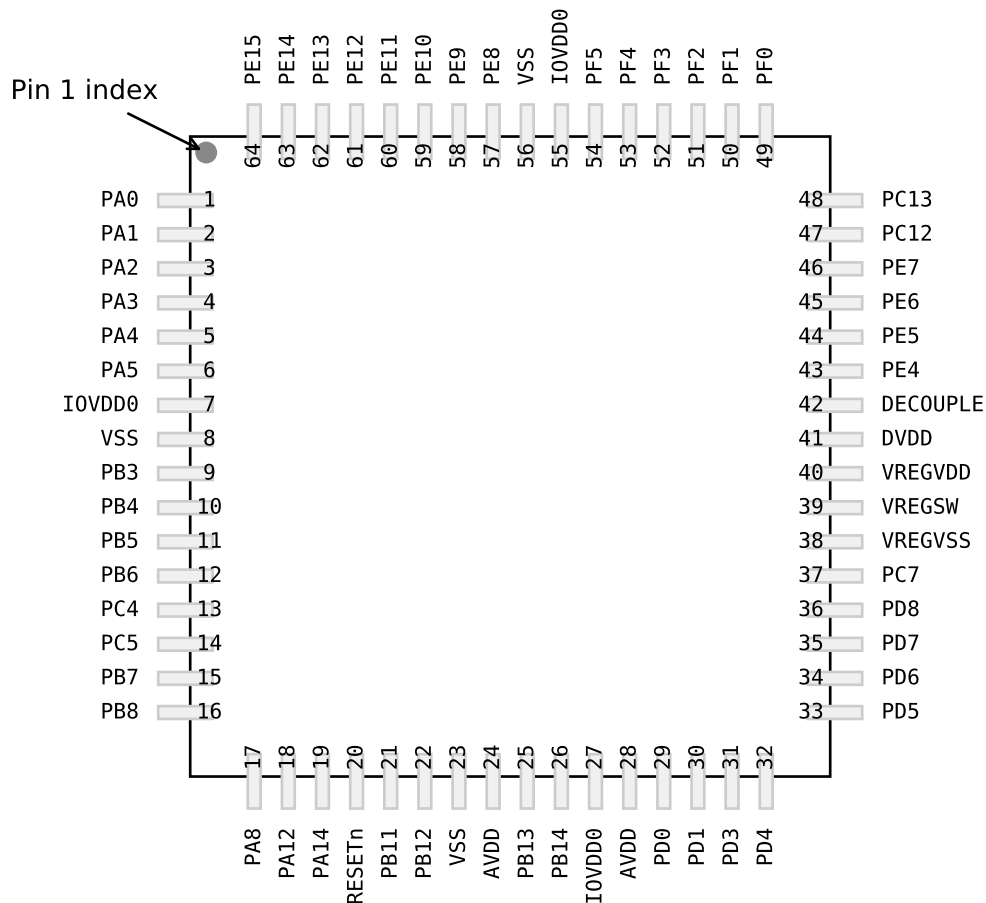


Figure 5.3. EFM32TG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.3. EFM32TG11B5xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB7	11	GPIO	PB8	12	GPIO
PA8	13	GPIO	PA9	14	GPIO
PA10	15	GPIO	RESETn	16	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	17	GPIO	AVDD	19 23	Analog power supply.
PB13	20	GPIO	PB14	21	GPIO
PD4	24	GPIO	PD5	25	GPIO
PD6	26	GPIO	PD7	27	GPIO
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC8	30	GPIO	PC9	31	GPIO
PC10	32	GPIO (5V)	PC11	33	GPIO (5V)
PC13	34	GPIO (5V)	PC14	35	GPIO (5V)
PC15	36	GPIO (5V)	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.12 EFM32TG11B5xx in QFN32 Device Pinout

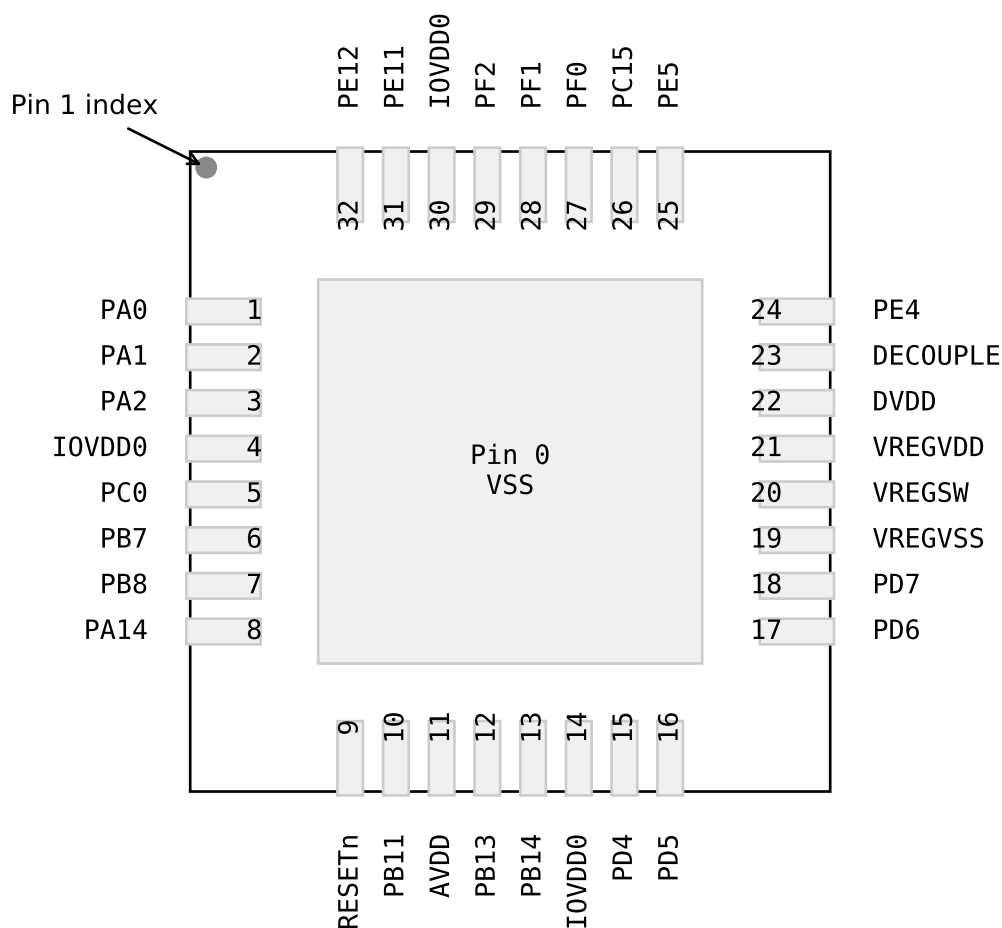


Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11 15	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	16	GPIO	PD5	17	GPIO
PD6	18	GPIO	PD7	19	GPIO
DVDD	20	Digital power supply.	DECOUPLE	21	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC13	22	GPIO (5V)	PC14	23	GPIO (5V)
PC15	24	GPIO (5V)	PF0	25	GPIO (5V)
PF1	26	GPIO (5V)	PF2	27	GPIO
PE10	29	GPIO	PE11	30	GPIO
PE12	31	GPIO	PE13	32	GPIO
Note: 1. GPIO with 5V tolerance are indicated by (5V).					

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4

7. QFN80 Package Specifications

7.1 QFN80 Package Dimensions

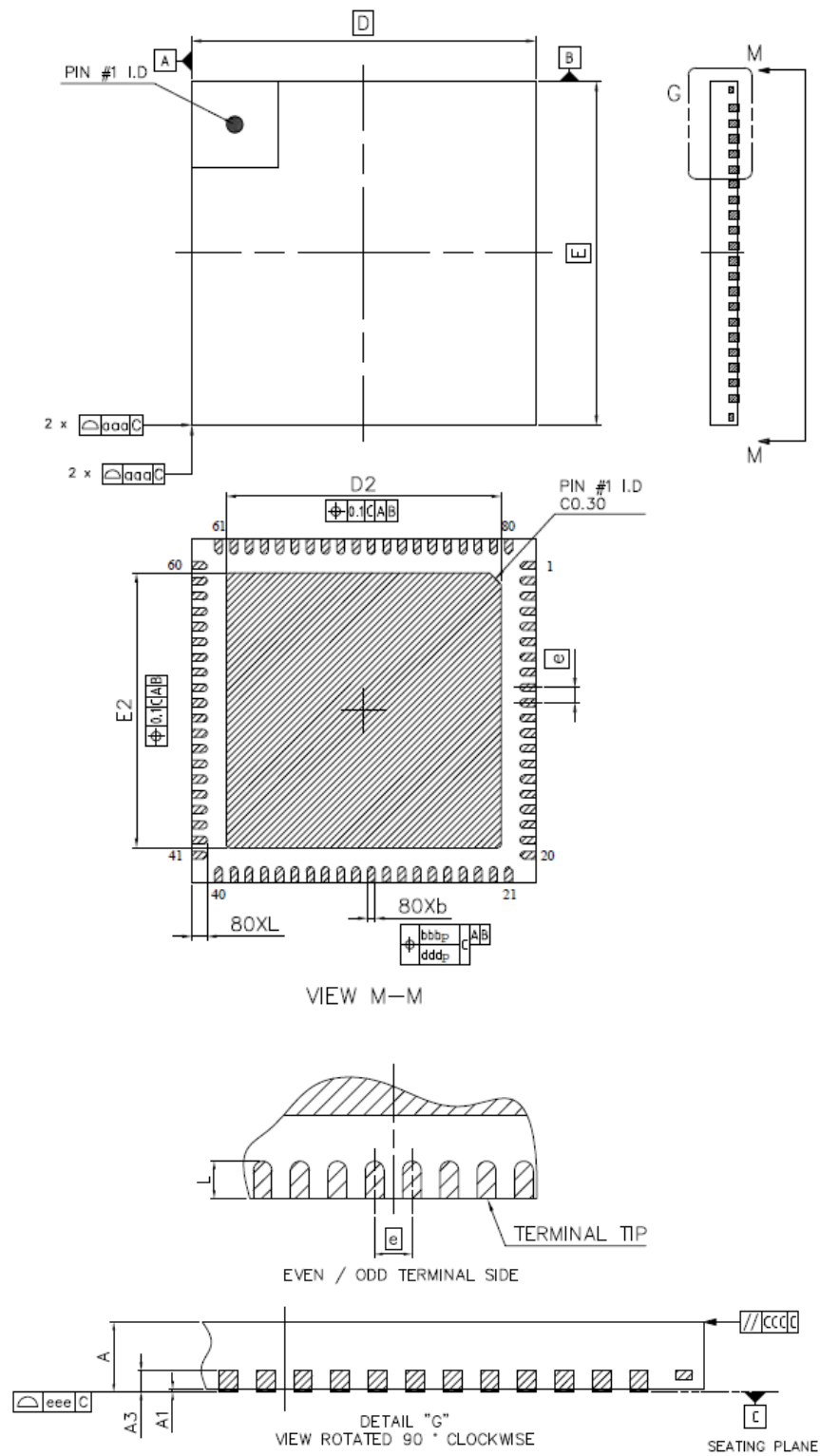


Figure 7.1. QFN80 Package Drawing

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions

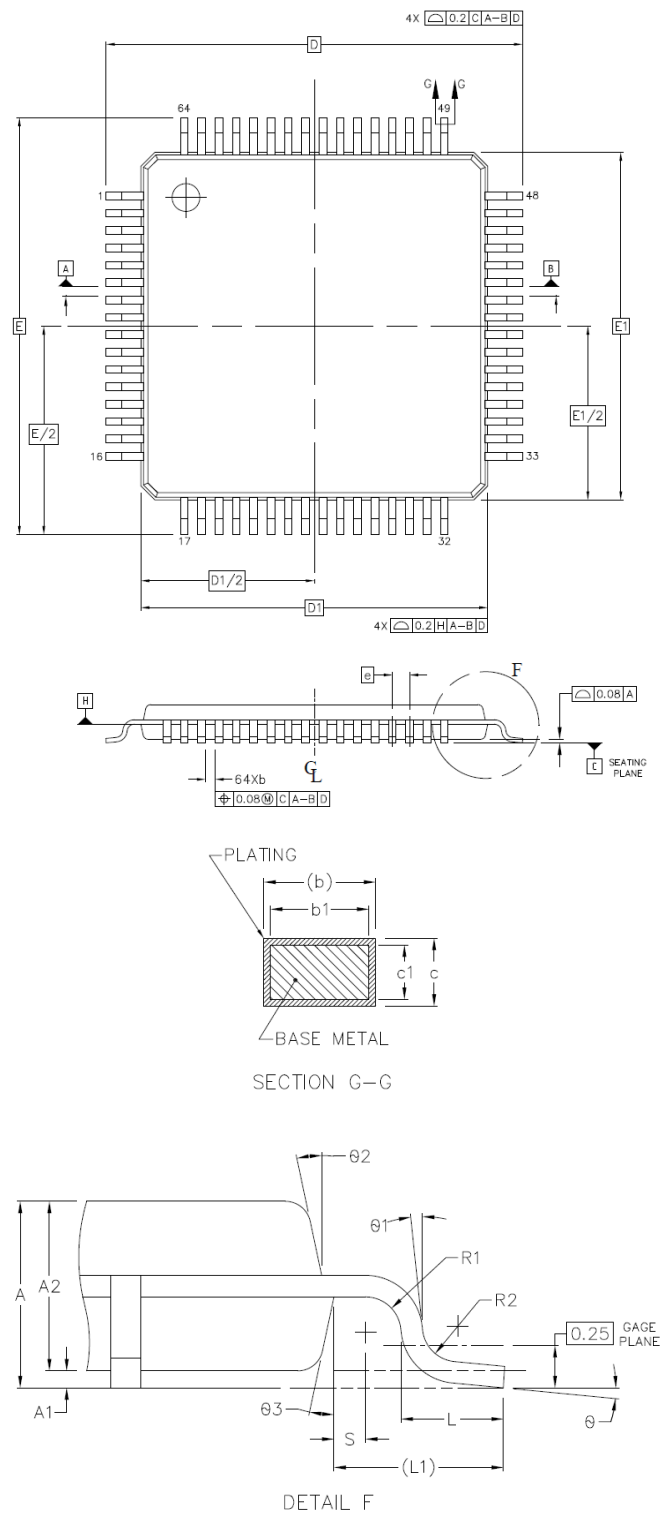


Figure 8.1. TQFP64 Package Drawing

Table 8.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

- Note:**
- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
 - 2. This Land Pattern Design is based on the IPC-7351 guidelines.
 - 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
 - 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
 - 5. The stencil thickness should be 0.125 mm (5 mils).
 - 6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
 - 7. A No-Clean, Type-3 solder paste is recommended.
 - 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 TQFP64 Package Marking



Figure 8.3. TQFP64 Package Marking

- The package marking consists of:
- P – The part number designation.
 - T – A trace or manufacturing code. The first letter is the device revision.
 - Y – The last 2 digits of the assembly year.
 - W – The 2-digit workweek when the device was assembled.

9.2 QFN64 PCB Land Pattern

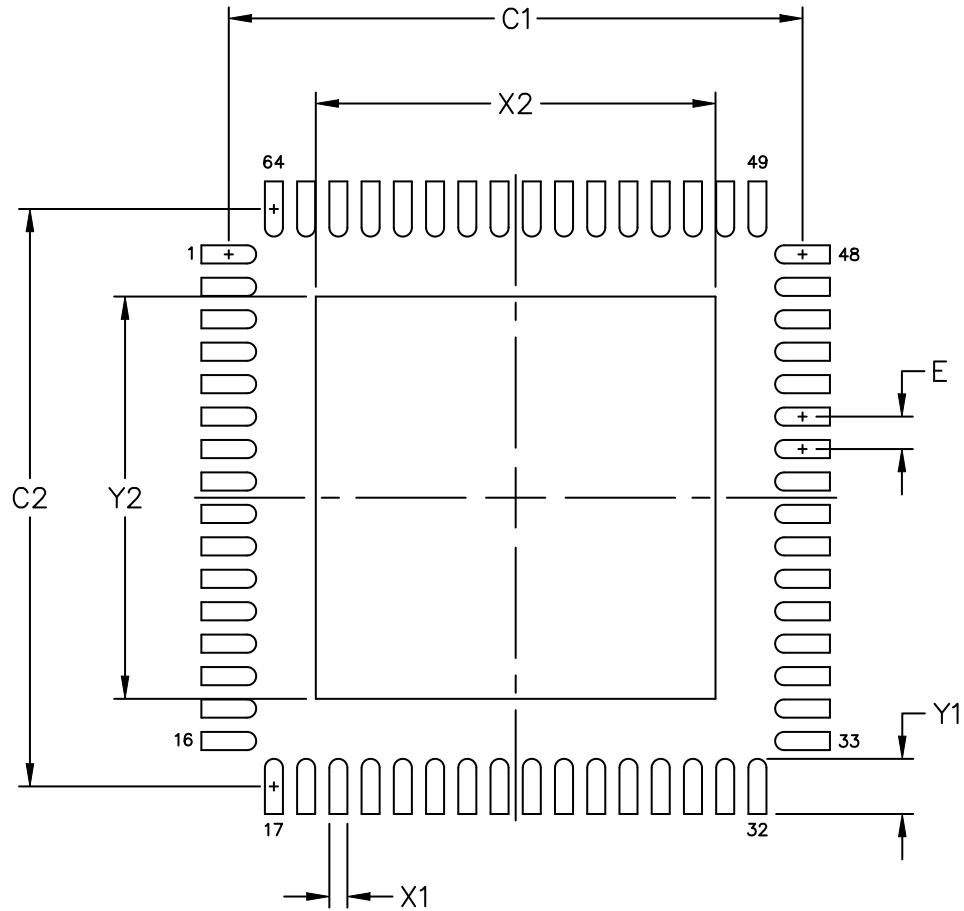


Figure 9.2. QFN64 PCB Land Pattern Drawing

11.2 QFN32 PCB Land Pattern

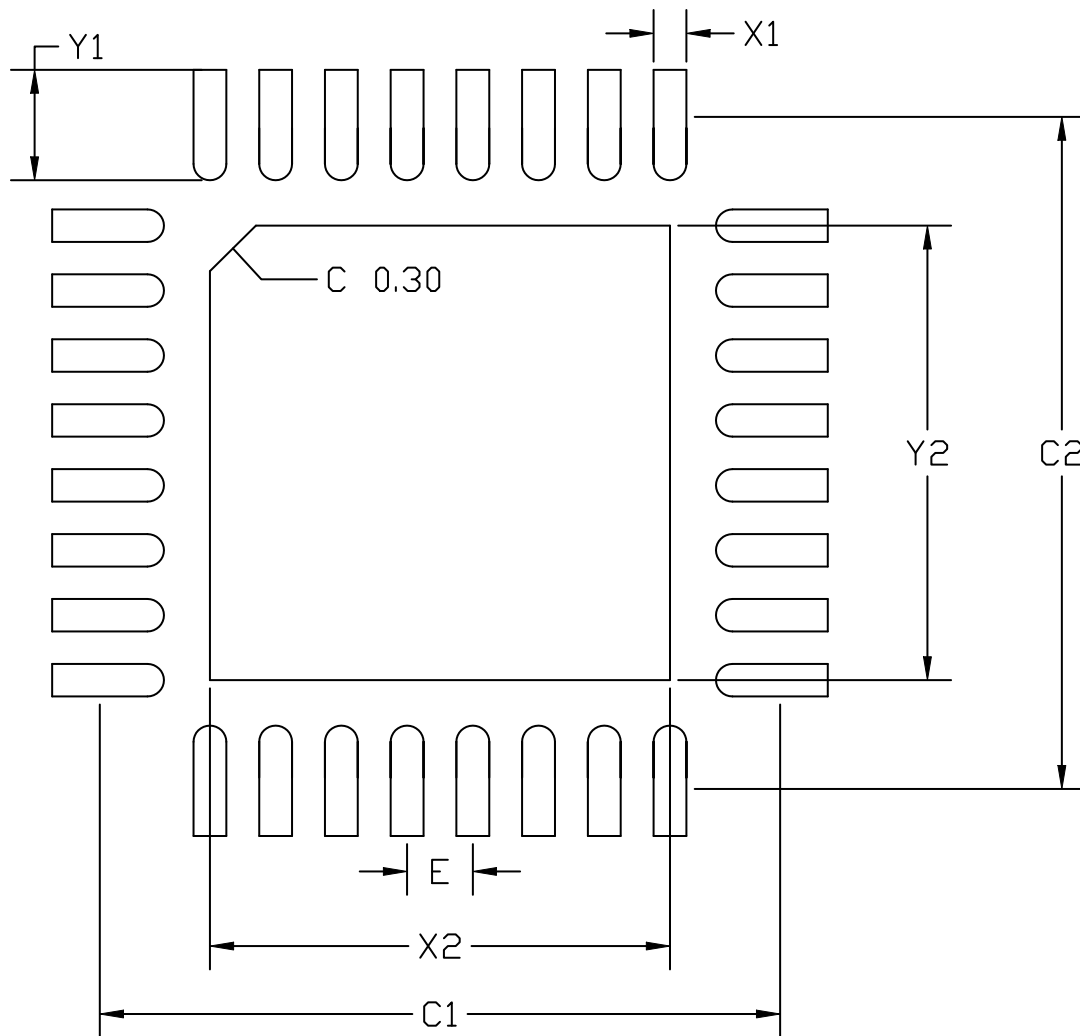


Figure 11.2. QFN32 PCB Land Pattern Drawing