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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b340f64iq64-ar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Timers/Counters

- 2 × 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
 - Dead-Time Insertion on one timer instance
- 2 × 32-bit Timer/Counter
- 32-bit Real Time Counter and Calendar (RTCC)
- 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
- 16-bit Low Energy Timer for waveform generation
- 16-bit Pulse Counter with asynchronous operation
- Watchdog Timer with dedicated RC oscillator
- Low Energy Sensor Interface (LESENSE)
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
 - Up to 16 inputs
- Ultra efficient Power-on Reset and Brown-Out Detector
- Debug Interface
 - 2-pin Serial Wire Debug interface
 - 4-pin JTAG interface
 - Micro Trace Buffer (MTB)

Pre-Programmed UART Bootloader

Wide Operating Range

- 1.8 V to 3.8 V single power supply
- Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
- Standard (-40 $^\circ C$ to 85 $^\circ C$ $T_A)$ and Extended (-40 $^\circ C$ to 125 $^\circ C$ $T_J)$ temperature grades available
- Packages
 - QFN32 (5x5 mm)
 - TQFP48 (7x7 mm)
 - QFN64 (9x9 mm)
 - TQFP64 (10x10 mm)
 - QFN80 (9x9 mm)
 - TQFP80 (12x12 mm)

3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Note:						
1. The minimum voltage req other loads can be calcula	uired in bypass mo ated as V _{DVDD_min}	ode is calculated using R _{BYP} from the +I _{LOAD} * R _{BYP_max} .	e DCDC spec	cification table	. Requiremen	ts for
2. VREGVDD must be tied t	o AVDD. Both VRI	EGVDD and AVDD minimum voltage	es must be sa	tisfied for the	part to operat	e.
 The system designer sho ue stays within the specifi 	uld consult the cha ied bounds across	racteristic specs of the capacitor use temperature and DC bias.	ed on DECOL	JPLE to ensur	e its capacita	nce val-
4. VSCALE0 to VSCALE2 v tion, peak currents will be mA (with a 2.7 μF capacit	oltage change tran dependent on the or).	sitions occur at a rate of 10 mV / use value of the DECOUPLE output cap	ec for approxi acitor, from 3	mately 20 use 35 mA (with a	ec. During this 1 μF capacito	s transi- r) to 70
5. When the CSEN peripher	al is used with cho	pping enabled (CSEN_CTRL_CHOF	PEN = ENABI	LE), IOVDD m	ust be equal	to AVDD.
6. The maximum limit on T _A cation. T _A (max) = T _J (ma Characteristics table for T	may be lower due ix) - (THETA _{JA} x P - _J and THETA _{JA} .	to device self-heating, which depend owerDissipation). Refer to the Absolution	ds on the pov ute Maximum	ver dissipatior Ratings table	of the specifies and the The	ic appli- rmal

4.1.3 Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Thermal resistance, QFN32	THETA _{JA_QFN32}	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	23.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	_	°C/W
Thermal resistance, TQFP48	THE-	4-Layer PCB, Air velocity = 0 m/s	—	44.1	_	°C/W
Раскаде	IAJA_TQFP48	4-Layer PCB, Air velocity = 1 m/s	—	43.5	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	_	°C/W
Thermal resistance, QFN64	THETA _{JA_QFN64}	4-Layer PCB, Air velocity = 0 m/s	—	20.9	_	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	18.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	_	°C/W
Thermal resistance, TQFP64	THE-	4-Layer PCB, Air velocity = 0 m/s	—	37.3	_	°C/W
Раскаде	IAJA_TQFP64	4-Layer PCB, Air velocity = 1 m/s	—	35.6	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	_	°C/W
Thermal resistance, QFN80	THETA _{JA_QFN80}	4-Layer PCB, Air velocity = 0 m/s	—	20.9	_	°C/W
Раскаде		4-Layer PCB, Air velocity = 1 m/s	—	18.2	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	_	°C/W
Thermal resistance, TQFP80	THE-	4-Layer PCB, Air velocity = 0 m/s	—	49.3	_	°C/W
Раскаде	je TA _{JA_TQFP80}	4-Layer PCB, Air velocity = 1 m/s	—	44.5	_	°C/W
		4-Layer PCB, Air velocity = 2 m/s		42.6		°C/W

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Wake up time from EM1	t _{EM1_WU}		_	3	_	AHB Clocks
Wake up from EM2	t _{EM2_WU}	Code execution from flash	—	10.1	_	μs
		Code execution from RAM	—	3.1	_	μs
Wake up from EM3	t _{EM3_WU}	Code execution from flash	—	10.1	_	μs
		Code execution from RAM	—	3.1	_	μs
Wake up from EM4H ¹	t _{EM4H_WU}	Executing from flash		88		μs
Wake up from EM4S ¹	t _{EM4S_WU}	Executing from flash	_	282	_	μs
Time from release of reset	t _{RESET}	Soft Pin Reset released	—	50	_	μs
ecution		Any other reset released	—	352		μs
Power mode scaling time	tSCALE	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2}	_	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ³	_	4.3	_	μs

Table 4.9. Wake Up Times

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.

2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).

3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.

4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Frequency limits	f _{HFRCO_BAND}	FREQRANGE = 0, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 3, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 6, FINETUNIN- GEN = 0	TBD	_	TBD	MHz
		FREQRANGE = 7, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 8, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 10, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 11, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 12, FINETUNIN- GEN = 0	TBD		TBD	MHz
		FREQRANGE = 13, FINETUNIN- GEN = 0	TBD		TBD	MHz

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Hysteresis (V _{CM} = 1.25 V,	V _{ACMPHYST}	HYSTSEL ⁵ = HYST0	TBD	0	TBD	mV
$BIASPROG^{4} = 0x10, FULL-$ $BIAS^{4} = 1)$		HYSTSEL ⁵ = HYST1	TBD	18	TBD	mV
		HYSTSEL ⁵ = HYST2	TBD	33	TBD	mV
		HYSTSEL ⁵ = HYST3	TBD	46	TBD	mV
		HYSTSEL ⁵ = HYST4	TBD	57	TBD	mV
		HYSTSEL ⁵ = HYST5	TBD	68	TBD	mV
		HYSTSEL ⁵ = HYST6	TBD	79	TBD	mV
		HYSTSEL ⁵ = HYST7	TBD	90	TBD	mV
		HYSTSEL ⁵ = HYST8	TBD	0	TBD	mV
		HYSTSEL ⁵ = HYST9	TBD	-18	TBD	mV
		HYSTSEL ⁵ = HYST10	TBD	-33	TBD	mV
		HYSTSEL ⁵ = HYST11	TBD	-45	TBD	mV
		HYSTSEL ⁵ = HYST12	TBD	-57	TBD	mV
		HYSTSEL ⁵ = HYST13	TBD	-67	TBD	mV
		HYSTSEL ⁵ = HYST14	TBD	-78	TBD	mV
		HYSTSEL ⁵ = HYST15	TBD	-88	TBD	mV
Comparator delay ³	t _{ACMPDELAY}	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	_	30	_	μs
		$BIASPROG^4 = 0x10, FULLBIAS^4 = 0$	_	3.7	_	μs
		$BIASPROG^4 = 0x02, FULLBIAS^4 = 1$	_	360	_	ns
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	_	35	_	ns
Offset voltage	VACMPOFFSET	BIASPROG ⁴ =0x10, FULLBIAS ⁴ = 1	TBD	_	TBD	mV
Reference voltage	V _{ACMPREF}	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal re-	R _{CSRES}	CSRESSEL ⁶ = 0	—	infinite	_	kΩ
		CSRESSEL ⁶ = 1	—	15	—	kΩ
		CSRESSEL ⁶ = 2	—	27	—	kΩ
		CSRESSEL ⁶ = 3	—	39	_	kΩ
		CSRESSEL ⁶ = 4	—	51		kΩ
		CSRESSEL ⁶ = 5	—	100	—	kΩ
		CSRESSEL ⁶ = 6	—	162	—	kΩ
		CSRESSEL ⁶ = 7		235		kΩ

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.22.	Digital to	Analog Converter	(VDAC)
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Output voltage	V _{DACOUT}	Single-Ended	0	_	V _{VREF}	V
		Differential ²	-V _{VREF}	—	V _{VREF}	V
Current consumption includ- ing references (2 channels) ¹	I _{DAC}	500 ksps, 12-bit, DRIVES- TRENGTH = 2, REFSEL = 4	_	396	_	μΑ
		44.1 ksps, 12-bit, DRIVES- TRENGTH = 1, REFSEL = 4	—	72	—	μA
		200 Hz refresh rate, 12-bit Sam- ple-Off mode in EM2, DRIVES- TRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WAR- MUPTIME = 0x02	_	2	_	μA
Current from HFPERCLK ⁴	IDAC_CLK		_	5.8		µA/MHz
Sample rate	SR _{DAC}		—	—	500	ksps
DAC clock frequency	f _{DAC}		—	—	1	MHz
Conversion time	t _{DACCONV}	f _{DAC} = 1MHz	2	_	_	μs
Settling time	t _{DACSETTLE}	50% fs step settling to 5 LSB		2.5		μs
Startup time	t _{DACSTARTUP}	Enable to 90% fs output, settling to 10 LSB	—	—	12	μs
Output impedance	R _{OUT}	$\label{eq:output} \begin{array}{l} DRIVESTRENGTH = 2,\ 0.4\ V \leq \\ V_{OUT} \leq V_{OPA} - 0.4\ V, -8\ mA < \\ I_{OUT} < 8\ mA, \ Full \ supply \ range \end{array}$	_	2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V $\leq V_{OUT} \leq V_{OPA} - 0.4 V$, -400 µA < $I_{OUT} < 400$ µA, Full supply range	_	2	_	Ω
		$\begin{array}{l} DRIVESTRENGTH = 2, \ 0.1 \ V \leq \\ V_{OUT} \leq V_{OPA} \ \text{-} \ 0.1 \ V, \ \text{-} 2 \ mA < \\ I_{OUT} < 2 \ mA, \ Full \ supply \ range \end{array}$		2	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$, -100 µA < $I_{OUT} < 100$ µA, Full supply range	_	2	_	Ω
Power supply rejection ratio ⁶	PSRR	Vout = 50% fs. DC		65.5	_	dB

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Note:						
 Supply current specification the load. 	ons are for VDAC	circuitry operating with static output o	only and do no	ot include curi	rent required	to drive
2. In differential mode, the o limited to the single-ender	utput is defined as d range.	the difference between two single-e	nded outputs	. Absolute vol	tage on each	output is
3. Entire range is monotonic	and has no missir	ng codes.				
4. Current from HFPERCLK the clock to the DAC mod	is dependent on H lule is enabled in th	IFPERCLK frequency. This current c ne CMU.	contributes to	the total supp	ly current use	ed when
5. Gain is calculated by mea 10% of full scale to ideal	asuring the slope fr VDAC output at 10	om 10% to 90% of full scale. Offset i % of full scale with the measured ga	is calculated t in.	by comparing	actual VDAC	output at
6. PSRR calculated as 20 *	log ₁₀ (ΔVDD / ΔV _O	_{UT}), VDAC output at 90% of full scale	е			

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3		135		dB
		DRIVESTRENGTH = 2	_	137	_	dB
		DRIVESTRENGTH = 1		121		dB
		DRIVESTRENGTH = 0		109		dB
Loop unit-gain frequency ⁷	UGF	DRIVESTRENGTH = 3, Buffer connection		3.38	_	MHz
		DRIVESTRENGTH = 2, Buffer connection		0.9	_	MHz
		DRIVESTRENGTH = 1, Buffer connection		132	_	kHz
		DRIVESTRENGTH = 0, Buffer connection		34	_	kHz
		DRIVESTRENGTH = 3, 3x Gain connection		2.57		MHz
		DRIVESTRENGTH = 2, 3x Gain connection	_	0.71	_	MHz
		DRIVESTRENGTH = 1, 3x Gain connection		113	_	kHz
		DRIVESTRENGTH = 0, 3x Gain connection		28	_	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	_	67	_	0
		DRIVESTRENGTH = 2, Buffer connection	—	69	_	o
		DRIVESTRENGTH = 1, Buffer connection	_	63	_	o
		DRIVESTRENGTH = 0, Buffer connection	_	68	_	o
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	_	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	_	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	_	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	_	176		µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	_	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	_	247	_	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz		245		µVrms

4.1.22 USART SPI

SPI Master Timing

Table 4.31. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}		2 * t _{HFPERCLK}	_	_	ns
CS to MOSI ^{1 3}	t _{CS_MO}		-19.8		18.9	ns
SCLK to MOSI ^{1 3}	t _{SCLK_MO}		-10		14.5	ns
MISO setup time ^{1 3}	t _{SU_MI}	IOVDD = 1.62 V	75	_		ns
		IOVDD = 3.0 V	40		_	ns
MISO hold time ^{1 3}	t _{H_MI}		-10			ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2. t_{HFPERCLK} is one period of the selected HFPERCLK.

3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).



Figure 4.1. SPI Master Timing Diagram

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB4	10	GPIO	PB5	11	GPIO
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.9. EFM32TG11B5xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 21 43	Digital IO power supply 0.
VSS	5 17 44	Ground	PB3	6	GPIO
PB4	7	GPIO	PB5	8	GPIO
PB6	9	GPIO	PB7	10	GPIO

GPIO Name		Pin Alternate Functionality / Description									
	Analog	Timers	Communication	Other							
PD5	BUSADC0Y BUSADC0X OPA2_OUT	WTIM0_CDTI1 #4 WTIM1_CC3 #1	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3								
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT OPA1_P	TIM1_CC0 #4 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_AL- TEX0 PRS_CH5 #2 ACMP0_O #2							
PD7	BUSADC0Y BUSADC0X ADC0_EXTN OPA1_N	TIM1_CC1 #4 WTIM1_CC1 #2 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_AL- TEX1 ACMP1_O #2							
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1							
PC6	BUSACMP0Y BU- SACMP0X OPA3_P LCD_SEG32	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 I2C0_SDA #2	LES_CH6							
PC7	BUSACMP0Y BU- SACMP0X OPA3_N LCD_SEG33	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 I2C0_SCL #2	LES_CH7							
PE4	BUSDY BUSCX LCD_COM0	WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 I2C0_SDA #7								
PE5	BUSCY BUSDX LCD_COM1	WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 I2C0_SCL #7								
PE6	BUSDY BUSCX LCD_COM2	WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2							
PE7	BUSCY BUSDX LCD_COM3	WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2							
PC8	BUSACMP1Y BU- SACMP1X LCD_SEG34		US0_CS #2	LES_CH8 PRS_CH4 #0							
PC9	BUSACMP1Y BU- SACMP1X LCD_SEG35		US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2							
PC10	BUSACMP1Y BU- SACMP1X		US0_RX #2	LES_CH10							
PC11	BUSACMP1Y BU- SACMP1X		US0_TX #2 I2C1_SDA #4	LES_CH11							
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BU- SACMP1Y BUSACMP1X	TIM1_CC3 #0	US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3	CMU_CLK0 #1 LES_CH12							
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BU- SACMP1Y BUSACMP1X	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3	LES_CH13							
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BU- SACMP1Y BUSACMP1X	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 LEU0_TX #5	LES_CH14 PRS_CH0 #2							

GPIO Name		Pin Alternate Functi		
	Analog	Timers	Communication	Other
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU- SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1
PE9	BUSCY BUSDX LCD_SEG5			
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE- TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL- TEX6 PRS_CH1 #3
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE- TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2	
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2	
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3	

Alternate	LOC	ATION	
Functionality	0 - 3	4 - 7	Description
U0_TX	2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13	USART0 chip select input / output.
US0_CTS	0: PE14 2: PC7 3: PC13	4: PB6 5: PB11	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 2: PC6 3: PC12	4: PB5 5: PD6	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0	USART0 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4	USART1 chip select input / output.
US1_CTS	1: PD4 2: PF3 3: PC6	4: PC12 5: PB13	USART1 Clear To Send hardware flow control input.
US1_RTS	1: PD5 2: PF4 3: PC7	4: PC13 5: PB14	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART1 Synchronous mode Master Output / Slave Input (MOSI).

Alternate	LOCA	ATION	
Functionality	0 - 3	4 - 7	Description
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP0X																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PCO
APORT0Y	BUSACMP0Y																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PCO
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				6A9				PA5		PA3		PA1	
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				6Yd				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				9AG		PA4		PA2		PA0
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		63d		PE7		PE5					
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 5.16. ACMP0 Bus and Pin Mapping

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
ОР	A1_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OP	PA1_	<u></u> P																															
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OP	A2_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VD	AC	0_0	UT1	/ 0	PA1	_οι	JT																										
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PFO		PE14		PE12		PE10		PE8		PE6		PE4				