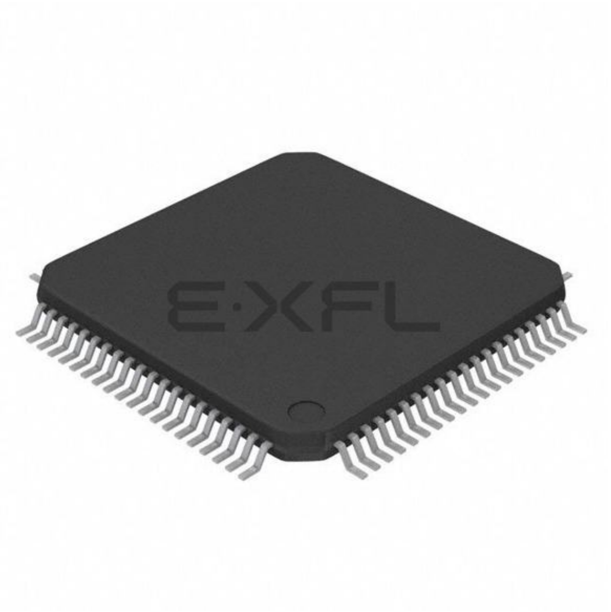

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b520f128gq80-a

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128IQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

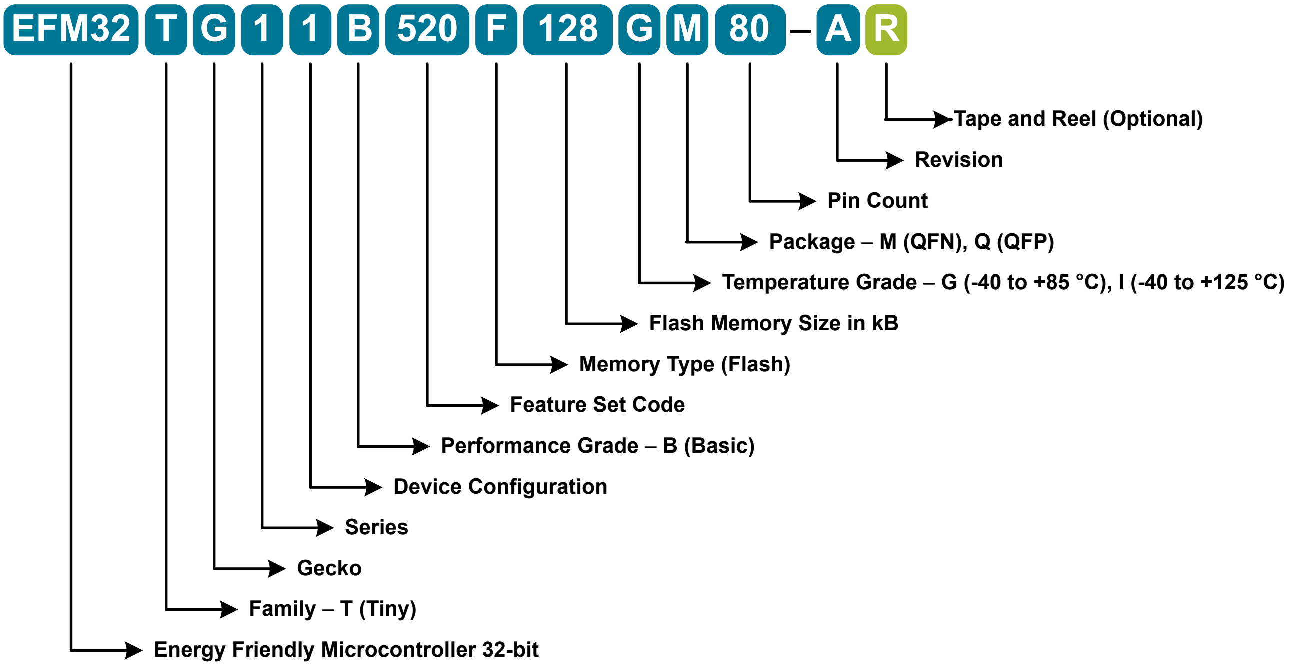

Figure 2.1. Ordering Code Key

3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC
-	LCD

3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

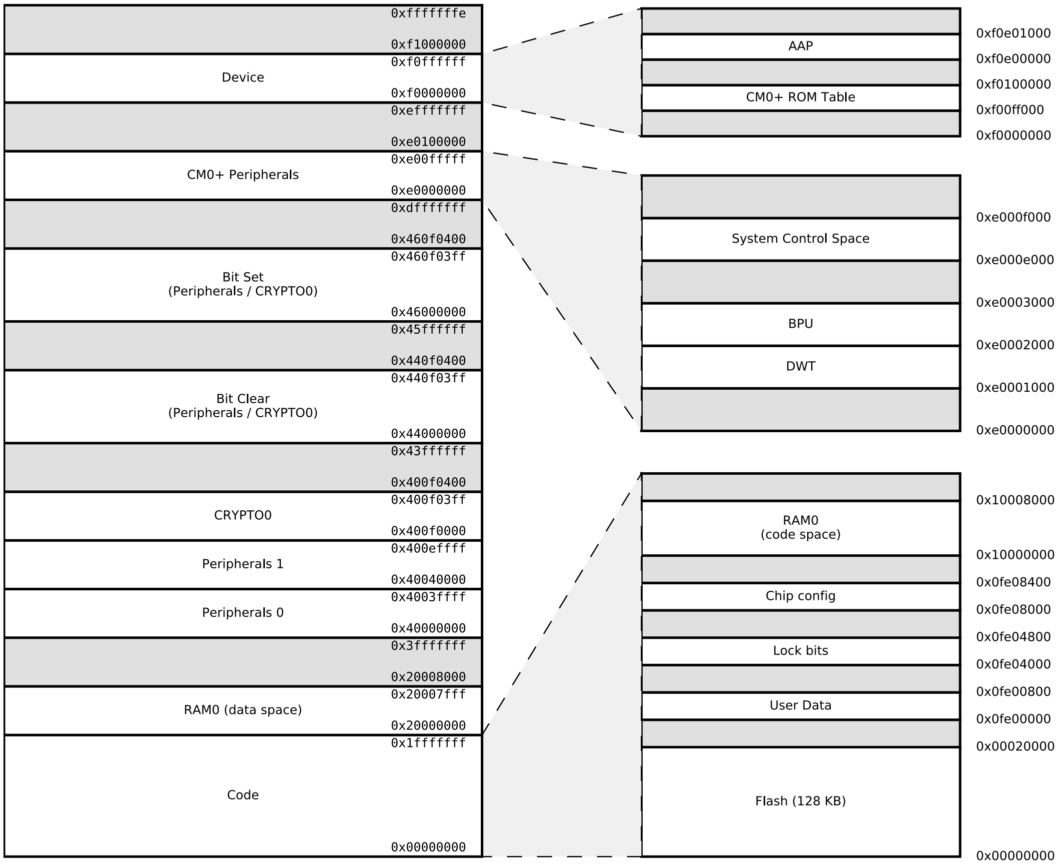

Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

4.1.6 Current Consumption

4.1.6.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	48 MHz crystal, CPU running while loop from flash	—	45	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	44	TBD	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	57	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	71	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	45	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	46	TBD	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	50	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	161	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	41	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	145	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	48 MHz crystal	—	34	—	µA/MHz
		48 MHz HFRCO	—	33	TBD	µA/MHz
		32 MHz HFRCO	—	34	—	µA/MHz
		26 MHz HFRCO	—	35	TBD	µA/MHz
		16 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	150	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	32	—	µA/MHz
		1 MHz HFRCO	—	136	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 32 kB RAM retention and RTCC running from LFXO	—	1.48	—	µA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.86	—	µA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	1.59	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.23	TBD	µA

4.1.10 Flash Memory Characteristics[5]

Table 4.17. Flash Memory Characteristics[5]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	26	32	µs
		Single word	59	68	83	µs
Page erase time[4]	t_{PERASE}		20	27	35	ms
Mass erase time[1]	t_{MERASE}		20	27	35	ms
Device erase time[2] [3]	t_{DERASE}	T ≤ 85 °C	—	54	70	ms
		T ≤ 125 °C	—	54	75	ms
Erase current[6]	I_{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.0	mA
Write current[6]	I_{WRITE}		—	—	3.5	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.12 Voltage Monitor (VMON)

Table 4.19. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.3	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	12.5	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[3]	DNL_{DAC}		TBD	—	TBD	LSB
Intergral non-linearity	INL_{DAC}		TBD	—	TBD	LSB
Offset error[5]	V_{OFFSET}	T = 25 °C	TBD	—	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error[5]	V_{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

4.1.21.2 I2C Fast-mode (Fm)[1]

Table 4.29. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

5.4 EFM32TG11B3xx in QFP64 Device Pinout

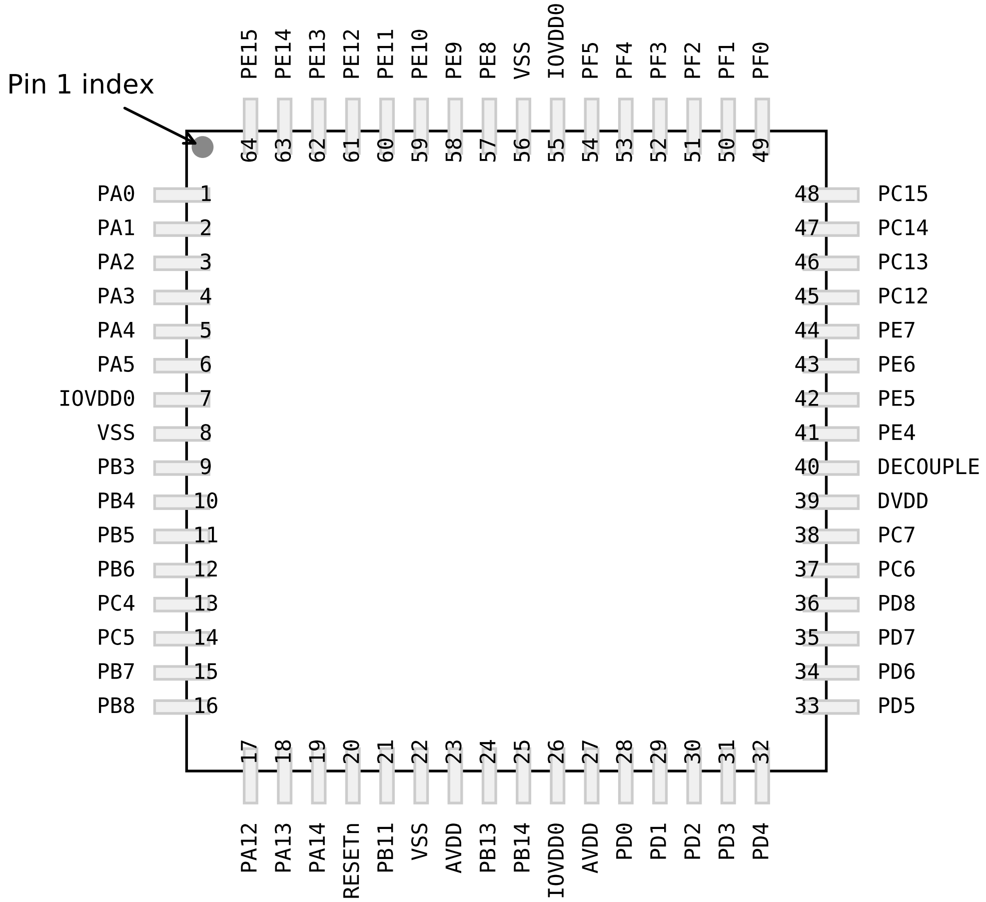

Figure 5.4. EFM32TG11B3xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.4. EFM32TG11B3xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.5 EFM32TG11B1xx in QFP64 Device Pinout

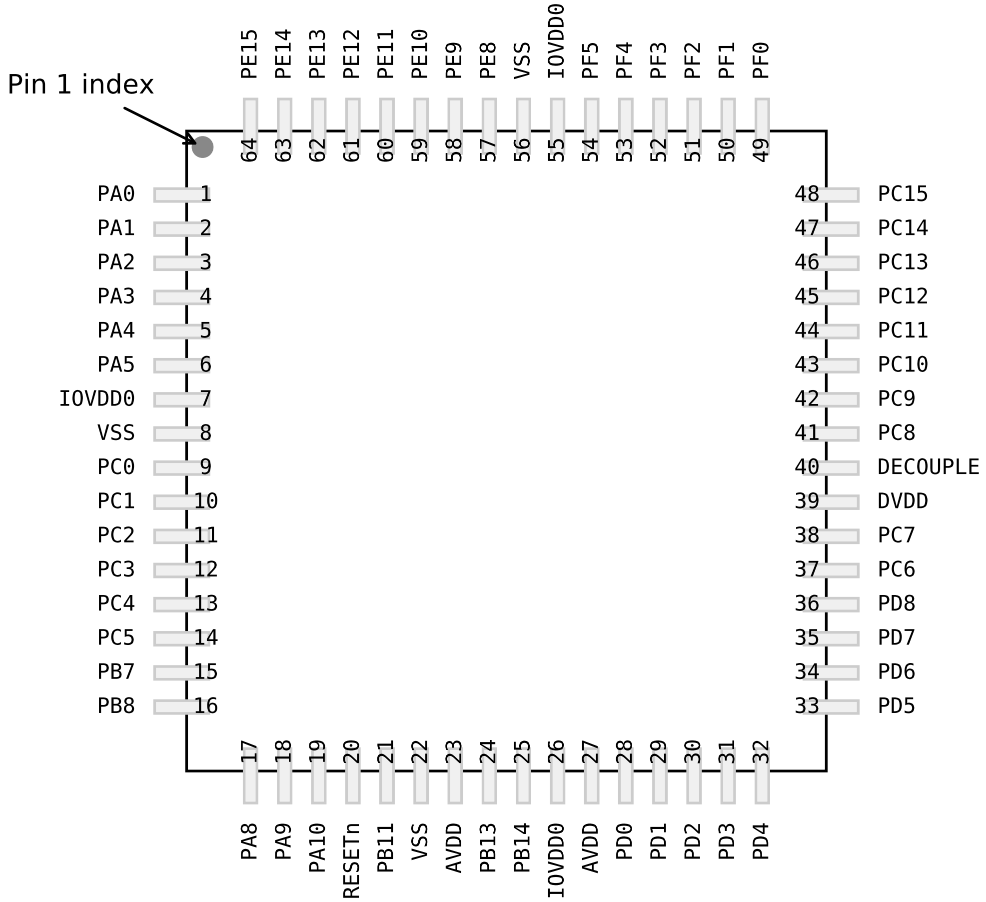

Figure 5.5. EFM32TG11B1xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.5. EFM32TG11B1xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PC0	9	GPIO (5V)	PC1	10	GPIO (5V)
PC2	11	GPIO (5V)	PC3	12	GPIO (5V)

5.7 EFM32TG11B3xx in QFN64 Device Pinout

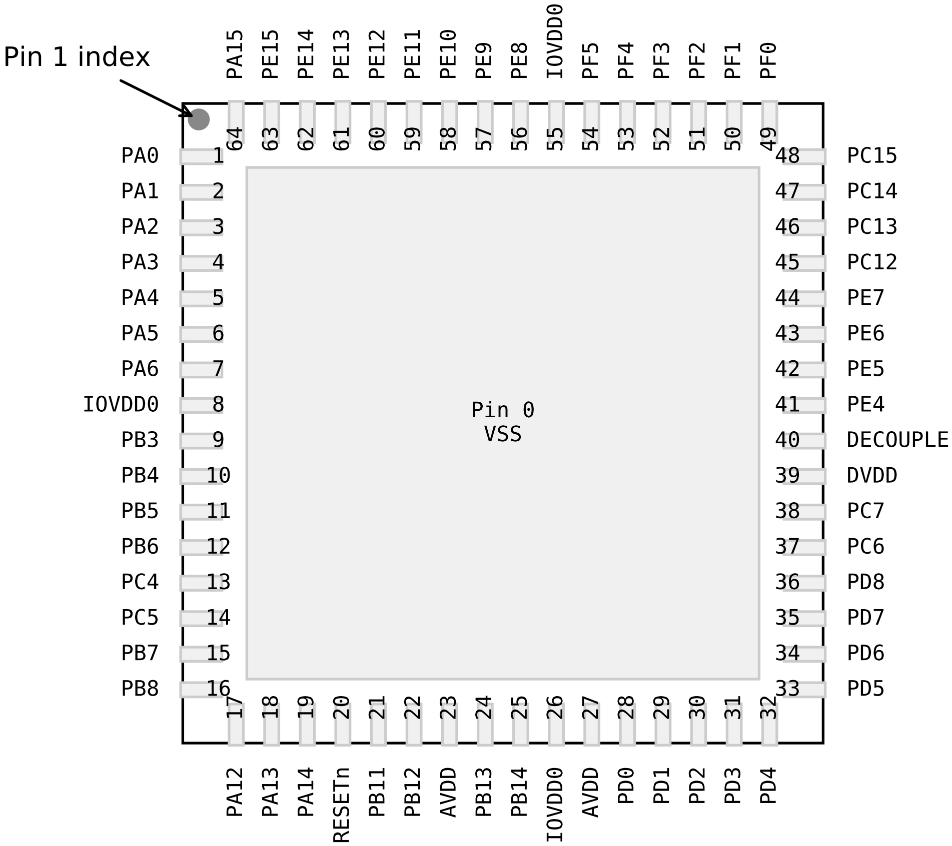

Figure 5.7. EFM32TG11B3xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.7. EFM32TG11B3xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA2_OUT																																	
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OPA2_P																																	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OPA3_N																																	
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 8.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 TQFP64 Package Marking

Figure 8.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 10.1. TQFP48 Package Dimensions

Dimension	Min	Typ	Max
A		7.00 BSC	
A1		3.50 BSC	
B		7.00 BSC	
B1		3.50 BSC	
C	1.00	—	1.20
D	0.17	—	0.27
E	0.95	—	1.05
F	0.17	—	0.23
G		0.50 BSC	
H	0.05	—	0.15
J	0.09	—	0.20
K	0.50	—	0.70
L	0	—	7
M		12 REF	
N	0.09	—	0.16
P		0.25 BSC	
R	0.150	—	0.250
S		9.00 BSC	
S1		4.50 BSC	
V		9.00 BSC	
V1		4.50 BSC	
W		0.20 BSC	
AA		1.00 BSC	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 QFN32 Package Marking

Figure 11.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.