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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b520f128im32-a

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128IQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

Table of Contents

1. Feature List	2
2. Ordering Information	4
3. System Overview	10
3.1 Introduction	10
3.2 Power	11
3.2.1 Energy Management Unit (EMU)	11
3.2.2 DC-DC Converter	11
3.2.3 EM2 and EM3 Power Domains	11
3.3 General Purpose Input/Output (GPIO)	12
3.4 Clocking	12
3.4.1 Clock Management Unit (CMU)	12
3.4.2 Internal and External Oscillators	12
3.5 Counters/Timers and PWM	12
3.5.1 Timer/Counter (TIMER)	12
3.5.2 Wide Timer/Counter (WTIMER)	12
3.5.3 Real Time Counter and Calendar (RTCC)	12
3.5.4 Low Energy Timer (LETIMER)	13
3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)	13
3.5.6 Pulse Counter (PCNT)	13
3.5.7 Watchdog Timer (WDOG)	13
3.6 Communications and Other Digital Peripherals	13
3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)	13
3.6.2 Universal Asynchronous Receiver/Transmitter (UART)	13
3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)	13
3.6.4 Inter-Integrated Circuit Interface (I ² C)	13
3.6.5 Controller Area Network (CAN)	14
3.6.6 Peripheral Reflex System (PRS)	14
3.6.7 Low Energy Sensor Interface (LESENSE)	14
3.7 Security Features	14
3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)	14
3.7.2 Crypto Accelerator (CRYPTO)	14
3.7.3 True Random Number Generator (TRNG)	14
3.7.4 Security Management Unit (SMU)	14
3.8 Analog	14
3.8.1 Analog Port (APORT)	15
3.8.2 Analog Comparator (ACMP)	15
3.8.3 Analog to Digital Converter (ADC)	15
3.8.4 Capacitive Sense (CSEN)	15
3.8.5 Digital to Analog Converter (VDAC)	15
3.8.6 Operational Amplifiers	15
3.8.7 Liquid Crystal Display Driver (LCD)	15
3.9 Reset Management Unit (RMU)	15

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD $\leq$ AVDD
- IOVDD $\leq$ AVDD

4.1.6 Current Consumption

4.1.6.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	48 MHz crystal, CPU running while loop from flash	—	45	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	44	TBD	μA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	57	—	μA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	71	—	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	45	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	46	TBD	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	50	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	161	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	41	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	145	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	48 MHz crystal	—	34	—	μA/MHz
		48 MHz HFRCO	—	33	TBD	μA/MHz
		32 MHz HFRCO	—	34	—	μA/MHz
		26 MHz HFRCO	—	35	TBD	μA/MHz
		16 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	150	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	32	—	μA/MHz
		1 MHz HFRCO	—	136	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I _{EM2_VS}	Full 32 kB RAM retention and RTCC running from LFXO	—	1.48	—	μA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.86	—	μA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	1.59	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 32 kB RAM retention and CRYOTIMER running from ULFR-CO	—	1.23	TBD	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode ³	IPD1_VS	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ⁴	—	0.18	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode ³	IPD2_VS	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ⁴	—	0.18	—	μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.3 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.
5. CMU_LFRCTRL_ENVREF = 1, CMU_LFRCTRL_VREFUPDATE = 1

4.1.14 Analog Comparator (ACMP)

Table 4.21. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG ⁴ ≤ 0x10 or FULL- BIAS ⁴ = 0	1.8	—	$V_{VREGVDD_MAX}$	V
		0x10 < BIASPROG ⁴ ≤ 0x20 and FULLBIAS ⁴ = 1	2.1	—	$V_{VREGVDD_MAX}$	V
Active current not including voltage reference ²	I_{ACMP}	BIASPROG ⁴ = 1, FULLBIAS ⁴ = 0	—	50	—	nA
		BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 0	—	306	—	nA
		BIASPROG ⁴ = 0x02, FULLBIAS ⁴ = 1	—	6.5	—	μA
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	—	74	TBD	μA
Current consumption of inter- nal voltage reference ²	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$)	$V_{ACMPHYST}$	$HYSTSEL^5 = HYST0$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST1$	TBD	18	TBD	mV
		$HYSTSEL^5 = HYST2$	TBD	33	TBD	mV
		$HYSTSEL^5 = HYST3$	TBD	46	TBD	mV
		$HYSTSEL^5 = HYST4$	TBD	57	TBD	mV
		$HYSTSEL^5 = HYST5$	TBD	68	TBD	mV
		$HYSTSEL^5 = HYST6$	TBD	79	TBD	mV
		$HYSTSEL^5 = HYST7$	TBD	90	TBD	mV
		$HYSTSEL^5 = HYST8$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST9$	TBD	-18	TBD	mV
		$HYSTSEL^5 = HYST10$	TBD	-33	TBD	mV
		$HYSTSEL^5 = HYST11$	TBD	-45	TBD	mV
		$HYSTSEL^5 = HYST12$	TBD	-57	TBD	mV
		$HYSTSEL^5 = HYST13$	TBD	-67	TBD	mV
		$HYSTSEL^5 = HYST14$	TBD	-78	TBD	mV
		$HYSTSEL^5 = HYST15$	TBD	-88	TBD	mV
Comparator delay ³	$t_{ACMPDELAY}$	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	—	30	—	μs
		$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 0$	—	3.7	—	μs
		$BIASPROG^4 = 0x02$, $FULLBIAS^4 = 1$	—	360	—	ns
		$BIASPROG^4 = 0x20$, $FULLBIAS^4 = 1$	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	$CSRESSEL^6 = 0$	—	infinite	—	k Ω
		$CSRESSEL^6 = 1$	—	15	—	k Ω
		$CSRESSEL^6 = 2$	—	27	—	k Ω
		$CSRESSEL^6 = 3$	—	39	—	k Ω
		$CSRESSEL^6 = 4$	—	51	—	k Ω
		$CSRESSEL^6 = 5$	—	100	—	k Ω
		$CSRESSEL^6 = 6$	—	162	—	k Ω
		$CSRESSEL^6 = 7$	—	235	—	k Ω

4.1.22 USART SPI

SPI Master Timing

Table 4.31. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		$2 * t_{HPERCLK}$	—	—	ns
CS to MOSI ^{1 3}	t_{CS_MO}		-19.8	—	18.9	ns
SCLK to MOSI ^{1 3}	t_{SCLK_MO}		-10	—	14.5	ns
MISO setup time ^{1 3}	t_{SU_MI}	IOVDD = 1.62 V	75	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time ^{1 3}	t_{H_MI}		-10	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HPERCLK}$ is one period of the selected HPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

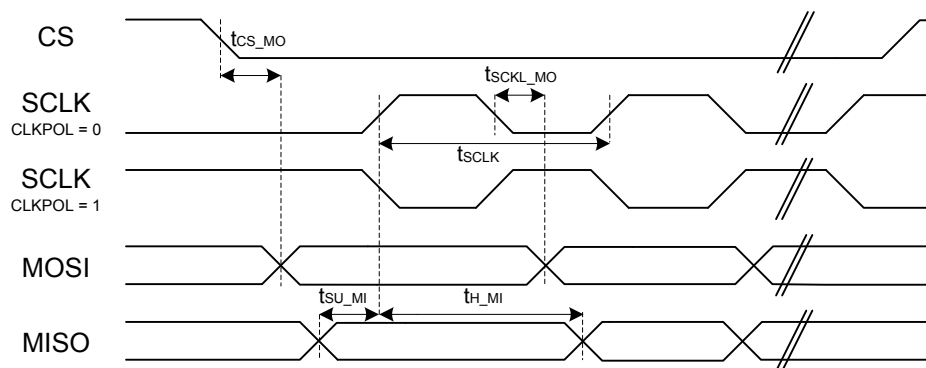


Figure 4.1. SPI Master Timing Diagram

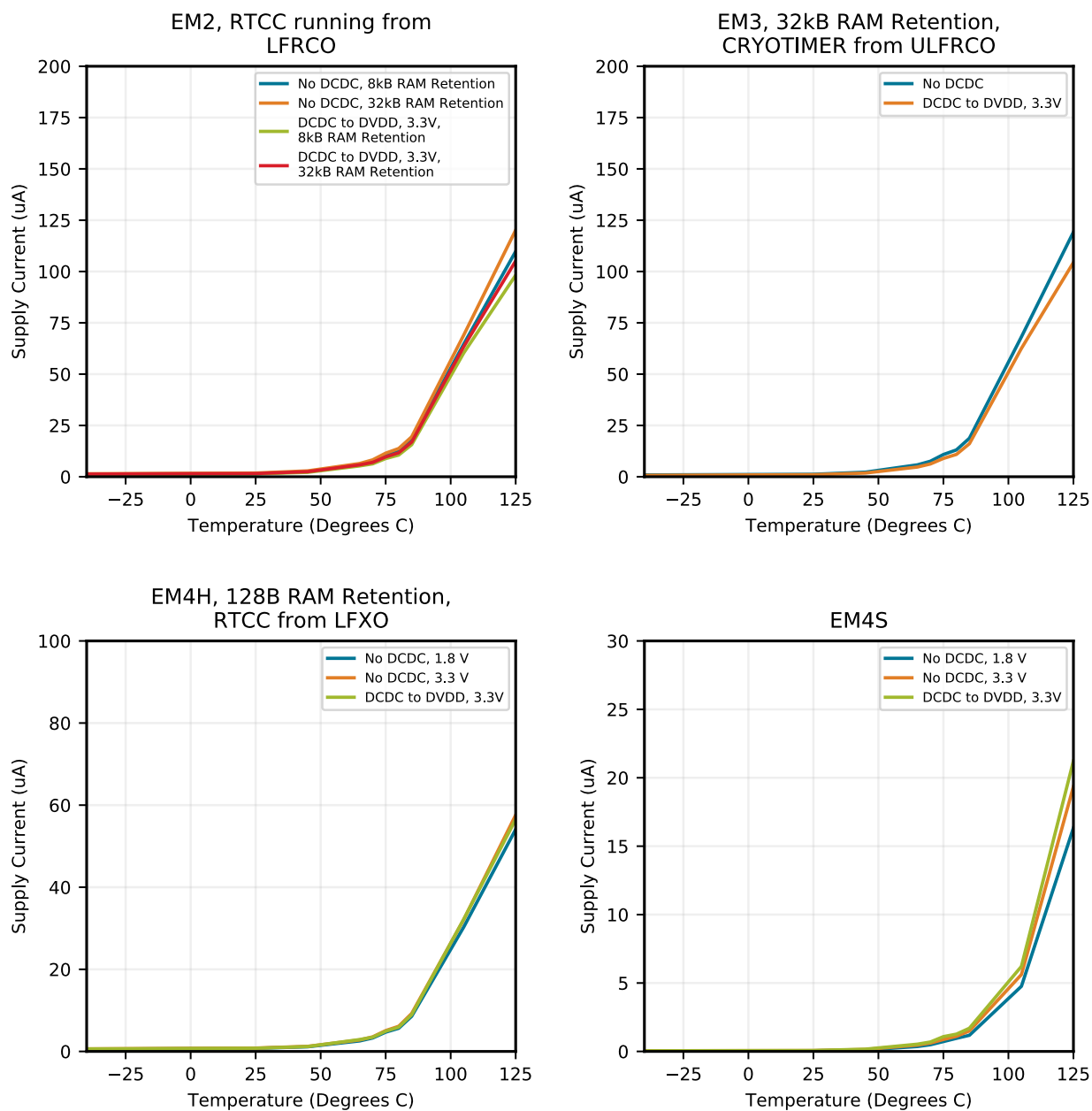


Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB7	11	GPIO	PB8	12	GPIO
PA12	13	GPIO	PA13	14	GPIO (5V)
PA14	15	GPIO	RESETn	16	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	17	GPIO	AVDD	19 23	Analog power supply.
PB13	20	GPIO	PB14	21	GPIO
PD4	24	GPIO	PD5	25	GPIO
PD6	26	GPIO	PD7	27	GPIO
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	30	GPIO	PE5	31	GPIO
PE6	32	GPIO	PE7	33	GPIO
PC13	34	GPIO (5V)	PC14	35	GPIO (5V)
PC15	36	GPIO (5V)	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.13 EFM32TG11B1xx in QFN32 Device Pinout

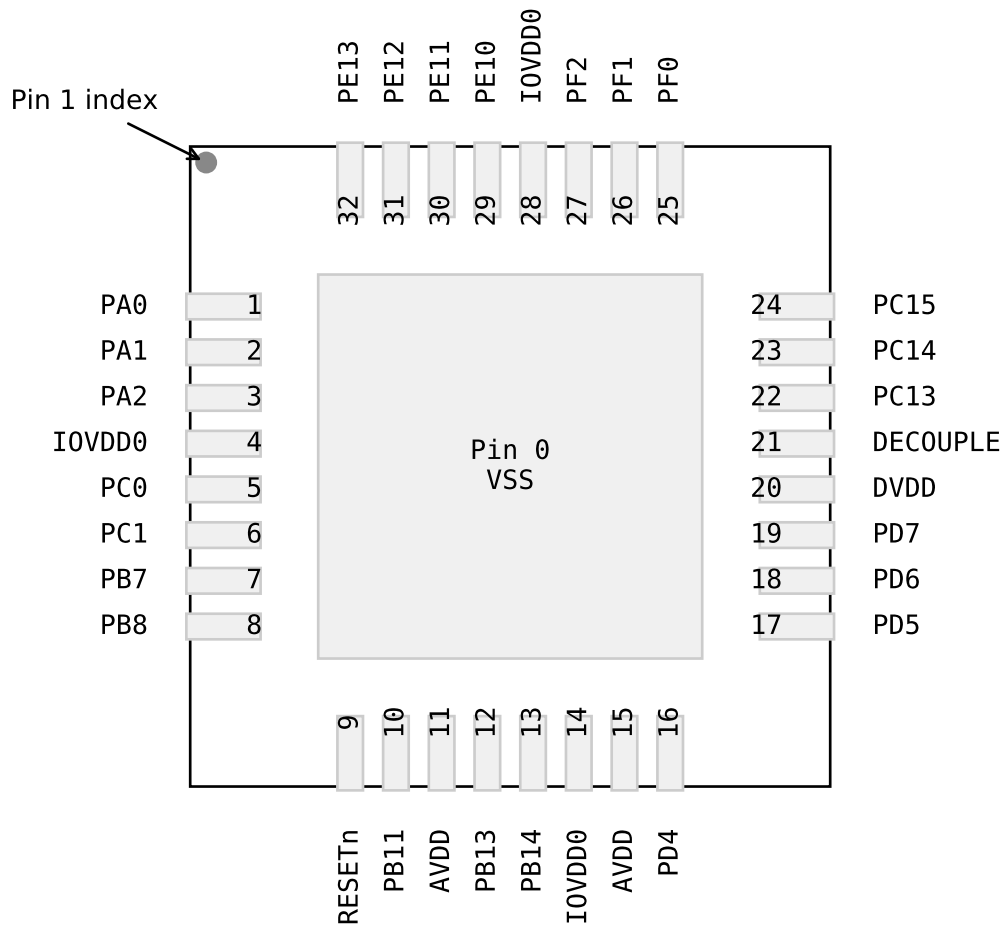


Figure 5.13. EFM32TG11B1xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.13. EFM32TG11B1xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 28	Digital IO power supply 0.	PC0	5	GPIO (5V)
PC1	6	GPIO (5V)	PB7	7	GPIO

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU- SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1
PE9	BUSCY BUSDX LCD_SEG5			
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE- TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL- TEX6 PRS_CH1 #3
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE- TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2	
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2	
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.

Table 5.20. VDACC0 / OPA Bus and Pin Mapping

[illegible]

7.3 QFN80 Package Marking



Figure 7.3. QFN80 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

Table 8.1. TQFP64 Package Dimensions

Dimension	Min	Typ	Max
A	—	1.15	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0	3.5	7
Θ1	0	—	0.10
Θ2	11	12	13
Θ3	11	12	13
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

Table 9.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN64 Package Marking



Figure 9.3. QFN64 Package Marking

The package marking consists of:

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- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
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