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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b520f128iq48-a

1. Feature List

The EFM32TG11 highlighted features are listed below.

- **ARM Cortex-M0+ CPU platform**
  - High performance 32-bit processor @ up to 48 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 37 μA/MHz in Active Mode (EM0)
  - 1.30 μA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power absent/ insufficient
- **Up to 128 kB flash program memory**
- **Up to 32 kB RAM data memory**
- **Communication Interfaces**
  - CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (24 MHz) operation on one instance
  - 1 × Universal Asynchronous Receiver/ Transmitter
  - 1 × Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2 × I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 67 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 8 Channel DMA Controller**
- **Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 × 32 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Up to 2 × Analog Comparator (ACMP)
  - Up to 4 × Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
  - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

3.6.5 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmittion may be disabled in order to support Time Triggered CAN applications.

3.6.6 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.7 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE^{TM} is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Tiny Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

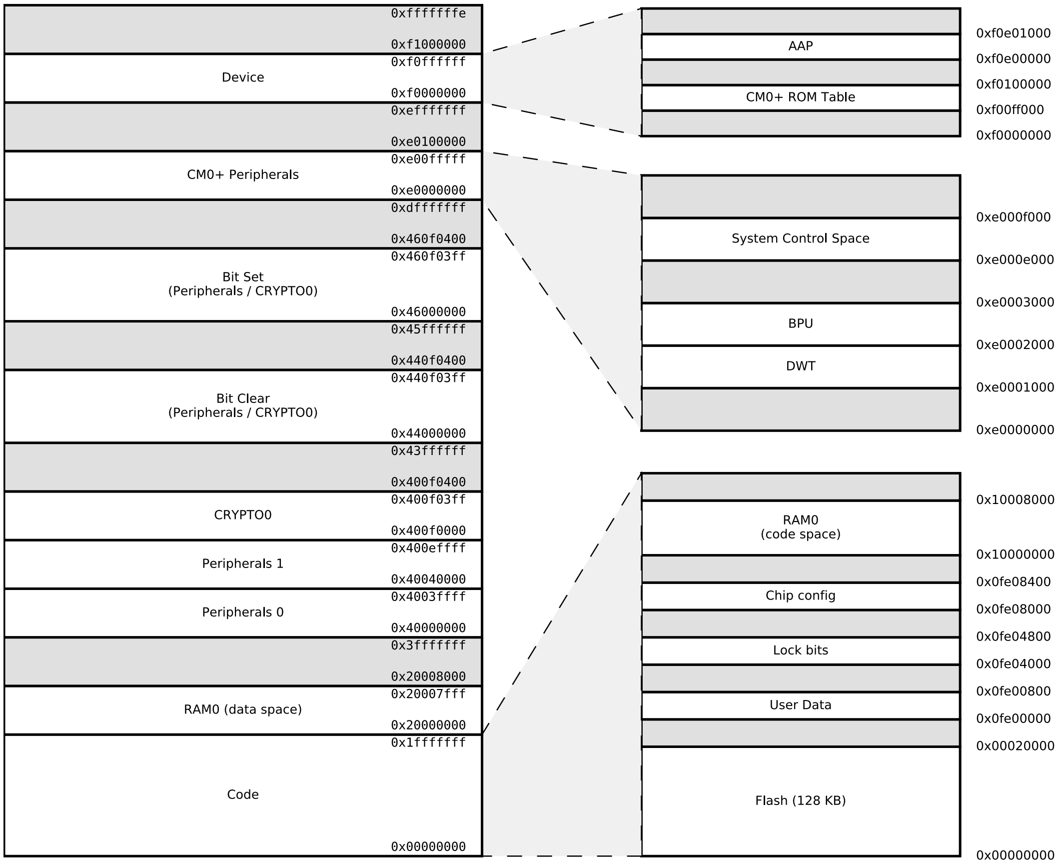

Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 μA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	10	TBD	nA
		BU_VIN powering backup domain[1]	—	450	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

4.1.6 Current Consumption

4.1.6.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	48 MHz crystal, CPU running while loop from flash	—	45	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	44	TBD	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	—	57	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	71	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	45	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	46	TBD	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	50	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	161	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	41	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	145	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	48 MHz crystal	—	34	—	µA/MHz
		48 MHz HFRCO	—	33	TBD	µA/MHz
		32 MHz HFRCO	—	34	—	µA/MHz
		26 MHz HFRCO	—	35	TBD	µA/MHz
		16 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	150	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	32	—	µA/MHz
		1 MHz HFRCO	—	136	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 32 kB RAM retention and RTCC running from LFXO	—	1.48	—	µA
		Full 32 kB RAM retention and RTCC running from LFRCO	—	1.86	—	µA
		8 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	1.59	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.23	TBD	µA

4.1.9.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.15. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{AUXHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	$t_{AUXHFRCO}$	$f_{AUXHFRCO} \geq 19$ MHz	—	400	—	ns
		$4 < f_{AUXHFRCO} < 19$ MHz	—	1.4	—	µs
		$f_{AUXHFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	$I_{AUXHFRCO}$	$f_{AUXHFRCO} = 48$ MHz	—	238	TBD	µA
		$f_{AUXHFRCO} = 38$ MHz	—	196	TBD	µA
		$f_{AUXHFRCO} = 32$ MHz	—	160	TBD	µA
		$f_{AUXHFRCO} = 26$ MHz	—	137	TBD	µA
		$f_{AUXHFRCO} = 19$ MHz	—	110	TBD	µA
		$f_{AUXHFRCO} = 16$ MHz	—	101	TBD	µA
		$f_{AUXHFRCO} = 13$ MHz	—	78	TBD	µA
		$f_{AUXHFRCO} = 7$ MHz	—	54	TBD	µA
		$f_{AUXHFRCO} = 4$ MHz	—	30	TBD	µA
		$f_{AUXHFRCO} = 2$ MHz	—	27	TBD	µA
		$f_{AUXHFRCO} = 1$ MHz	—	25	TBD	µA
Coarse trim step size (% of period)	$SS_{AUXHFRCO\_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{AUXHFRCO\_FINE}$		—	0.1	—	%
Period jitter	$PJ_{AUXHFRCO}$		—	0.2	—	% RMS

4.1.9.6 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.16. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

4.1.12 Voltage Monitor (VMON)

Table 4.19. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.3	TBD	µA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	12.5	TBD	µA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.20. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	μA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	μA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	166	—	μA

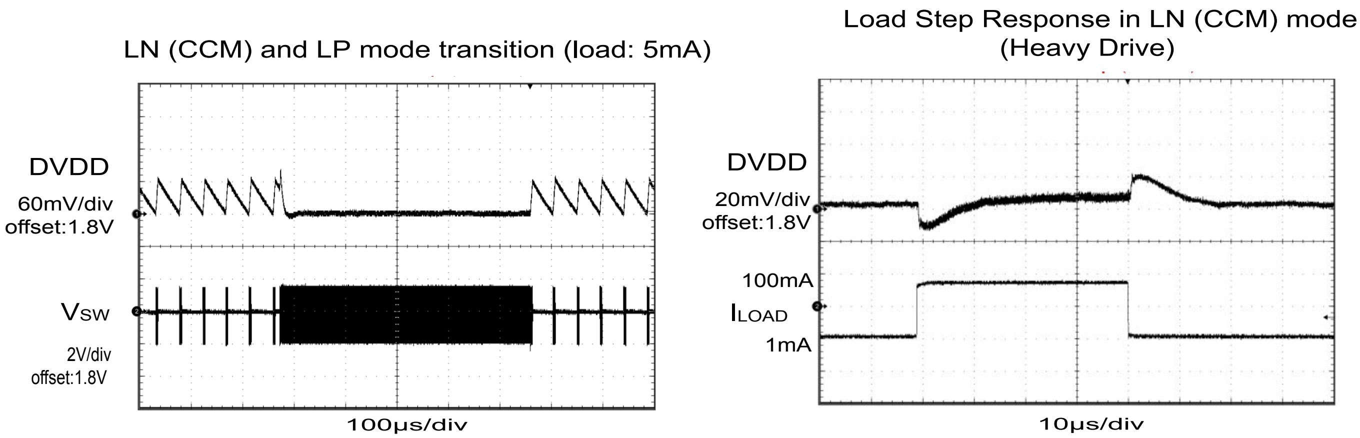

Figure 4.9. DC-DC Converter Transition Waveforms

5. Pin Definitions

5.1 EFM32TG11B5xx in QFP80 Device Pinout

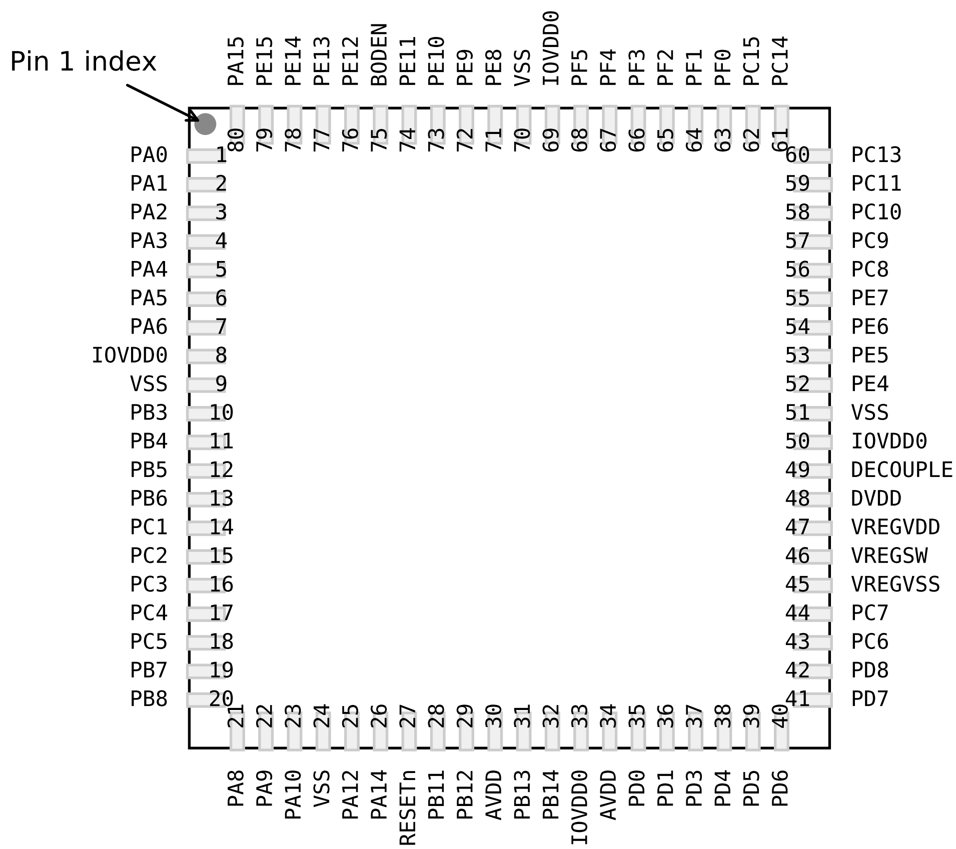

Figure 5.1. EFM32TG11B5xx in QFP80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.1. EFM32TG11B5xx in QFP80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 33 50 69	Digital IO power supply 0.

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PD5	BUSADC0Y BUSADC0X OPA2_OUT	WTIM0_CDTI1 #4 WTIM1_CC3 #1	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT OPA1_P	TIM1_CC0 #4 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_AL-TEX0 PRS_CH5 #2 ACMP0_O #2
PD7	BUSADC0Y BUSADC0X ADC0_EXTN OPA1_N	TIM1_CC1 #4 WTIM1_CC1 #2 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_AL-TEX1 ACMP1_O #2
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1
PC6	BUSACMP0Y BU-SACMP0X OPA3_P LCD_SEG32	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 I2C0_SDA #2	LES_CH6
PC7	BUSACMP0Y BU-SACMP0X OPA3_N LCD_SEG33	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 I2C0_SCL #2	LES_CH7
PE4	BUSDY BUSCX LCD_COM0	WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 I2C0_SDA #7	
PE5	BUSCY BUSDX LCD_COM1	WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 I2C0_SCL #7	
PE6	BUSDY BUSCX LCD_COM2	WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2
PE7	BUSCY BUSDX LCD_COM3	WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2
PC8	BUSACMP1Y BU-SACMP1X LCD_SEG34		US0_CS #2	LES_CH8 PRS_CH4 #0
PC9	BUSACMP1Y BU-SACMP1X LCD_SEG35		US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC10	BUSACMP1Y BU-SACMP1X		US0_RX #2	LES_CH10
PC11	BUSACMP1Y BU-SACMP1X		US0_TX #2 I2C1_SDA #4	LES_CH11
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BU-SACMP1Y BUSACMP1X	TIM1_CC3 #0	US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3	CMU_CLK0 #1 LES_CH12
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BU-SACMP1Y BUSACMP1X	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3	LES_CH13
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BU-SACMP1Y BUSACMP1X	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 LEU0_TX #5	LES_CH14 PRS_CH0 #2

5.15 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.14 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.15. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 2: PD6 3: PB11	4: PA6 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 2: PD7 3: PA12	4: PA14 7: PA5	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.
BU_STAT	0: PA8		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PA12		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0		CAN0 RX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM0_CC0	0: PA0 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 2: PD3 3: PC1	4: PF2 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 3: PB7	4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 3: PB8	4: PD7 5: PF3	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 3: PB11	4: PC13 5: PF4	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 6: PF5	Timer 1 Capture Compare input / output channel 3.
U0_CTS	 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 5.17. ACMP1 Bus and Pin Mapping

Port	APORT0X	APORT0Y	APORT1X	APORT1Y	APORT2X	APORT2Y	APORT3X	APORT3Y	APORT4X	APORT4Y
Bus	BUSACMP1X	BUSACMP1Y	BUSAX	BUSAY	BUSBX	BUSBY	BUSCX	BUSCY	BUSDX	BUSDY
CH31										
CH30			PB14			PB14				
CH29				PB13	PB13					
CH28			PB12			PB12				
CH27				PB11	PB11					
CH26										
CH25										
CH24										
CH23										
CH22			PB6			PB6				
CH21				PB5	PB5			PF5	PF5	
CH20			PB4			PB4	PF4			PF4
CH19				PB3	PB3			PF3	PF3	
CH18							PF2			PF2
CH17								PF1	PF1	
CH16							PF0			PF0
CH15				PA15	PA15			PE15	PE15	
CH14			PA14			PA14	PE14			PE14
CH13				PA13	PA13			PE13	PE13	
CH12							PE12			PE12
CH11								PE11	PE11	
CH10			PA10			PA10	PE10			PE10
CH9				PA9	PA9			PE9	PE9	
CH8							PE8			PE8
CH7	PC15	PC15						PE7	PE7	
CH6	PC14	PC14	PA6			PA6	PE6			PE6
CH5	PC13	PC13		PA5	PA5			PE5	PE5	
CH4	PC12	PC12	PA4			PA4	PE4			PE4
CH3	PC11	PC11		PA3	PA3					
CH2	PC10	PC10	PA2			PA2				
CH1	PC9	PC9		PA1	PA1					
CH0	PC8	PC8	PA0			PA0				

Table 5.20. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OPA0_P																																	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					

6. TQFP80 Package Specifications

6.1 TQFP80 Package Dimensions

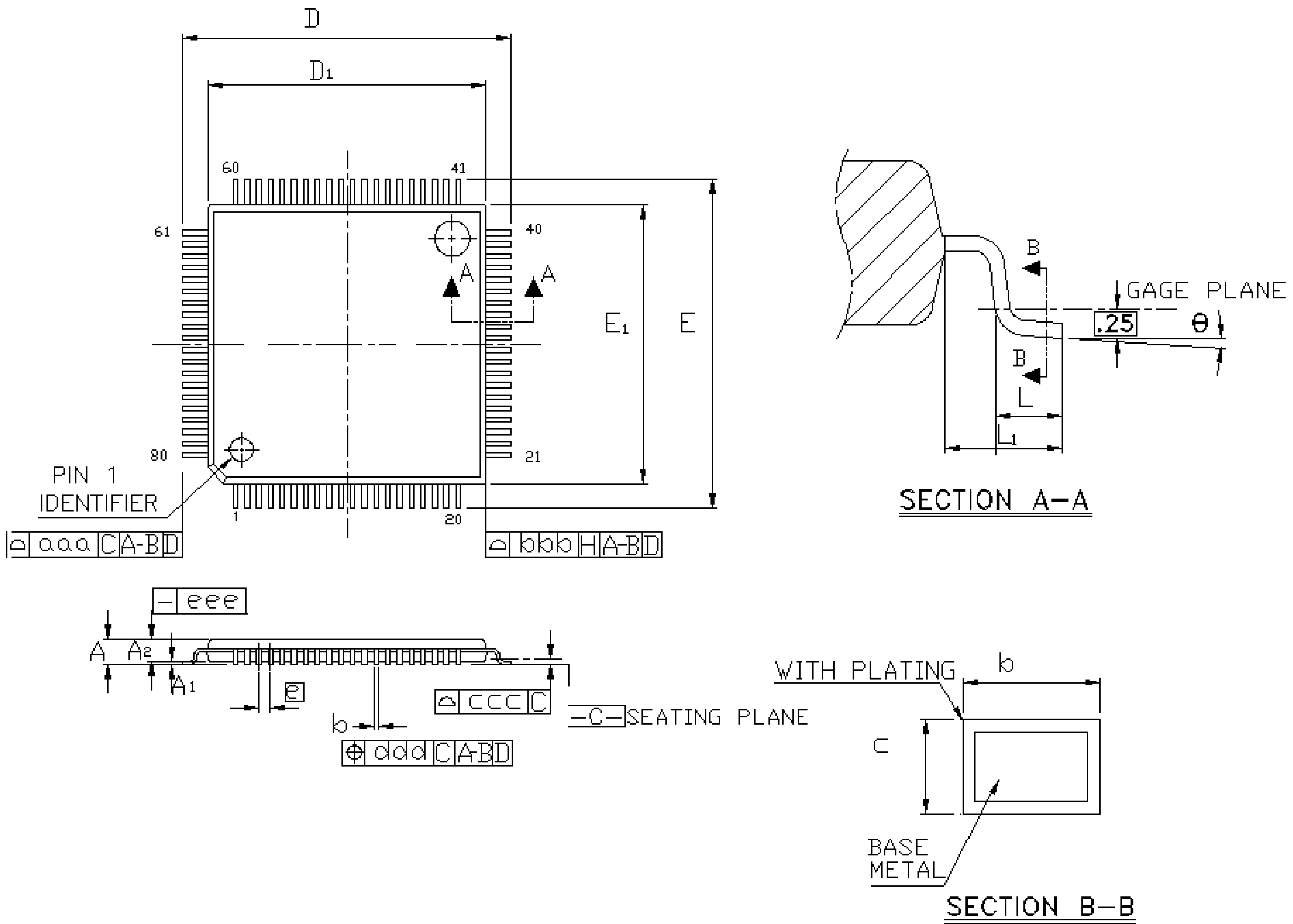

Figure 6.1. TQFP80 Package Drawing

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions

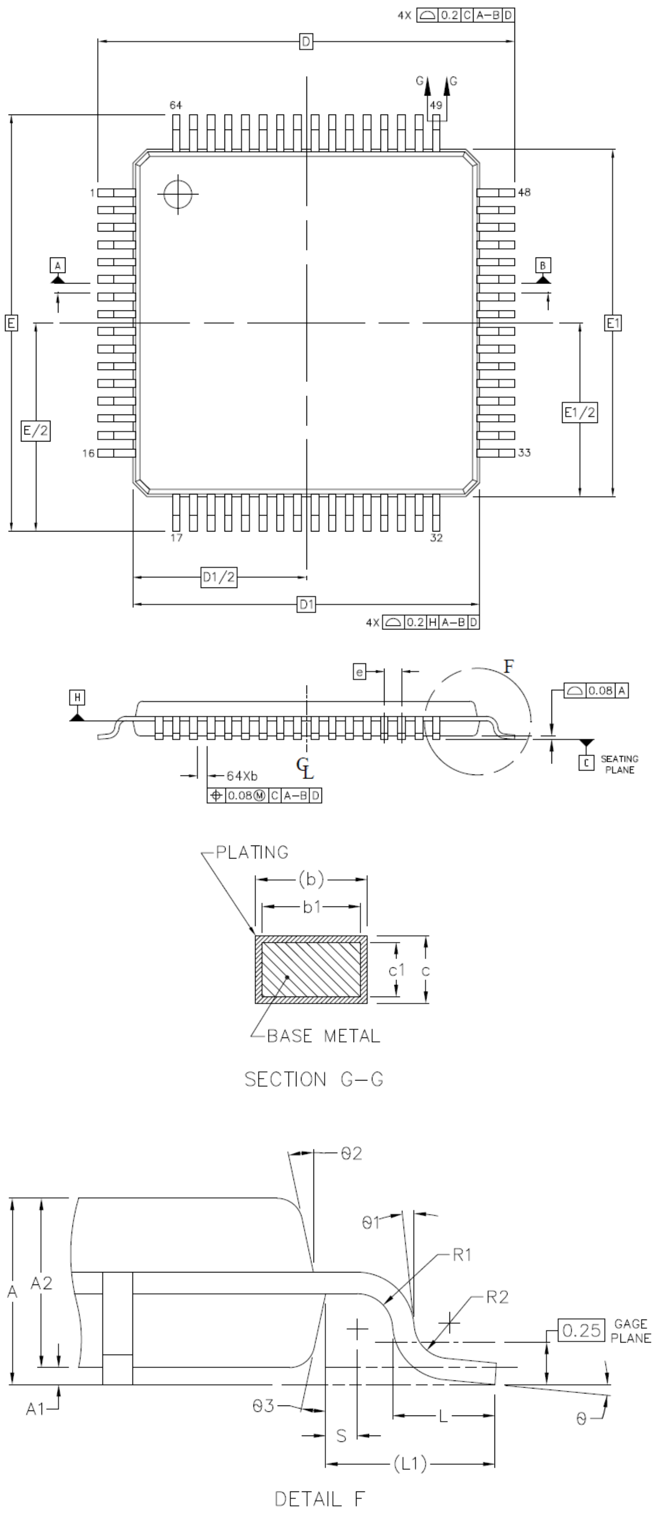

Figure 8.1. TQFP64 Package Drawing

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions

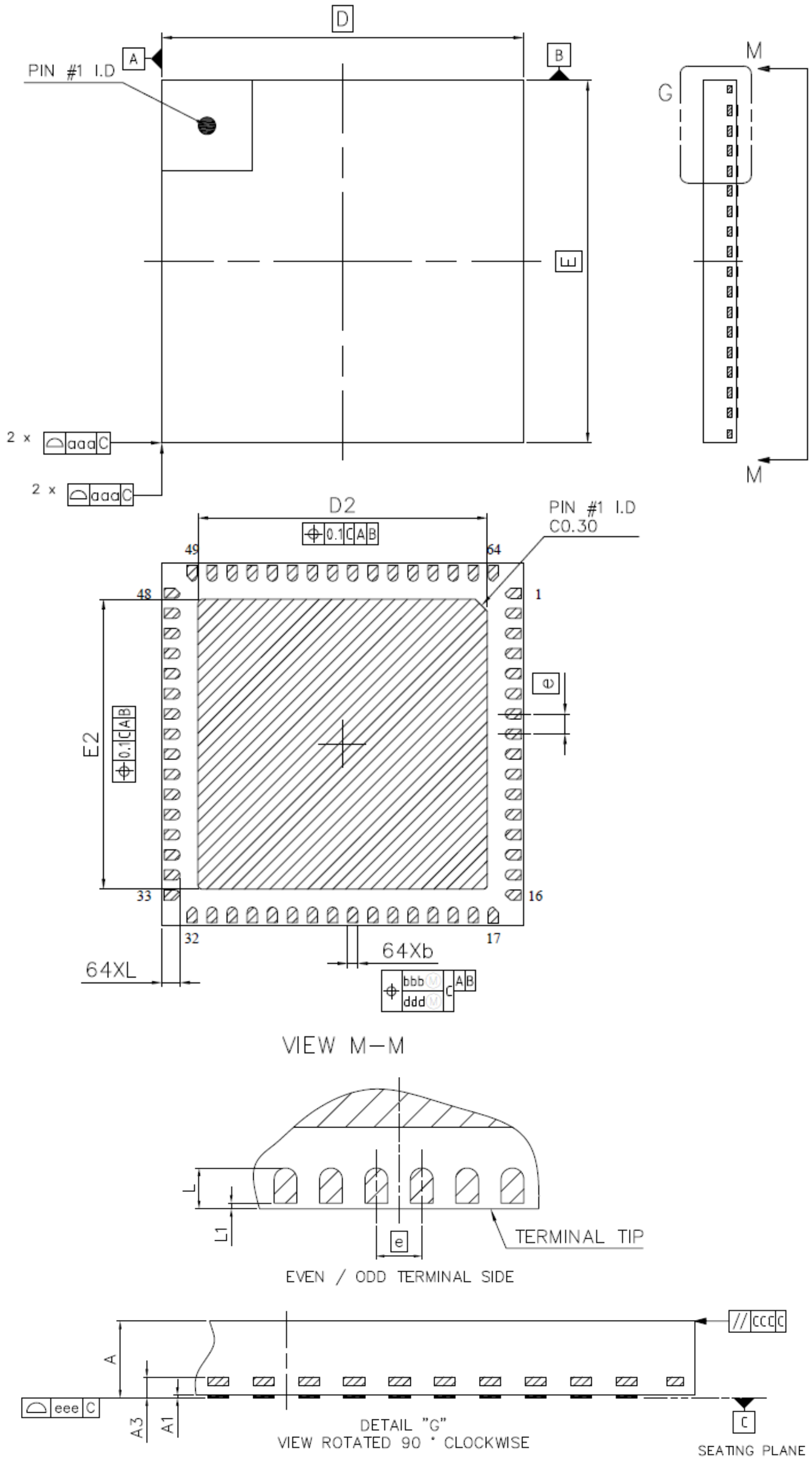

Figure 9.1. QFN64 Package Drawing

Table 9.2. QFN64 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.