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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b520f128iq48-ar

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3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	12C0
APORT	I2C1
-	IDAC
-	LCD

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.8	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V out- put, I_{DCDC_LOAD} = 10 mA	2.4	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I _{DCDC_LOAD} = 200 mA	2.6	_	V _{VREGVDD} MAX	V
Output voltage programma- ble range ¹	V _{DCDC_0}		1.8	_	V _{VREGVDD}	V
Regulation DC accuracy	ACC _{DC}	Low Noise (LN) mode, 1.8 V tar- get output	TBD		TBD	V
Regulation window ⁴	WIN _{REG}	Low Power (LP) mode, LPCMPBIASEMxx ³ = 0, 1.8 V tar- get output, I _{DCDC_LOAD} ≤ 75 µA	TBD	_	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx ³ = 3, 1.8 V tar- get output, I _{DCDC_LOAD} ≤ 10 mA	TBD	_	TBD	V
Steady-state output ripple	V _R		_	3	—	mVpp
Output voltage under/over- shoot	V _{OV}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	_	25	TBD	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	_	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions com- pared to DC level in LN mode	_	200	_	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	_	40	_	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode		100	_	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	_	0.1	_	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	_	0.1	—	%

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	_	0.75	—	μA
		128 byte RAM retention, CRYO- TIMER running from ULFRCO	—	0.37	_	μA
		128 byte RAM retention, no RTCC	_	0.37	_	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.05	—	μA
Current consumption of pe- ripheral power domain 1, with voltage scaling enabled	IPD1_VS	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ¹	_	0.18	_	μA
Current consumption of pe- ripheral power domain 2, with voltage scaling enabled	IPD2_VS	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ¹	_	0.18	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.

2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.8 Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
DVDD BOD threshold	V _{DVDDBOD}	DVDD rising	_	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	—	_	V
		DVDD falling (EM2/EM3)	TBD	_	_	V
DVDD BOD hysteresis	V _{DVDDBOD_HYST}		_	18	_	mV
DVDD BOD response time	tDVDDBOD_DELAY	Supply drops at 0.1V/µs rate	_	2.4	_	μs
AVDD BOD threshold	V _{AVDDBOD}	AVDD rising	_	_	TBD	V
		AVDD falling (EM0/EM1)	TBD		_	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	V _{AVDDBOD_HYST}		_	20	_	mV
AVDD BOD response time	t _{AVDDBOD_DELAY}	Supply drops at 0.1V/µs rate	_	2.4	_	μs
EM4 BOD threshold	V _{EM4DBOD}	AVDD rising	_	_	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V _{EM4BOD_HYST}		_	25	_	mV
EM4 BOD response time	t _{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	_	300	_	μs

Table 4.10. Brown Out Detector (BOD)

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Crystal frequency	f _{HFXO}		4	—	48	MHz
Supported crystal equivalent series resistance (ESR)	ESR _{HFXO}	48 MHz crystal	_	_	50	Ω
		24 MHz crystal	_	_	150	Ω
		4 MHz crystal	—	—	180	Ω
Supported range of crystal load capacitance ¹	C _{HFXO_CL}		TBD	_	TBD	pF
Nominal on-chip tuning cap range ²	C _{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	8.7	_	51.7	pF
On-chip tuning capacitance step	SS _{HFXO}		_	0.08		pF
Startup time	t _{HFXO}	48 MHz crystal, ESR = 50 Ohm, C_L = 8 pF	_	350		μs
		24 MHz crystal, ESR = 150 Ohm, C_L = 6 pF	_	700	—	μs
		4 MHz crystal, ESR = 180 Ohm, C_L = 18 pF	_	3	_	ms
Current consumption after	I _{HFXO}	48 MHz crystal	—	880	_	μA
startup		24 MHz crystal		420	_	μA
		4 MHz crystal	_	80		μA

Table 4.12. High-Frequency Crystal Oscillator (HFXO)

Note:

1. Total load capacitance as seen by the crystal.

2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.11 General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input low voltage	V _{IL}	GPIO pins	—	_	IOVDD*0.3	V
Input high voltage	V _{IH}	GPIO pins	IOVDD*0.7	_	—	V
Output high voltage relative to IOVDD	V _{OH}	Sourcing 3 mA, IOVDD \ge 3 V,	IOVDD*0.8		—	V
		DRIVESTRENGTH ¹ = WEAK				
		Sourcing 1.2 mA, IOVDD \ge 1.62 V,	IOVDD*0.6		_	V
		DRIVESTRENGTH ¹ = WEAK				
		Sourcing 20 mA, IOVDD ≥ 3 V,	IOVDD*0.8		—	V
		DRIVESTRENGTH ¹ = STRONG				
		Sourcing 8 mA, IOVDD ≥ 1.62 V,	IOVDD*0.6		—	V
		DRIVESTRENGTH ¹ = STRONG				
Output low voltage relative to	V _{OL}	Sinking 3 mA, IOVDD \ge 3 V,	_		IOVDD*0.2	V
IOVDD		DRIVESTRENGTH ¹ = WEAK				
		Sinking 1.2 mA, IOVDD \ge 1.62 V,	—		IOVDD*0.4	V
		DRIVESTRENGTH ¹ = WEAK				
		Sinking 20 mA, IOVDD ≥ 3 V,	—	_	IOVDD*0.2	V
		DRIVESTRENGTH ¹ = STRONG				
		Sinking 8 mA, IOVDD ≥ 1.62 V,	—		IOVDD*0.4	V
		DRIVESTRENGTH ¹ = STRONG				
Input leakage current	I _{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	_	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—		TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	_	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	I _{5VTOLLEAK}	IOVDD < GPIO ≤ IOVDD + 2 V	_	3.3	TBD	μA
I/O pin pull-up/pull-down re- sistor	R _{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses re- moved by the glitch suppres- sion filter	t _{IOGLITCH}		TBD	25	TBD	ns

Table 4.18. General-Purpose I/O (GPIO)

4.1.17 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{8 1}.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	_	3.8	V
		HCMDIS = 1	1.62		3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	_	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	_	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	_	_	MΩ
Output voltage	V _{OUT}		V _{VSS}		V _{OPA}	V
Load capacitance ²	C _{LOAD}	OUTSCALE = 0	_		75	pF
		OUTSCALE = 1	_	_	37.5	pF
Output impedance	R _{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V \leq V _{OUT} \leq V _{OPA} - 0.4 V, -8 mA $<$ I _{OUT} $<$ 8 mA, Buffer connection, Full supply range	_	0.25	_	Ω
		$\begin{array}{l} DRIVESTRENGTH = 0 \mbox{ or } 1, \ 0.4 \ V \\ \leq V_{OUT} \leq V_{OPA} \mbox{ - } 0.4 \ V, \ -400 \ \muA < \\ I_{OUT} < 400 \ \muA, \ Buffer \ connection, \\ Full \ supply \ range \end{array}$	_	0.6		Ω
		$\begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, \ 0.1 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} - 0.1 \text{ V}, \ -2 \text{ mA} < \\ I_{OUT} < 2 \text{ mA}, \ Buffer \ connection, \\ Full \ supply \ range \end{array}$		0.4	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V \leq V _{OUT} \leq V _{OPA} - 0.1 V, -100 µA $<$ I _{OUT} $<$ 100 µA, Buffer connection, Full supply range	_	1		Ω
Internal closed-loop gain	G _{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUT- SCALE = 0	—	580	_	μA
		DRIVESTRENGTH = 2, OUT- SCALE = 0	—	176	-	μA
		DRIVESTRENGTH = 1, OUT- SCALE = 0	—	13	-	μA
		DRIVESTRENGTH = 0, OUT- SCALE = 0	_	4.7	-	μA

Table 4.24. Operational Amplifier (OPAMP)



Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.



Figure 5.11. EFM32TG11B1xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 22 43	Digital IO power supply 0.
VSS	5 18 44	Ground	PC0	6	GPIO (5V)
PC1	7	GPIO (5V)	PC2	8	GPIO (5V)
PC3	9	GPIO (5V)	PC4	10	GPIO

GPIO Name	Pin Alternate Functionality / Description					
	Analog	Timers	Communication	Other		
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU- SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2		
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX		
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX		
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4		
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1		
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1		
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI		
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1		
PE9	BUSCY BUSDX LCD_SEG5					
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9		
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2		
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE- TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL- TEX6 PRS_CH1 #3		
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE- TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5		
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2			
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2			
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3			

Alternate	LOCATION				
Functionality	0 - 3	4 - 7	Description		
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.		
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.		
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.		
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.		
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.		
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.		
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.		
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is re- ceived, and has a built-in pull up when JTAG is active.		
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is re- ceived.		
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4		
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4		
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4		
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4		

Alternate	LOCA				
Functionality	0 - 3	4 - 7	Description		
LCD_SEG35	0: PC9		LCD segment line 35.		
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.		
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.		
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.		
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.		
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.		
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.		
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.		
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.		
LES_CH0	0: PC0		LESENSE channel 0.		
LES_CH1	0: PC1		LESENSE channel 1.		
LES_CH2	0: PC2		LESENSE channel 2.		
LES_CH3	0: PC3		LESENSE channel 3.		

Alternate	LOCATION				
Functionality	0 - 3	4 - 7	Description		
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.		
OPA3_OUT	0: PD1		Operational Amplifier 3 output.		
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.		
PCNT0_S0IN	0: PC13 2: PC0 3: PD6	4: PA0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.		
PCNT0_S1IN	0: PC14 2: PC1 3: PD7	4: PA1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.		
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.		
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.		
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.		
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.		
PRS_CH4	0: PC8 2: PF1		Peripheral Reflex System PRS, channel 4.		
PRS_CH5	0: PC9 2: PD6		Peripheral Reflex System PRS, channel 5.		
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.		
PRS_CH7	0: PB13 2: PE7		Peripheral Reflex System PRS, channel 7.		

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

Dimension	Min	Тур	Мах	
A	0.70	0.75	0.80	
A1	0.00	_	0.05	
b	0.20	0.25	0.30	
A3	0.203 REF			
D	9.00 BSC			
е	0.40 BSC			
E	9.00 BSC			
D2	7.10	7.20	7.30	
E2	7.10	7.20	7.30	
L	0.35	0.40	0.45	
ааа	0.10			
bbb	0.10			
ссс	0.10			
ddd	0.05			
еее	0.08			

Table 7.1. QFN80 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 TQFP64 PCB Land Pattern



Figure 8.2. TQFP64 PCB Land Pattern Drawing



Figure 10.3. TQFP48 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

11. QFN32 Package Specifications

11.1 QFN32 Package Dimensions

