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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (T _J)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b520f128iq64-ar

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3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

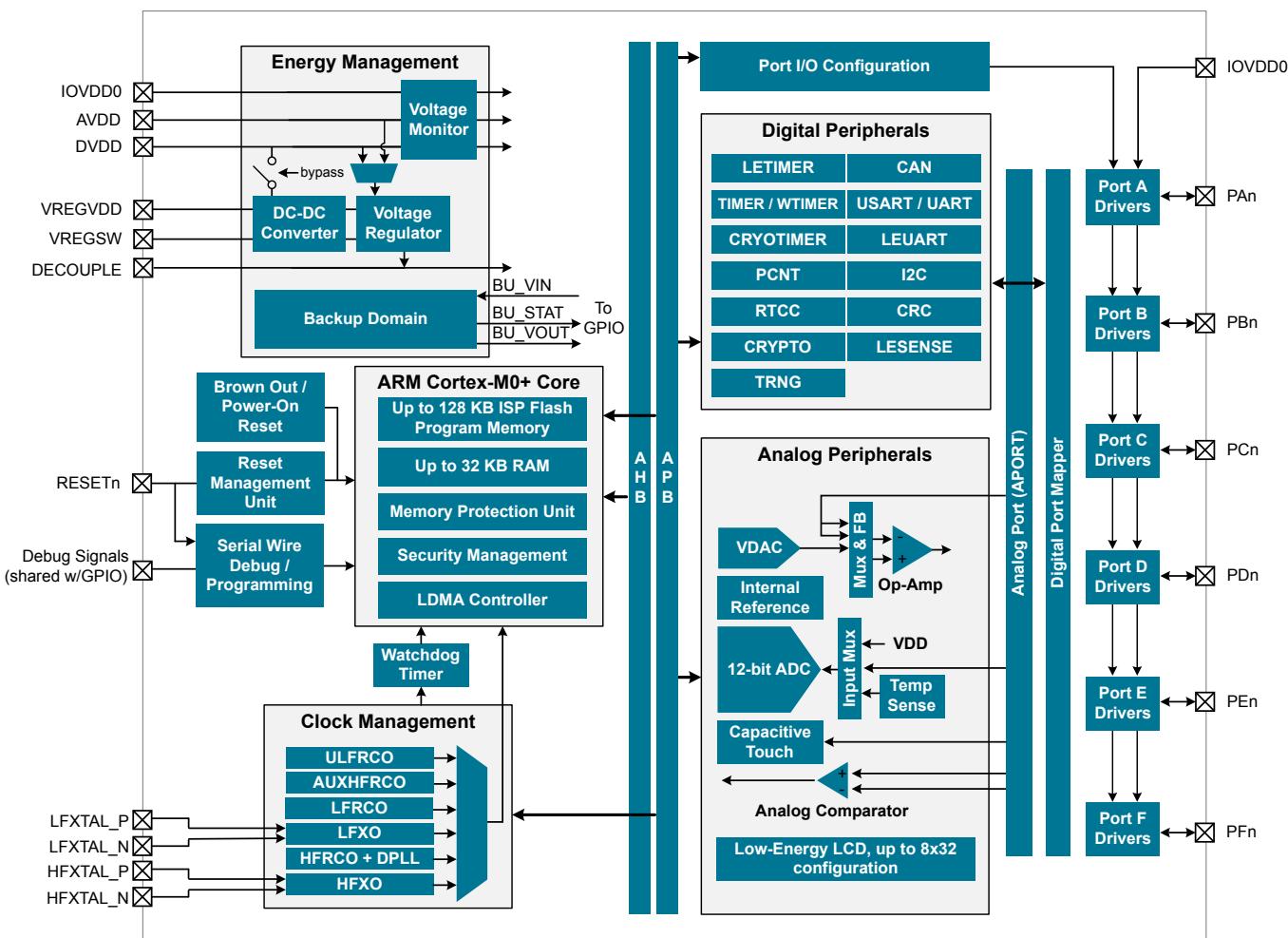


Figure 3.1. Detailed EFM32TG11 Block Diagram

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M0+ RISC processor
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Micro-Trace Buffer (MTB)
- Up to 128 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [Documentation] area.

4.1.7 Wake Up Times

Table 4.9. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Wake up time from EM1	t _{EM1_WU}		—	3	—	AHB Clocks	
Wake up from EM2	t _{EM2_WU}	Code execution from flash	—	10.1	—	μs	
		Code execution from RAM	—	3.1	—	μs	
Wake up from EM3	t _{EM3_WU}	Code execution from flash	—	10.1	—	μs	
		Code execution from RAM	—	3.1	—	μs	
Wake up from EM4H ¹	t _{EM4H_WU}	Executing from flash	—	88	—	μs	
Wake up from EM4S ¹	t _{EM4S_WU}	Executing from flash	—	282	—	μs	
Time from release of reset source to first instruction execution	t _{RESET}	Soft Pin Reset released	—	50	—	μs	
		Any other reset released	—	352	—	μs	
Power mode scaling time	t _{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2}	—	31.8	—	μs	
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ³	—	4.3	—	μs	
Note:							
1. Time from wake up request until first instruction is executed. Wakeup results in device reset.							
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).							
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.							
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.							

4.1.10 Flash Memory Characteristics⁵Table 4.17. Flash Memory Characteristics⁵

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—	—	cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	26	32	μs
		Single word	59	68	83	μs
Page erase time ⁴	t _{PERASE}		20	27	35	ms
Mass erase time ¹	t _{MERASE}		20	27	35	ms
Device erase time ^{2 3}	t _{DERASE}	T ≤ 85 °C	—	54	70	ms
		T ≤ 125 °C	—	54	75	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.0	mA
Write current ⁶	I _{WRITE}		—	—	3.5	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.16 Capacitive Sense (CSEN)

Table 4.23. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t _{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	—	μs
		Delta Modulation Conversion (single comparison)	—	1.55	—	μs
Maximum external capacitive load	C _{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R _{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WAR-MUPCNT=0	I _{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	25	—	nA
Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WAR-MUPCNT=0	I _{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹	—	57	—	nA

4.1.21.2 I2C Fast-mode (Fm)¹Table 4.29. I2C Fast-mode (Fm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	400	kHz
SCL clock low time	t _{LOW}		1.3	—	—	μs
SCL clock high time	t _{HIGH}		0.6	—	—	μs
SDA set-up time	t _{SU_DAT}		100	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t _{SU_STA}		0.6	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3	—	—	μs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

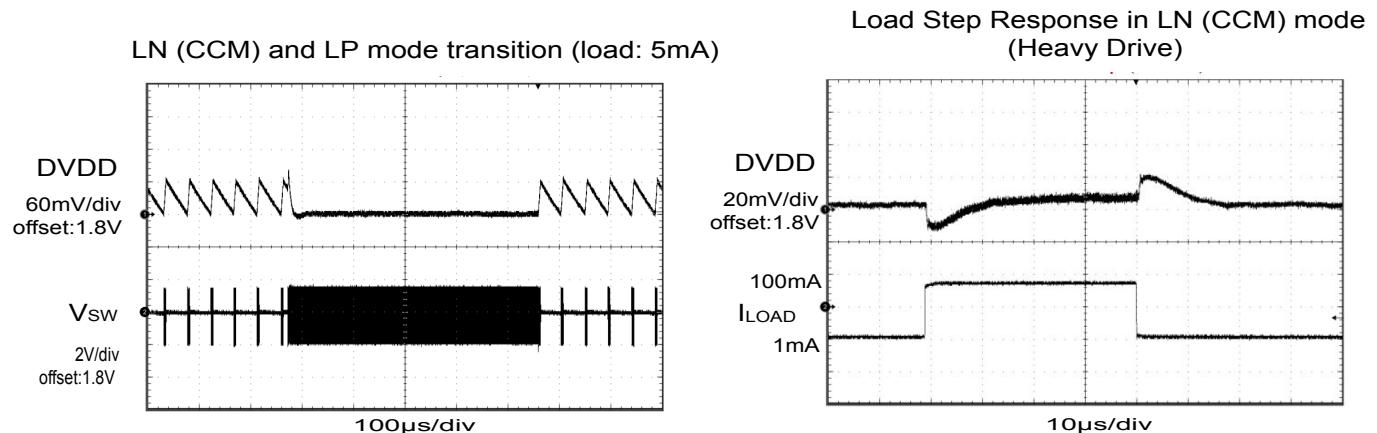


Figure 4.9. DC-DC Converter Transition Waveforms

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	9 24 51 70	Ground	PB3	10	GPIO
PB4	11	GPIO	PB5	12	GPIO
PB6	13	GPIO	PC1	14	GPIO (5V)
PC2	15	GPIO (5V)	PC3	16	GPIO (5V)
PC4	17	GPIO	PC5	18	GPIO
PB7	19	GPIO	PB8	20	GPIO
PA8	21	GPIO	PA9	22	GPIO
PA10	23	GPIO	PA12	25	GPIO
PA14	26	GPIO	RESETn	27	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	28	GPIO	PB12	29	GPIO
AVDD	30 34	Analog power supply.	PB13	31	GPIO
PB14	32	GPIO	PD0	35	GPIO (5V)
PD1	36	GPIO	PD3	37	GPIO
PD4	38	GPIO	PD5	39	GPIO
PD6	40	GPIO	PD7	41	GPIO
PD8	42	GPIO	PC6	43	GPIO
PC7	44	GPIO	VREGVSS	45	Voltage regulator VSS
VREGSW	46	DCDC regulator switching node	VREGVDD	47	Voltage regulator VDD input
DVDD	48	Digital power supply.	DECOPUPLE	49	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	52	GPIO	PE5	53	GPIO
PE6	54	GPIO	PE7	55	GPIO
PC8	56	GPIO	PC9	57	GPIO
PC10	58	GPIO (5V)	PC11	59	GPIO (5V)
PC13	60	GPIO (5V)	PC14	61	GPIO (5V)
PC15	62	GPIO (5V)	PF0	63	GPIO (5V)
PF1	64	GPIO (5V)	PF2	65	GPIO
PF3	66	GPIO	PF4	67	GPIO
PF5	68	GPIO	PE8	71	GPIO
PE9	72	GPIO	PE10	73	GPIO
PE11	74	GPIO	BODEN	75	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE12	76	GPIO	PE13	77	GPIO
PE14	78	GPIO	PE15	79	GPIO
PA15	80	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.2 EFM32TG11B5xx in QFN80 Device Pinout

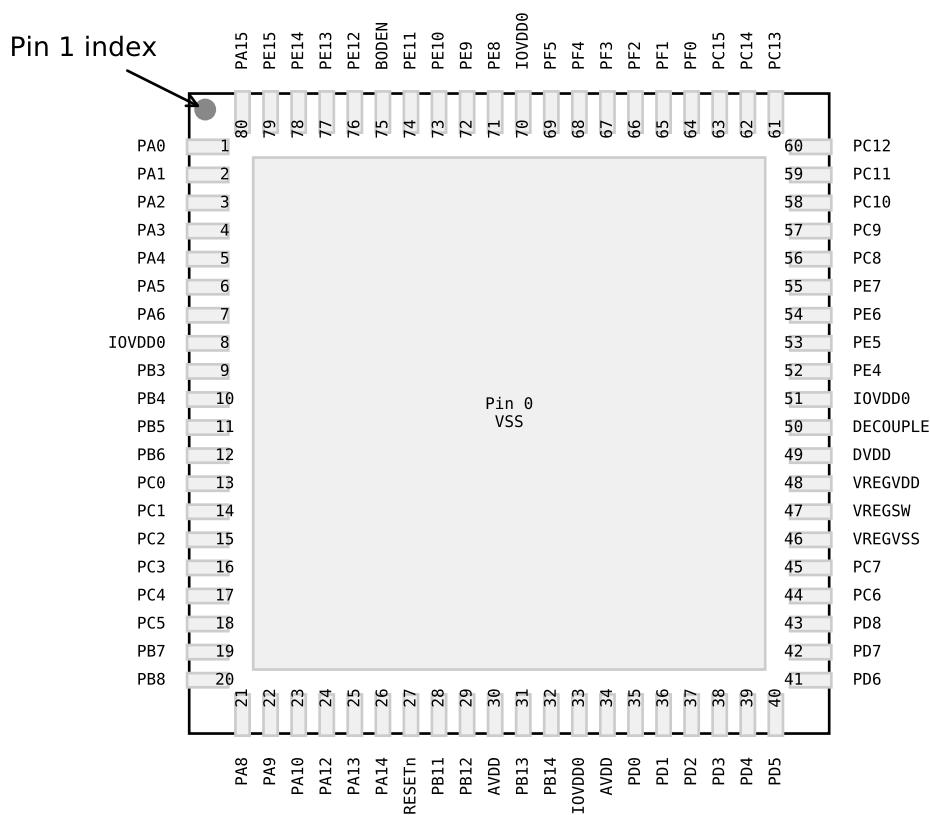


Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.2. EFM32TG11B5xx in QFN80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO
PA8	21		PA9	22	
PA10	23		PA11	24	
PA12	25		PA13	26	
PA14	27		PA15	28	
RESETn	29		PE15	29	
PB11	30		PE14	31	
AVDD	32		PE13	32	
PB12	33		PE12	33	
PB13	34		PE11	34	
PB14	35		PE10	35	
IOVDD0	36		PE9	36	
AVDD	37		PE8	37	
PD0	38		PE7	38	
PD1	39		PE6	39	
PD2	40		PE5	40	
PD3			PE4		
PD4			PE3		
PD5			PE2		
			PE1		
			PF0		
			PC15		
			PC14		
			PC13		
			PC12		
			PC11		
			PC10		
			PC9		
			PC8		
			PE7		
			PE6		
			PE5		
			PE4		
			IOVDD0		
			DECOPPLE		
			DVDD		
			VREGVDD		
			VREGSW		
			VREGVSS		
			PC7		
			PC6		
			PD8		
			PD7		
			PD6		

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOPUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB7	11	GPIO	PB8	12	GPIO
PA8	13	GPIO	PA9	14	GPIO
PA10	15	GPIO	RESETn	16	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	17	GPIO	AVDD	19 23	Analog power supply.
PB13	20	GPIO	PB14	21	GPIO
PD4	24	GPIO	PD5	25	GPIO
PD6	26	GPIO	PD7	27	GPIO
DVDD	28	Digital power supply.	DECOPPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC8	30	GPIO	PC9	31	GPIO
PC10	32	GPIO (5V)	PC11	33	GPIO (5V)
PC13	34	GPIO (5V)	PC14	35	GPIO (5V)
PC15	36	GPIO (5V)	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PC4		LCD segment line 24.
LCD_SEG25	0: PC5		LCD segment line 25.
LCD_SEG26	0: PA9		LCD segment line 26.
LCD_SEG27	0: PA10		LCD segment line 27.
LCD_SEG28	0: PB11		LCD segment line 28.
LCD_SEG29	0: PB12		LCD segment line 29.
LCD_SEG30	0: PD3		LCD segment line 30.
LCD_SEG31	0: PD4		LCD segment line 31.
LCD_SEG32	0: PC6		LCD segment line 32.
LCD_SEG33	0: PC7		LCD segment line 33.
LCD_SEG34	0: PC8		LCD segment line 34.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM0_CC0	0: PA0 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 2: PD3 3: PC1	4: PF2 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 3: PB7	4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 3: PB8	4: PD7 5: PF3	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 3: PB11	4: PC13 5: PF4	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 6: PF5	Timer 1 Capture Compare input / output channel 3.
U0_CTS	2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 5.18. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC0Y	BUSADC0X	Bus
										CH31
				PB14			PB14			CH30
				PB13	PB13	PB12				CH29
				PB12		PB11				CH28
				PB11						CH27
										CH26
										CH25
										CH24
										CH23
				PB6		PB6				CH22
PF4	PF5	PF5	PF4	PF4	PF4	PB5	PB5	PB4	PB4	CH21
PF2	PF3	PF3	PF2	PF2	PF2	PB3	PB3	PB3	PB3	CH20
PF0	PF1	PF1	PF1	PF0	PF0					CH19
PE15	PE15	PE15	PE14	PE14	PE14	PA15	PA15	PA14	PA14	CH18
PE14	PE13	PE13	PE13	PE12	PE12	PA13	PA13	PA13	PA13	CH17
PE12	PE11	PE11	PE11	PE10	PE10	PA10	PA10	PA10	PA10	CH16
PE10	PE9	PE9	PE9	PE8	PE8	PA9	PA9	PA9	PA9	CH15
PE8	PE7	PE7	PE7	PE6	PE6	PA6	PA6	PA6	PA6	CH14
PE6	PE5	PE5	PE5	PE4	PE4	PA5	PA5	PA5	PA5	CH13
PE4						PA3	PA3	PA3	PA3	CH12
						PA2	PA2	PA2	PA2	CH11
						PA1	PA1	PA1	PA1	CH10
						PA0	PA0	PA0	PA0	CH9
										CH8
										CH7
								PD7	PD7	PD7
								PD6	PD6	PD6
								PD5	PD5	PD5
								PD4	PD4	PD4
								PD3	PD3	PD3
								PD2	PD2	PD2
								PD1	PD1	PD1
								PD0	PD0	PD0

APORT4Y	APORT3Y	APORT2Y	APORT1Y	APORT14X	APORT3X	APORT2X	APORT1X	APORT4Y	APORT3Y	APORT2Y	APORT1Y	Port
BUSDY	BUSCY	BUSBY	BUSAY	BUSDX	BUSCX	BUSBX	BUSAX	BUSDY	BUSCY	BUSBY	BUSAY	Bus
												CH31
		PB14			PB14					PB14		CH30
		PB13		PB13		PB12			PB12		PB13	CH29
	PB12	PB11		PB11					PB11		PB14	CH28
												CH27
												CH26
												CH25
												CH24
												CH23
												CH22
		PB6		PB6		PB5		PB6		PB6		CH21
	PF5	PB5		PF5		PB4		PF5		PF5		CH20
PF4	PB4	PF4		PF4		PB3		PF3		PF3		CH19
PF3	PB3	PF3		PF3		PF2		PF2		PF2		CH18
PF2		PF1		PF1		PF0		PF0		PF1		CH17
PF0						PA15		PE15		PE15		CH16
PE15	PA15	PE15		PE15		PA14		PA14		PA14		CH15
PE14	PA14	PE14		PE14		PA13		PE13		PA13		CH14
PE13	PA13	PE13		PE13		PE12		PE12		PE12		CH13
PE12		PE12				PE11		PE11		PE11		CH12
PE11						PA10		PA10		PA10		CH11
PE10	PA10	PE10		PE10		PA9		PE9		PE9		CH10
PE9	PA9	PE9		PE9		PE8		PE8		PE8		CH9
PE8		PE8				PE7		PE7		PE7		CH8
PE7						PE6		PA6		PA6		CH7
PE6	PA6	PE6		PE6		PA5		PE5		PE5		CH6
PE5	PA5	PE5		PE5		PA4		PE4		PE4		CH5
PE4	PA4	PE4		PE4		PA3		PA3		PA3		CH4
						PA2		PA2		PA2		CH3
						PA1		PA1		PA1		CH2
						PA0		PA0		PA0		CH1
												CH0

APORT4Y	APORT3Y	APORT2Y	APORT1Y		APORT1X	APORT3X	APORT2X	APORT1X		APORT4Y	APORT3Y	APORT2Y	APORT1Y	Port
BUSDY	BUSCY	BUSBY	BUSAY		BUSDX	BUSCX	BUSBX	BUSAX		BUSDY	BUSCY	BUSBY	BUSAY	Bus
														CH31
		PB14					PB14							CH30
		PB13				PB13								CH29
	PB12					PB12								CH28
	PB11					PB11								CH27
														CH26
														CH25
														CH24
														CH23
														CH22
							PB6							CH21
	PB5				PB5		PB5							CH20
PF4		PB4			PF5		PB4							CH19
	PF3		PB3		PF3		PB3							CH18
PF2					PF2									CH17
PF0		PF1			PF1									CH16
					PF0									CH15
	PE15		PA15		PE15		PA15							PA15
PE14		PA14			PE14		PA14							PA14
	PE13		PA13		PE13		PA13							PA13
PE12					PE12									CH13
PE11					PE11									CH12
PE10		PA10			PE10		PA10							CH11
PE9					PE9		PA9							CH10
PE8					PE8									CH9
	PE7				PE7									CH8
PE6		PA6			PE6		PA6							CH7
	PE5		PA5		PE5		PA5							CH6
PE4		PA4			PE4		PA4							CH5
							PA3							CH4
							PA2							CH3
							PA1							CH2
							PA0							CH1
								PA0						CH0

6.2 TQFP80 PCB Land Pattern

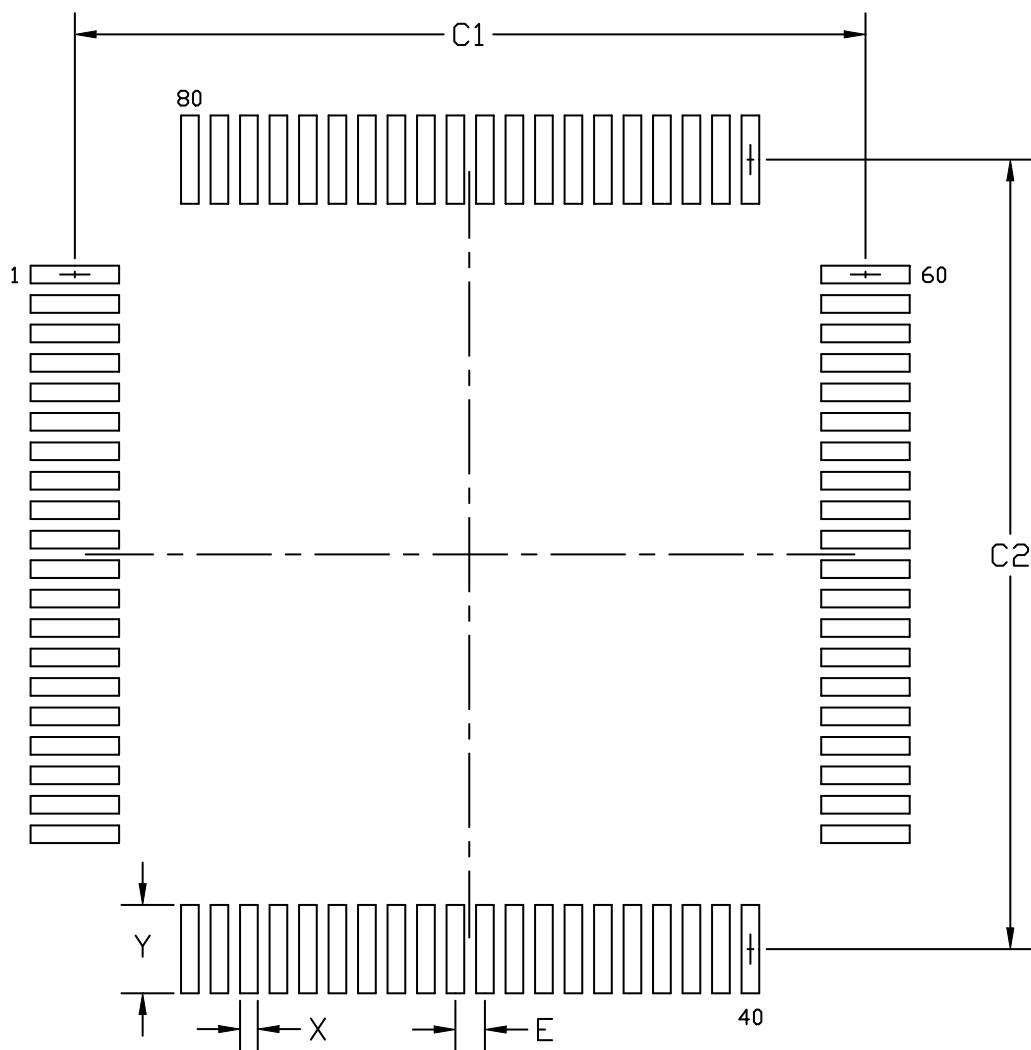


Figure 6.2. TQFP80 PCB Land Pattern Drawing