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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-WFQFN Exposed Pad
Supplier Device Package	80-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64gm80-a

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Table of Contents

1.	Feature List	. 2
2.	Ordering Information	. 4
3.	System Overview	10
	3.1 Introduction	.10
	3.2 Power	.11
	3.2.1 Energy Management Unit (EMU)	.11
	3.2.2 DC-DC Converter	.11
	3.2.3 EM2 and EM3 Power Domains	.11
	3.3 General Purpose Input/Output (GPIO).	.12
	3.4 Clocking	.12
	3.4.1 Clock Management Unit (CMU)	.12
	3.4.2 Internal and External Oscillators.	.12
	3.5 Counters/Timers and PWM	.12
	3.5.1 Timer/Counter (TIMER)	.12
	3.5.2 Wide Timer/Counter (WTIMER)	.12
	3.5.3 Real Time Counter and Calendar (RTCC)	. IZ
	3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)	13
	3.5.6 Pulse Counter (PCNT)	.13
	3.5.7 Watchdog Timer (WDOG).	.13
	3.6 Communications and Other Digital Peripherals	.13
	3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART).	.13
	3.6.2 Universal Asynchronous Receiver/Transmitter (UART)	.13
	3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)	.13
	3.6.4 Inter-Integrated Circuit Interface (I ² C)	.13
	3.6.5 Controller Area Network (CAN)	.14
	3.6.6 Peripheral Reflex System (PRS)	.14
	3.6.7 Low Energy Sensor Interface (LESENSE)	.14
	3.7 Security Features.	.14
	3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)	.14
	3.7.2 Crypto Accelerator (CRYPTO)	.14
	3.7.3 True Random Number Generator (TRNG)	.14
		. 14
	3.8 Analog	.14
	3.8.1 Analog Poll (APORT)	.15
	3.8.3 Analog to Digital Converter (ADC)	.15
	3.8.4 Capacitive Sense (CSEN).	.15
	3.8.5 Digital to Analog Converter (VDAC)	.15
	3.8.6 Operational Amplifiers	.15
	3.8.7 Liquid Crystal Display Driver (LCD)	.15
	3.9 Reset Management Unit (RMU)	.15

3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	12C0
APORT	I2C1
-	IDAC
-	LCD

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

4.1.14 Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V _{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	—	—	V _{ACMPVDD}	V
Supply voltage	VACMPVDD	$BIASPROG^4 \le 0x10 \text{ or } FULL-BIAS^4 = 0$	1.8	—	V _{VREGVDD} MAX	V
		$0x10 < BIASPROG^4 \le 0x20$ and FULLBIAS ⁴ = 1	2.1	_	V _{VREGVDD} MAX	V
Active current not including voltage reference ²	IACMP	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	—	50	_	nA
		$BIASPROG^4 = 0x10, FULLBIAS^4 = 0$		306	_	nA
		$BIASPROG^4 = 0x02, FULLBIAS^4$ $= 1$	_	6.5	_	μA
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	_	74	TBD	μA
Current consumption of inter- nal voltage reference ²	IACMPREF	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	_	50	_	nA
		VLP selected as input using VDD	—	20	_	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	_	μA
		VADIV selected as input using VDD/1		2.4	_	μA

Table 4.21. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current, continuous conversions, WARMUP- MODE=KEEPCSENWARM	ICSEN_ACTIVE	SAR or Delta Modulation conver- sions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on		90.5		μA
HFPERCLK supply current	ICSEN_HFPERCLK	Current contribution from HFPERCLK when clock to CSEN block is enabled.	_	2.25	_	µA/MHz

Note:

 Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.17 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{8 1}.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	_	3.8	V
		HCMDIS = 1	1.62		3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	_	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	_	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	_	_	MΩ
Output voltage	V _{OUT}		V _{VSS}		V _{OPA}	V
Load capacitance ²	C _{LOAD}	OUTSCALE = 0	_		75	pF
		OUTSCALE = 1	_	_	37.5	pF
Output impedance	R _{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V \leq V _{OUT} \leq V _{OPA} - 0.4 V, -8 mA $<$ I _{OUT} $<$ 8 mA, Buffer connection, Full supply range	_	0.25	_	Ω
		$\begin{array}{l} DRIVESTRENGTH = 0 \mbox{ or } 1, \ 0.4 \ V \\ \leq V_{OUT} \leq V_{OPA} \mbox{ - } 0.4 \ V, \ -400 \ \muA < \\ I_{OUT} < 400 \ \muA, \ Buffer \ connection, \\ Full \ supply \ range \end{array}$	_	0.6		Ω
		$\begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, \ 0.1 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} - 0.1 \text{ V}, \ -2 \text{ mA} < \\ I_{OUT} < 2 \text{ mA}, \ Buffer \ connection, \\ Full \ supply \ range \end{array}$		0.4	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V \leq V _{OUT} \leq V _{OPA} - 0.1 V, -100 µA $<$ I _{OUT} $<$ 100 µA, Buffer connection, Full supply range	_	1		Ω
Internal closed-loop gain	G _{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUT- SCALE = 0	—	580	_	μA
		DRIVESTRENGTH = 2, OUT- SCALE = 0	—	176	-	μA
		DRIVESTRENGTH = 1, OUT- SCALE = 0	—	13	-	μA
		DRIVESTRENGTH = 0, OUT- SCALE = 0	_	4.7	-	μA

Table 4.24. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Slew rate ⁵	SR	DRIVESTRENGTH = 3, INCBW=1 ³	_	4.7	_	V/µs
		DRIVESTRENGTH = 3, INCBW=0	_	1.5	_	V/µs
		DRIVESTRENGTH = 2, INCBW=1 ³	_	1.27	_	V/µs
		DRIVESTRENGTH = 2, INCBW=0	_	0.42		V/µs
		DRIVESTRENGTH = 1, INCBW=1 ³	_	0.17	_	V/µs
		DRIVESTRENGTH = 1, INCBW=0	_	0.058		V/µs
		DRIVESTRENGTH = 0, INCBW=1 ³	_	0.044	_	V/µs
		DRIVESTRENGTH = 0, INCBW=0	_	0.015	_	V/µs
Startup time ⁶	T _{START}	DRIVESTRENGTH = 2	_	_	TBD	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	_	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	_	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	_	TBD	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	_	70	_	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	_	70	_	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90	_	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90		dB

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:					

1. GPIO with 5V tolerance are indicated by (5V).

5.15 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.14 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Alternate	LOCATION				
Functionality	0 - 3	4 - 7	Description		
ACMP0_O	0: PE13 2: PD6 3: PB11	4: PA6 7: PB3	Analog comparator ACMP0, digital output.		
ACMP1_O	0: PF2 2: PD7 3: PA12	4: PA14 7: PA5	Analog comparator ACMP1, digital output.		
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.		
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.		
BOOT_RX	0: PF1		Bootloader RX.		
BOOT_TX	0: PF0		Bootloader TX.		
BU_STAT	0: PA8		Backup Power Domain status, whether or not the system is in backup mode.		
BU_VIN	0: PD8		Battery input for Backup Power Domain.		
BU_VOUT	0: PA12		Power output for Backup Power Domain.		
CAN0_RX	0: PC0 1: PF0 2: PD0		CAN0 RX.		

Table 5.15. Alternate Functionality Overview

Alternate	LOCATION		LOCATION		
Functionality	0 - 3	4 - 7	Description		
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.		
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.		
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.		
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.		
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.		
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.		
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.		
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is re- ceived, and has a built-in pull up when JTAG is active.		
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is re- ceived.		
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4		
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4		
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4		
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4		

Alternate	LOCA	ATION	
Functionality	0 - 3	4 - 7	Description
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8	Low Energy Timer LETIM0, output channel 0.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 5.17. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	СНЗС	CH26	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH16	CH18	CH17	CH16	CH1	CH14	CH13	CH12	CH11	CH10	сн9	CH8	CH7	9HC	CH5	CH4	СНЗ	CH2	CH1	СНО
CE	хт																																
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
CE	хт_	SEN	ISE																														
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 5.19. CSEN Bus and Pin Mapping

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
ОР	A1_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
OP	PA1_	<u></u> P																															
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
OP	A2_	N																															
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
VD	AC	0_0	UT1	/ 0	PA1	_οι	JT																										
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Dimension	Min	Тур	Мах										
A	_	1.15	1.20										
A1	0.05	—	0.15										
A2	0.95	1.00	1.05										
b	0.17	0.22	0.27										
b1	0.17	0.20	0.23										
С	0.09	—	0.20										
c1	0.09	—	0.16										
D	12.00 BSC												
D1	10.00 BSC												
е		0.50 BSC											
E	12.00 BSC												
E1	10.00 BSC												
L	0.45	0.60	0.75										
L1		1.00 REF											
R1	0.08	_	_										
R2	0.08	_	0.20										
S	0.20	_	_										
θ	0	3.5	7										
Θ1	0	_	0.10										
Θ2	11	12	13										
θ3	11	12	13										

Table 8.1. TQFP64 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions



10.2 TQFP48 PCB Land Pattern



Figure 10.2. TQFP48 PCB Land Pattern Drawing

 Table 10.2.
 TQFP48 PCB Land Pattern Dimensions

Тур
8.50
8.50
0.50
0.30
1.60

Note:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.
- 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
- 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. QFN32 Package Specifications

11.1 QFN32 Package Dimensions

