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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64gq48-a

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

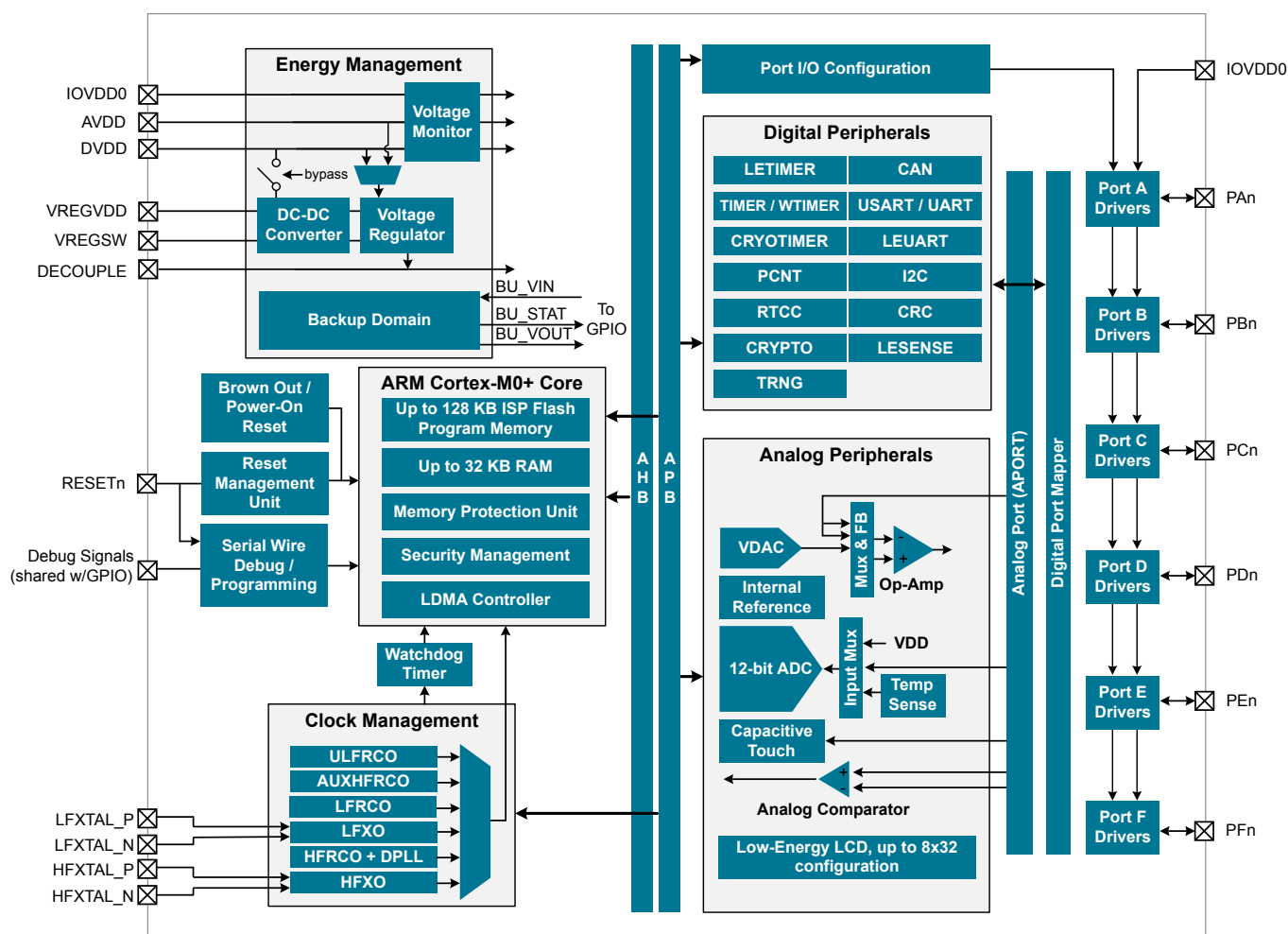


Figure 3.1. Detailed EFM32TG11 Block Diagram

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range ⁶	T _A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage ²	V _{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage ^{2 1}	V _{VREGVDD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	I _{VREGVDD}	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
DVDD operating supply voltage	V _{DVDD}		1.62	—	V _{VREGVDD}	V
IOVDD operating supply voltage	V _{IOVDD}	All IOVDD pins ⁵	1.62	—	V _{VREGVDD}	V
DECOUPLE output capacitor ^{3 4}	C _{DECOUPLE}		0.75	1.0	2.75	μF
HFCORECLK frequency	f _{CORE}	VSCALE2, MODE = WS1	—	—	48	MHz
		VSCALE2, MODE = WS0	—	—	25	MHz
		VSCALE0, MODE = WS1	—	—	20	MHz
		VSCALE0, MODE = WS0	—	—	10	MHz
HFCLK frequency	f _{HFCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	f _{HFSRCCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	f _{HFBUSCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	f _{HFPERCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	f _{HFPERBCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	f _{HFPERCCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V _{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R _{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT ²	R _{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I _{BU_VIN}	BU_VIN not powering backup domain	—	10	TBD	nA
		BU_VIN powering backup domain ¹	—	450	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.

2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.82	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.45	—	μA
		128 byte RAM retention, no RTCC	—	0.45	TBD	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.07	TBD	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I _{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ¹	—	0.18	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I _{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ¹	—	0.18	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.3 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.7 Wake Up Times

Table 4.9. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.1	—	μs
		Code execution from RAM	—	3.1	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.1	—	μs
		Code execution from RAM	—	3.1	—	μs
Wake up from EM4H ¹	t_{EM4H_WU}	Executing from flash	—	88	—	μs
Wake up from EM4S ¹	t_{EM4S_WU}	Executing from flash	—	282	—	μs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	50	—	μs
		Any other reset released	—	352	—	μs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2}	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ³	—	4.3	—	μs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/ μs for approximately 20 μs . During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none"> 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 3. ± 100 mV differential drive. 4. In ACMPn_CTRL register. 5. In ACMPn_HYSTERESIS registers. 6. In ACMPn_INPUTSEL register. 						

5. Pin Definitions

5.1 EFM32TG11B5xx in QFP80 Device Pinout

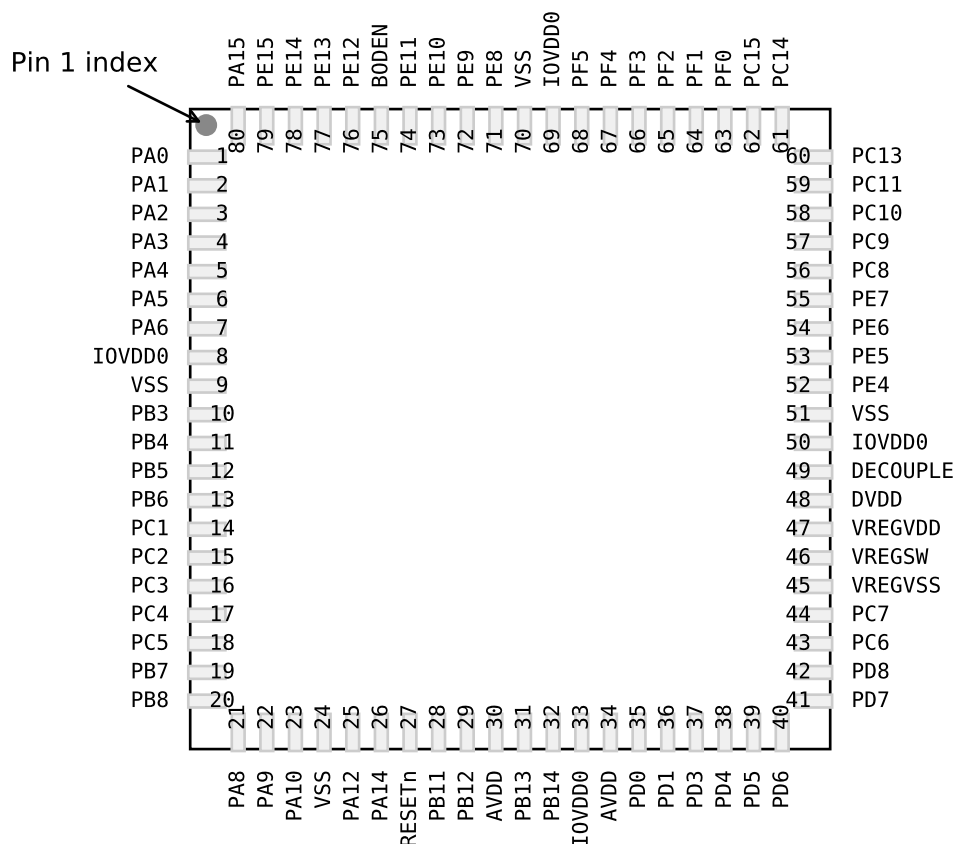


Figure 5.1. EFM32TG11B5xx in QFP80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.1. EFM32TG11B5xx in QFP80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 33 50 69	Digital IO power supply 0.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE12	76	GPIO	PE13	77	GPIO
PE14	78	GPIO	PE15	79	GPIO
PA15	80	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	79	GPIO	PA15	80	GPIO
Note: 1. GPIO with 5V tolerance are indicated by (5V).					

5.4 EFM32TG11B3xx in QFP64 Device Pinout

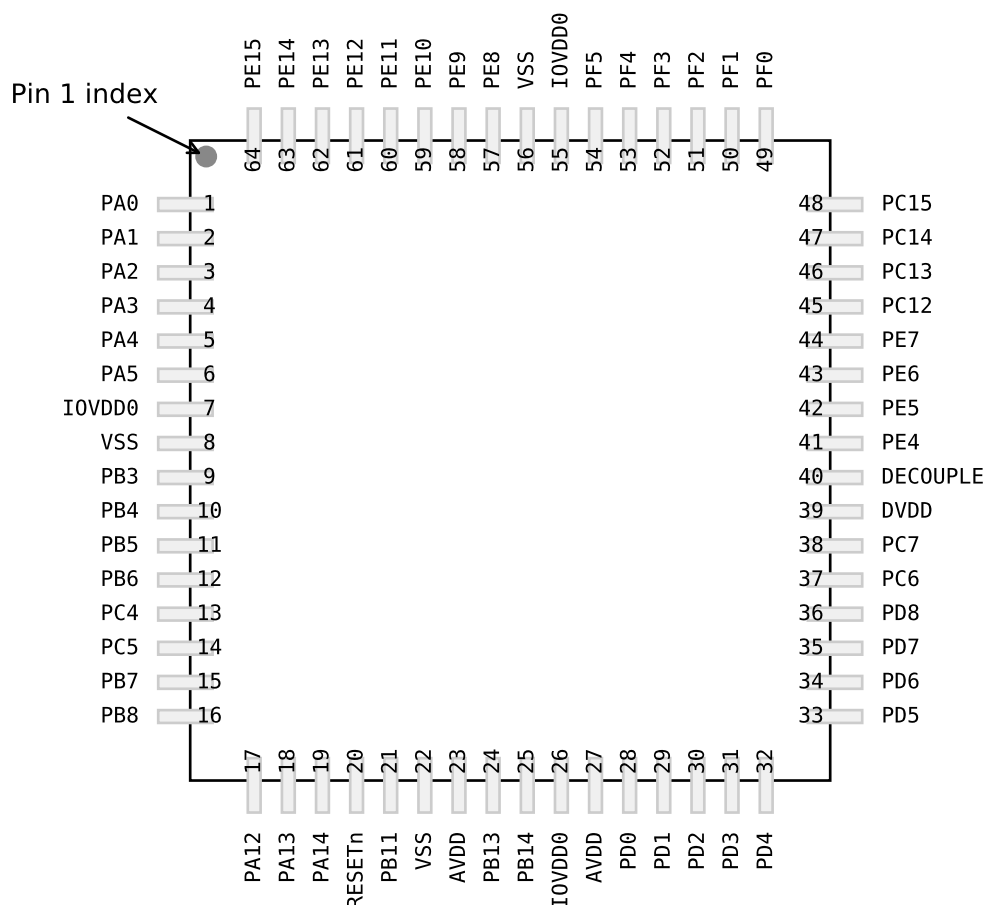


Figure 5.4. EFM32TG11B3xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.4. EFM32TG11B3xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.12 EFM32TG11B5xx in QFN32 Device Pinout

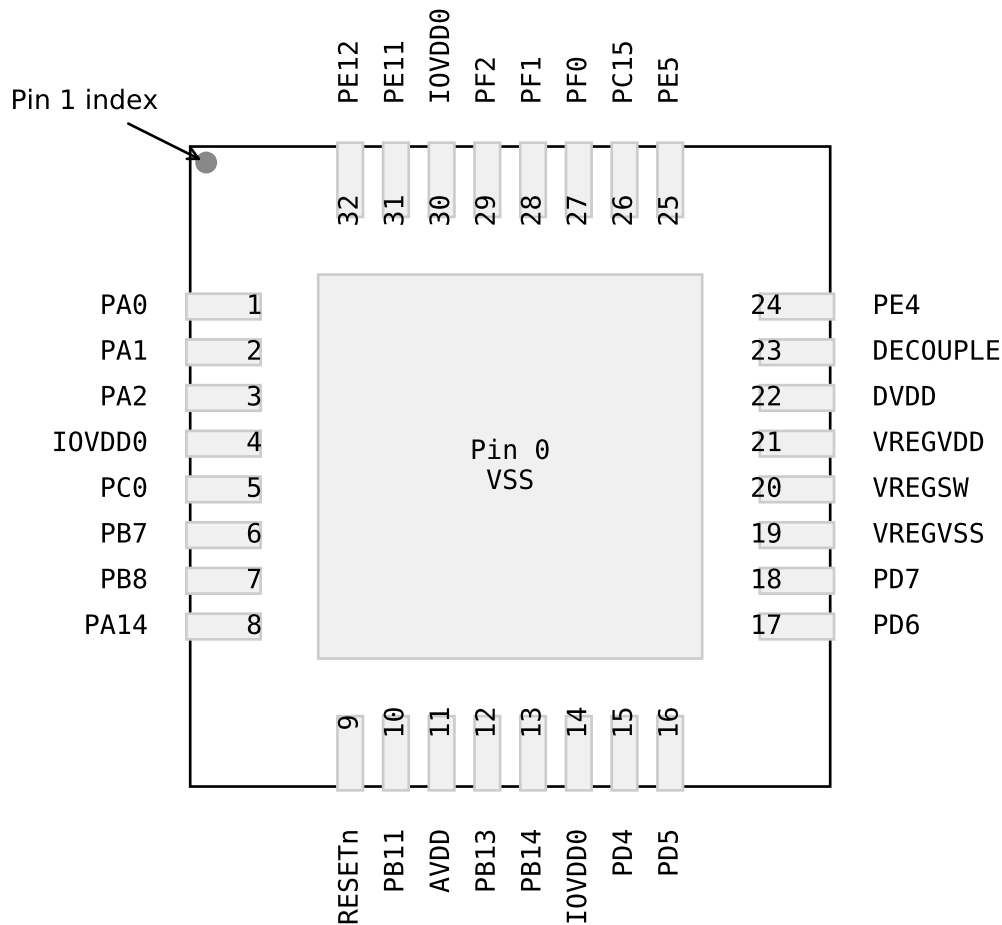


Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.14 GPIO Functionality Table](#) or [5.15 Alternate Functionality Overview](#).

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BU- SACMP1Y BUSACMP1X	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 LEU0_RX #5	LES_CH15 PRS_CH1 #2
PF0	BUSDY BUSCX	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	CAN0_RX #1 US1_CLK #2 US2_TX #5 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLKTCK BOOT_TX
PF1	BUSCY BUSDX	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US1_CS #2 US2_RX #5 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PF2	BUSDY BUSCX LCD_SEG0	TIM0_CC2 #4 TIM1_CC0 #5	CAN0_TX #1 US1_TX #5 US2_CLK #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO GPIO_EM4WU4
PF3	BUSCY BUSDX LCD_SEG1	TIM0_CDTI0 #2 TIM1_CC1 #5	US1_CTS #2	CMU_CLK1 #4 PRS_CH0 #1
PF4	BUSDY BUSCX LCD_SEG2	TIM0_CDTI1 #2 TIM1_CC2 #5	US1_RTS #2	PRS_CH1 #1
PF5	BUSCY BUSDX LCD_SEG3	TIM0_CDTI2 #2 TIM1_CC3 #6	US2_CS #5	PRS_CH2 #1 DBG_TDI
PE8	BUSDY BUSCX LCD_SEG4			PRS_CH3 #1
PE9	BUSCY BUSDX LCD_SEG5			
PE10	BUSDY BUSCX LCD_SEG6	TIM1_CC0 #1 WTIM0_CDTI0 #0	US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE11	BUSCY BUSDX LCD_SEG7	TIM1_CC1 #1 WTIM0_CDTI1 #0	US0_RX #0	LES_ALTEX5 PRS_CH3 #2
PE12	BUSDY BUSCX LCD_SEG8	TIM1_CC2 #1 WTIM0_CDTI2 #0 LE- TIM0_OUT0 #4	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_AL- TEX6 PRS_CH1 #3
PE13	BUSCY BUSDX LCD_SEG9	TIM1_CC3 #1 LE- TIM0_OUT1 #4	US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 GPIO_EM4WU5
PE14	BUSDY BUSCX LCD_SEG10		US0_CTS #0 LEU0_TX #2	
PE15	BUSCY BUSDX LCD_SEG11		US0_RTS #0 LEU0_RX #2	
PA15	BUSAY BUSBX LCD_SEG12		US2_CLK #3	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
CAN0_TX	0: PC1 1: PF2 2: PD1		CAN0 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6	4: PA3	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.
LCD_SEG7	0: PE11		LCD segment line 7.
LCD_SEG8	0: PE12		LCD segment line 8.

9.2 QFN64 PCB Land Pattern

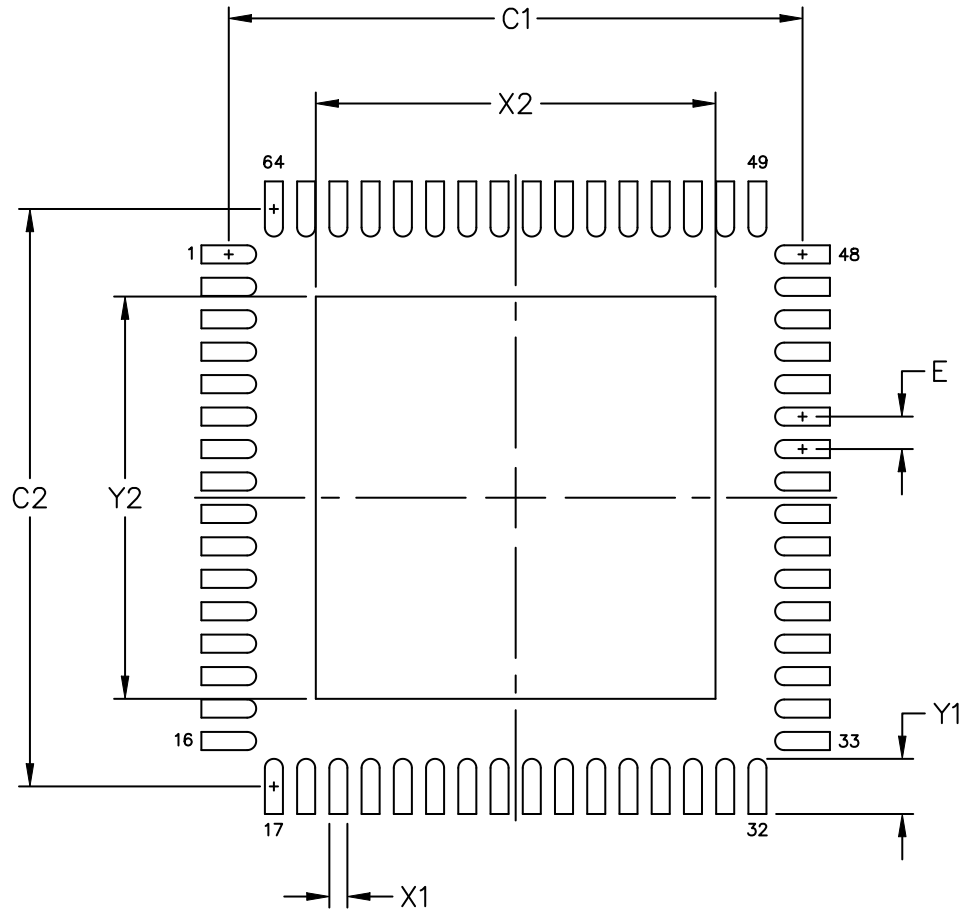


Figure 9.2. QFN64 PCB Land Pattern Drawing

9.3 QFN64 Package Marking



Figure 9.3. QFN64 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

Table 11.1. QFN32 Package Dimensions

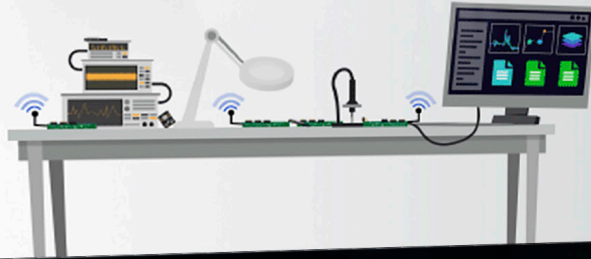
Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	5.0 BSC		
D2/E2	3.60	3.70	3.80
E	5.0 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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