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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64gq64-ar

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2. Ordering Information

Table 2.1. Ordering Information

	Floob	DAM	DC-DC				
Ordering Code	(kB)	(kB)	verter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

4.1.6.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_DCM	48 MHz crystal, CPU running while loop from flash	—	38	_	µA/MHz
DCM mode ²		48 MHz HFRCO, CPU running while loop from flash	_	37	_	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	_	45	_	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	—	53	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	43	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	47	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	61	_	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	587	_	µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_CCM	48 MHz crystal, CPU running while loop from flash	—	49	_	µA/MHz
abled, DCDC in Low Noise CCM mode ¹		48 MHz HFRCO, CPU running while loop from flash	_	48	_	µA/MHz
		48 MHz HFRCO, CPU running Prime from flash	_	55	—	µA/MHz
		48 MHz HFRCO, CPU running CoreMark loop from flash	_	63	_	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	_	60	_	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	68	_	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	96	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1157	—	µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_LPM	32 MHz HFRCO, CPU running while loop from flash	_	32	—	µA/MHz
abled, DCDC in LP mode ³		26 MHz HFRCO, CPU running while loop from flash	_	33	_	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	36		µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	156	—	µA/MHz

4.1.12 Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply current (including I_SENSE)	I _{VMON}	In EM0 or EM1, 1 supply monitored, $T \le 85 \text{ °C}$	_	6.3	TBD	μA
		In EM0 or EM1, 4 supplies monitored, $T \le 85 \text{ °C}$	—	12.5	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62		nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	_	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	_	99	_	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold		99		nA
Loading of monitored supply	I _{SENSE}	In EM0 or EM1	—	2	_	μA
		In EM2, EM3 or EM4	—	2	_	nA
Threshold range	V _{VMON_RANGE}		1.62	_	3.4	V
Threshold step size	N _{VMON_STESP}	Coarse	—	200	_	mV
		Fine	—	20	—	mV
Response time	t _{VMON_RES}	Supply drops at 1V/µs rate		460		ns
Hysteresis	V _{VMON_HYST}		_	26	_	mV

Table 4.19. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current, continuous conversions, WARMUP- MODE=KEEPCSENWARM	ICSEN_ACTIVE	SAR or Delta Modulation conver- sions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on		90.5		μA
HFPERCLK supply current	ICSEN_HFPERCLK	Current contribution from HFPERCLK when clock to CSEN block is enabled.	_	2.25	_	µA/MHz

Note:

 Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Slew rate ⁵	SR	DRIVESTRENGTH = 3, INCBW=1 ³	_	4.7	_	V/µs
		DRIVESTRENGTH = 3, INCBW=0	_	1.5	_	V/µs
		DRIVESTRENGTH = 2, INCBW=1 ³	_	1.27	_	V/µs
		DRIVESTRENGTH = 2, INCBW=0	_	0.42		V/µs
		DRIVESTRENGTH = 1, INCBW=1 ³	_	0.17	_	V/µs
		DRIVESTRENGTH = 1, INCBW=0	_	0.058		V/µs
		DRIVESTRENGTH = 0, INCBW=1 ³	_	0.044	_	V/µs
		DRIVESTRENGTH = 0, INCBW=0	_	0.015	_	V/µs
Startup time ⁶	T _{START}	DRIVESTRENGTH = 2	_	_	TBD	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	_	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	_	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	_	TBD	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	_	70	_	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	_	70	_	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90	_	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	_	90		dB

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Note:								
1. Specified configuration fo V. Nominal voltage gain is	r 3X-Gain configu s 3.	uration is: INCBW = 1, HCMDIS = 1, I	RESINSEL = '	/SS, V _{INPUT} =	= 0.5 V, V _{OUT}	_{PUT} = 1.5		
2. If the maximum C _{LOAD} is	exceeded, an iso	lation resistor is required for stability.	See AN0038	for more infor	mation.			
3. When INCBW is set to 1 or the OPAMP may not b	 When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable. 							
4. Current into the load resist drive the resistor feedbac another ~10 μA current w	4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.							
5. Step between 0.2V and V	/ _{OPA} -0.2V, 10%-9	0% rising/falling range.						
6. From enable to output se	ttled. In sample-a	nd-off mode, RC network after OPAN	IP will contrib	ute extra dela	y. Settling err	or < 1mV.		
7. In unit gain connection, U product of the OPAMP ar	IGF is the gain-band 1/3 attenuation	andwidth product of the OPAMP. In 32 of the feedback network.	x Gain conneo	tion, UGF is t	he gain-band	width		
8. Specified configuration fo V _{OUTPUT} = 0.5 V.	r Unit gain buffer	configuration is: INCBW = 0, HCMDI	S = 0, RESIN	SEL = DISAB	LE. V _{INPUT} =	0.5 V,		
9. When HCMDIS=1 and inp and CMRR specifications	put common mode do not apply to th	e transitions the region from V _{OPA} -1.4 his transition region.	4V to V _{OPA} -1\	/, input offset	will change. F	PSRR		
4.1.18 LCD Driver								

Table 4.25. LCD Driver

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Frame rate	f _{LCDFR}		TBD	_	TBD	Hz
LCD supply range ²	V _{LCDIN}		1.8		3.8	V
LCD output voltage range	V _{LCD}	Current source mode, No external LCD capacitor	2.0		V _{LCDIN} -0.4	V
		Step-down mode with external LCD capacitor	2.0		V _{LCDIN}	V
		Charge pump mode with external LCD capacitor	2.0	_	Min of 3.8 and 1.9 * V _{LCDIN}	V
Contrast control step size	STEP _{CONTRAST}	Current source mode	_	64	—	mV
		Charge pump or Step-down mode	_	43	—	mV
Contrast control step accura- cy ¹	ACC _{CONTRAST}		_	+/-4	_	%

Note:

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

2. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description					
PE15	79	GPIO	PA15	80	GPIO					
Note: 1. GPIO with	Note: 1. GPIO with 5V tolerance are indicated by (5V).									

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24 28	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	29	GPIO (5V)
PD1	30	GPIO	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC7	37	GPIO
VREGVSS	38	Voltage regulator VSS	VREGSW	39	DCDC regulator switching node
VREGVDD	40	Voltage regulator VDD input	DVDD	41	Digital power supply.
DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	43	GPIO
PE5	44	GPIO	PE6	45	GPIO
PE7	46	GPIO	PC12	47	GPIO (5V)
PC13	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.6. EFM32TG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.6.	EFM32TG11B5xx	in QFN64	Device	Pinout
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 38	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:	-			-	

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description											
	Analog	Timers	Communication	Other								
PC4	BUSACMP0Y BU- SACMP0X OPA0_P LCD_SEG24	TIM0_CC0 #5 TIM0_CDTI2 #3 LE- TIM0_OUT0 #3	US2_CLK #0 U0_TX #4 I2C1_SDA #0	LES_CH4 GPIO_EM4WU6								
PC5	BUSACMP0Y BU- SACMP0X OPA0_N LCD_SEG25	TIM0_CC1 #5 LE- TIM0_OUT1 #3	US2_CS #0 U0_RX #4 I2C1_SCL #0	LES_CH5								
PB7	LFXTAL_P	TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 U0_CTS #4									
PB8	LFXTAL_N	TIM0_CDTI1 #4 TIM1_CC1 #3	US0_RX #4 US1_CS #0 U0_RTS #4	CMU_CLKI0 #2								
PA8	BU_STAT	TIM0_CC0 #6 LE- TIM0_OUT0 #6	US2_RX #2									
PA9	BUSAY BUSBX LCD_SEG26	TIM0_CC1 #6 LE- TIM0_OUT1 #6	US2_CLK #2									
PA10	BUSBY BUSAX LCD_SEG27	TIM0_CC2 #6	US2_CS #2									
PA12	BU_VOUT	WTIM0_CDTI0 #2	US0_CLK #5 US2_RTS #2	CMU_CLK0 #5 ACMP1_O #3								
PA13	BUSAY BUSBX	TIM0_CC2 #7 WTIM0_CDTI1 #2	US0_CS #5 US2_TX #3									
PA14	BUSBY BUSAX LCD_BEXT	WTIM0_CDTI2 #2	US1_TX #6 US2_RX #3 US3_RTS #2	ACMP1_O #4								
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT LCD_SEG28	TIM0_CDTI2 #4 TIM1_CC2 #3 LE- TIM0_OUT0 #1 PCNT0_S1IN #7	US0_CTS #5 US1_CLK #5 US2_CS #3 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLKI0 #7 ACMP0_O #3 GPIO_EM4WU7								
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT LCD_SEG29	TIM1_CC3 #3 LE- TIM0_OUT1 #1 PCNT0_S0IN #7	US2_CTS #1 I2C1_SCL #1									
PB13	BUSAY BUSBX HFXTAL_P	WTIM1_CC0 #0	US0_CLK #4 US1_CTS #5 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0								
PB14	BUSBY BUSAX HFXTAL_N	WTIM1_CC1 #0	US0_CS #4 US1_RTS #5 LEU0_RX #1	PRS_CH6 #1								
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU- SADC0Y BUSADC0X	WTIM1_CC2 #0	CAN0_RX #2 US1_TX #1									
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BU- SADC0Y BUSADC0X OPA3_OUT	TIM0_CC0 #2 WTIM1_CC3 #0	CAN0_TX #2 US1_RX #1									
PD2	BUSADC0Y BUSADC0X	TIM0_CC1 #2 WTIM1_CC0 #1	US1_CLK #1									
PD3	BUSADC0Y BUSADC0X OPA2_N LCD_SEG30	TIM0_CC2 #2 WTIM1_CC1 #1	US1_CS #1									
PD4	BUSADC0Y BUSADC0X OPA2_P LCD_SEG31	WTIM0_CDTI0 #4 WTIM1_CC2 #1	US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0								

Alternate	LOC	ATION							
Functionality	0 - 3	4 - 7	Description						
ТІМ0_СС0	0: PA0 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.						
TIM0_CC1	0: PA1 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.						
TIM0_CC2	0: PA2 2: PD3 3: PC1	4: PF2 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.						
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.						
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.						
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.						
TIM1_CC0	0: PC13 1: PE10 3: PB7	4: PD6 5: PF2	Timer 1 Capture Compare input / output channel 0.						
TIM1_CC1	0: PC14 1: PE11 3: PB8	4: PD7 5: PF3	Timer 1 Capture Compare input / output channel 1.						
TIM1_CC2	0: PC15 1: PE12 3: PB11	4: PC13 5: PF4	Timer 1 Capture Compare input / output channel 2.						
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 6: PF5	Timer 1 Capture Compare input / output channel 3.						
U0_CTS	2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.						
U0_RTS	2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.						
U0_RX	2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.						

Alternate	LOCA	ATION										
Functionality	0 - 3	4 - 7	Description									
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.									
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.									
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.									
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.									
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.									
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.									
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.									
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.									
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.									
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.									
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.									
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.									
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.									

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	СНЗ	CH2	CH1	CH0
APORT0X	BUSADC0X																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT0Y	BUSADC0Y																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				6A9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 5.18. ADC0 Bus and Pin Mapping

Port	Bus	CH31	СНЗС	CH26	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH16	CH18	CH17	CH16	CH1	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	9HC	CH5	CH4	СНЗ	CH2	CH1	СНО
CE	хт																																
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
CE	хт_	SEN	ISE																														
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Table 5.19. CSEN Bus and Pin Mapping

Dimension	Min	Тур	Max								
A	_	_	1.20								
A1	0.05	—	0.15								
A2	0.95	1.00	1.05								
b	0.17	0.17 0.20									
с	0.09	0.09 —									
D		14.00 BSC									
D1	12.00 BSC										
е	0.50 BSC										
E	14.00 BSC										
E1		12.00 BSC									
L	0.45	0.60	0.75								
L1		1.00 REF									
θ	0	3.5	7								
ааа		0.20									
bbb		0.20									
ссс	0.08										
ddd	0.08										
еее		0.05									
Note:											

Table 6.1. TQFP80 Package Dimensions

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This package outline conforms to JEDEC MS-026, variant ADD.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Мах									
A	0.70	0.75	0.80								
A1	0.00	_	0.05								
b	0.20	0.25	0.30								
A3	0.203 REF										
D		9.00 BSC									
е	0.40 BSC										
E	9.00 BSC										
D2	7.10	7.20	7.30								
E2	7.10	7.20	7.30								
L	0.35	0.40	0.45								
ааа		0.10									
bbb		0.10									
ссс	0.10										
ddd	0.05										
еее	0.08										

Table 7.1. QFN80 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP48 Package Specifications

10.1 TQFP48 Package Dimensions

