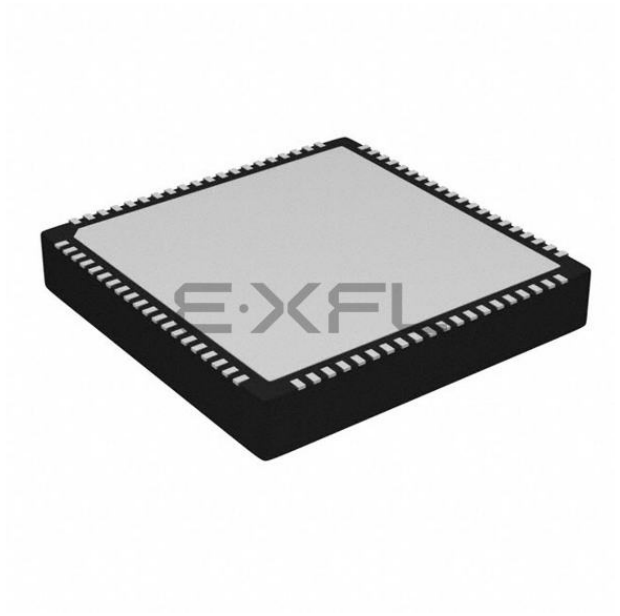
Silicon Labs - EFM32TG11B540F64IM80-A Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	80-WFQFN Exposed Pad
Supplier Device Package	80-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64im80-a

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC
-	LCD

4.1.8 Brown Out Detector (BOD)

Table 4.10. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling (EM0/EM1)	TBD	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	TBD	—	TBD	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	TBD	—	TBD	MHz

4.1.19 Pulse Counter (PCNT)

Table 4.26. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 Analog Port (APORT)

Table 4.27. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

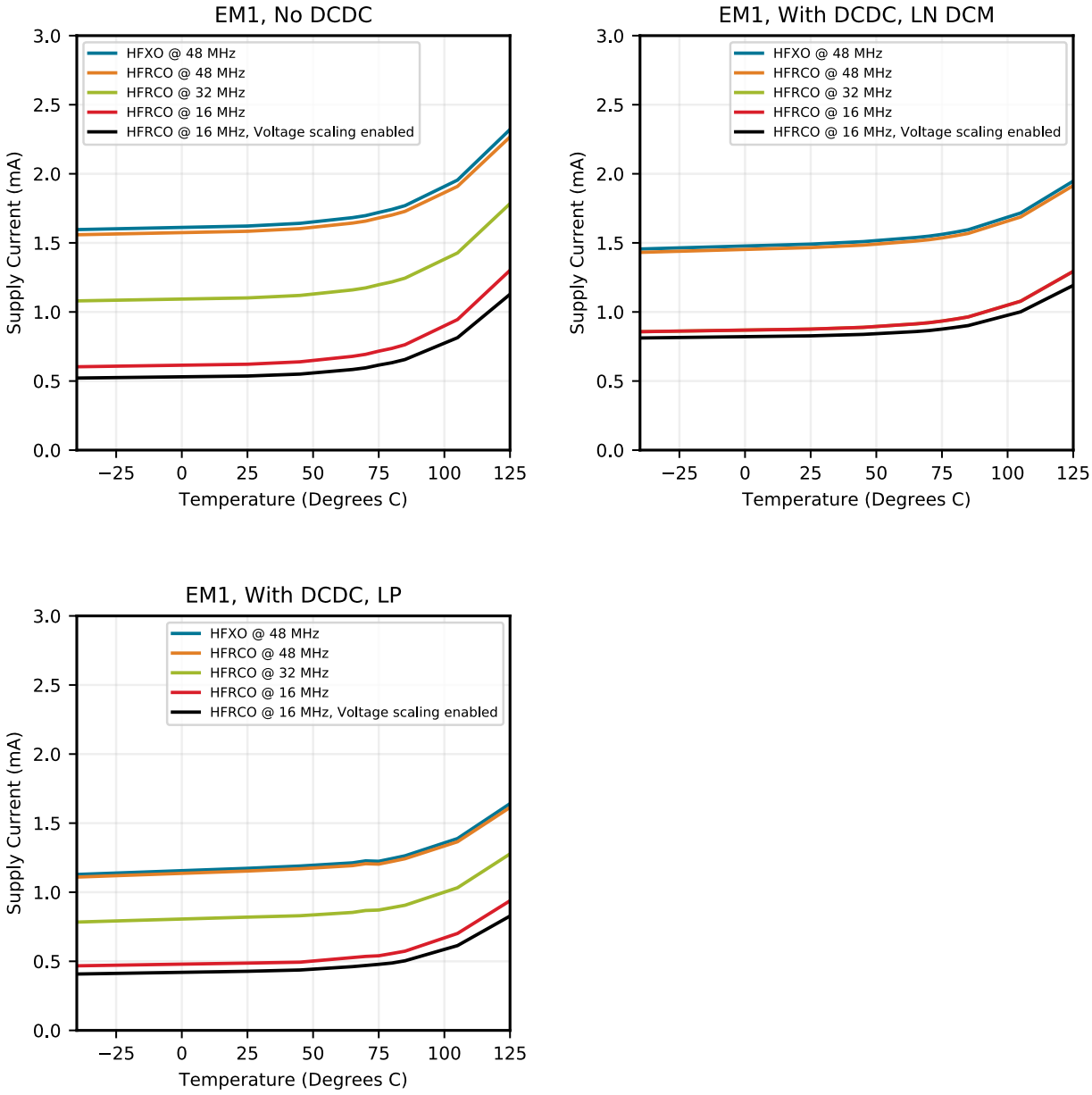


Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

5.2 EFM32TG11B5xx in QFN80 Device Pinout

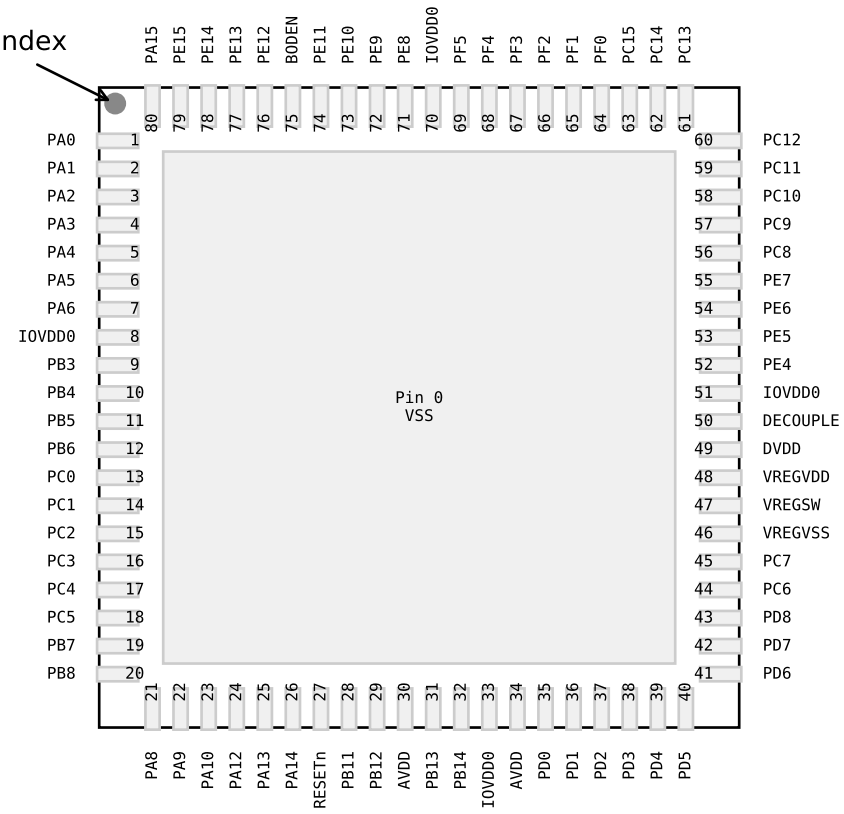


Figure 5.2. EFM32TG11B5xx in QFN80 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.2. EFM32TG11B5xx in QFN80 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 46	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 33 51 70	Digital IO power supply 0.	PB3	9	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:
1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	11	GPIO	PA8	12	GPIO
PA12	13	GPIO	PA14	14	GPIO
RESETn	15	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	16	GPIO
AVDD	18 22	Analog power supply.	PB13	19	GPIO
PB14	20	GPIO	PD4	23	GPIO
PD5	24	GPIO	PD6	25	GPIO
PD7	26	GPIO	PD8	27	GPIO
VREGVSS	28	Voltage regulator VSS	VREGSW	29	DCDC regulator switching node
VREGVDD	30	Voltage regulator VDD input	DVDD	31	Digital power supply.
DECOUPLE	32	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	33	GPIO
PE5	34	GPIO	PE6	35	GPIO
PE7	36	GPIO	PF0	37	GPIO (5V)
PF1	38	GPIO (5V)	PF2	39	GPIO
PF3	40	GPIO	PF4	41	GPIO
PF5	42	GPIO	PE10	45	GPIO
PE11	46	GPIO	PE12	47	GPIO
PE13	48	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA14	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	15	GPIO	PD5	16	GPIO
PD6	17	GPIO	PD7	18	GPIO
VREGSW	20	DCDC regulator switching node	VREGVDD	21	Voltage regulator VDD input
DVDD	22	Digital power supply.	DECOUPLE	23	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	24	GPIO	PE5	25	GPIO
PC15	26	GPIO (5V)	PF0	27	GPIO (5V)
PF1	28	GPIO (5V)	PF2	29	GPIO
PE11	31	GPIO	PE12	32	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB8	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11 15	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	16	GPIO	PD5	17	GPIO
PD6	18	GPIO	PD7	19	GPIO
DVDD	20	Digital power supply.	DECOUPLE	21	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PC13	22	GPIO (5V)	PC14	23	GPIO (5V)
PC15	24	GPIO (5V)	PF0	25	GPIO (5V)
PF1	26	GPIO (5V)	PF2	27	GPIO
PE10	29	GPIO	PE11	30	GPIO
PE12	31	GPIO	PE13	32	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.
LCD_SEG7	0: PE11		LCD segment line 7.
LCD_SEG8	0: PE12		LCD segment line 8.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG35	0: PC9		LCD segment line 35.
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.

Table 5.19. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
CEXT_SENSE																																	
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA3_OUT																																	
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14								PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
OPA3_P																																	
APORT4X	BUSDX											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT3X	BUSCX												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT2X	BUSBX			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT1X	BUSAX		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
VDAC0_OUT0 / OPA0_OUT																																	
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	

11.2 QFN32 PCB Land Pattern

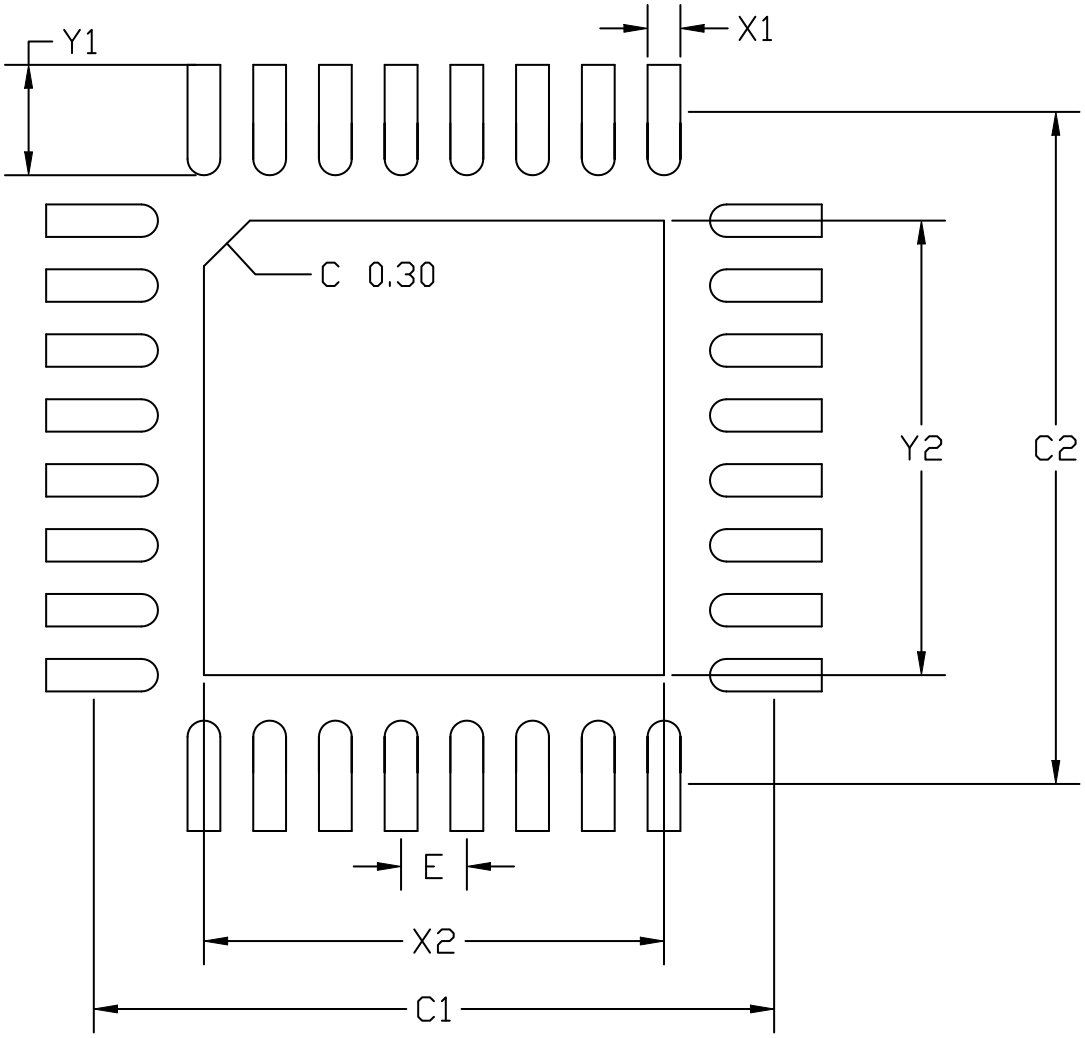
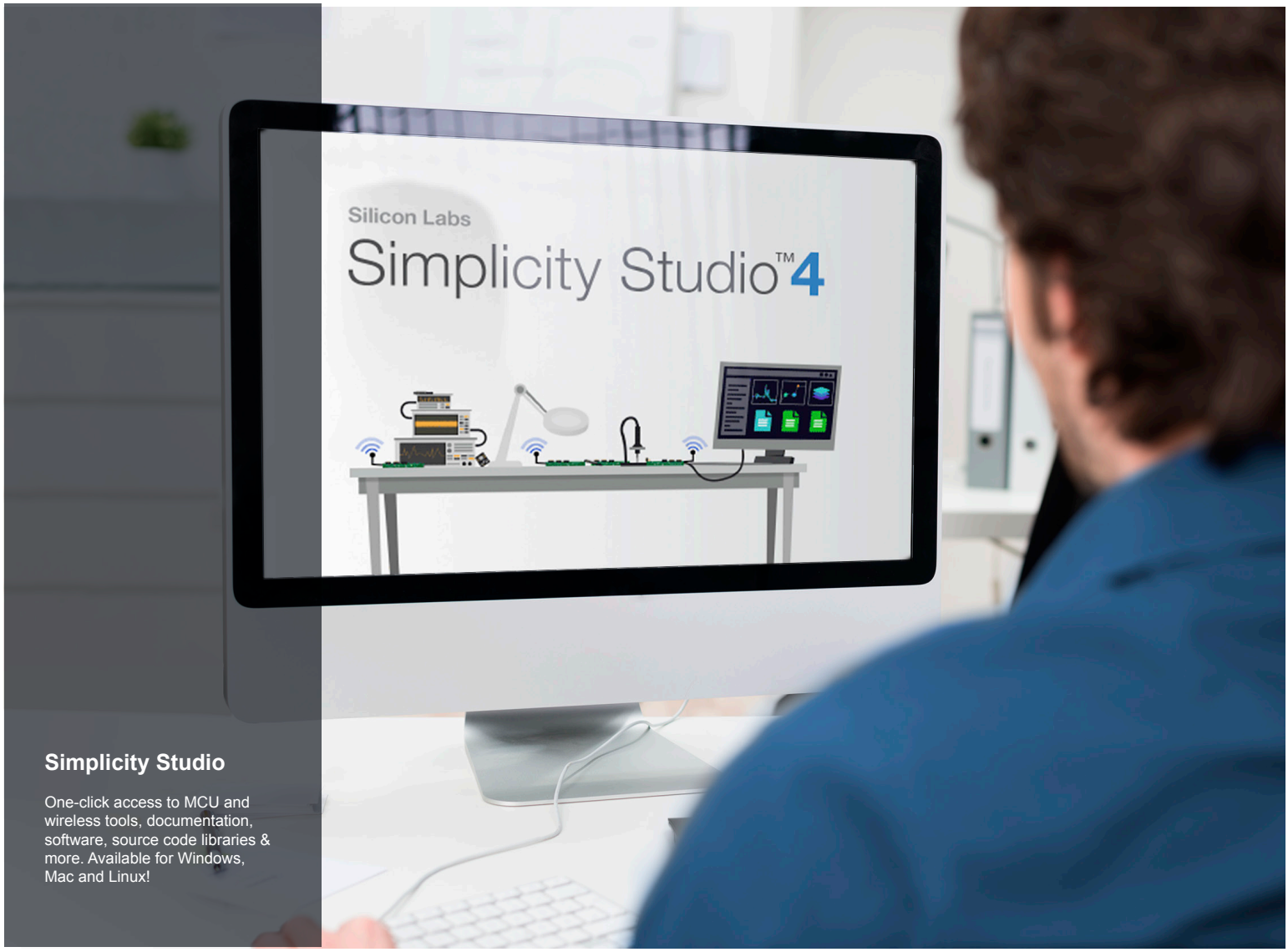


Figure 11.2. QFN32 PCB Land Pattern Drawing



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