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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64iq48-a

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

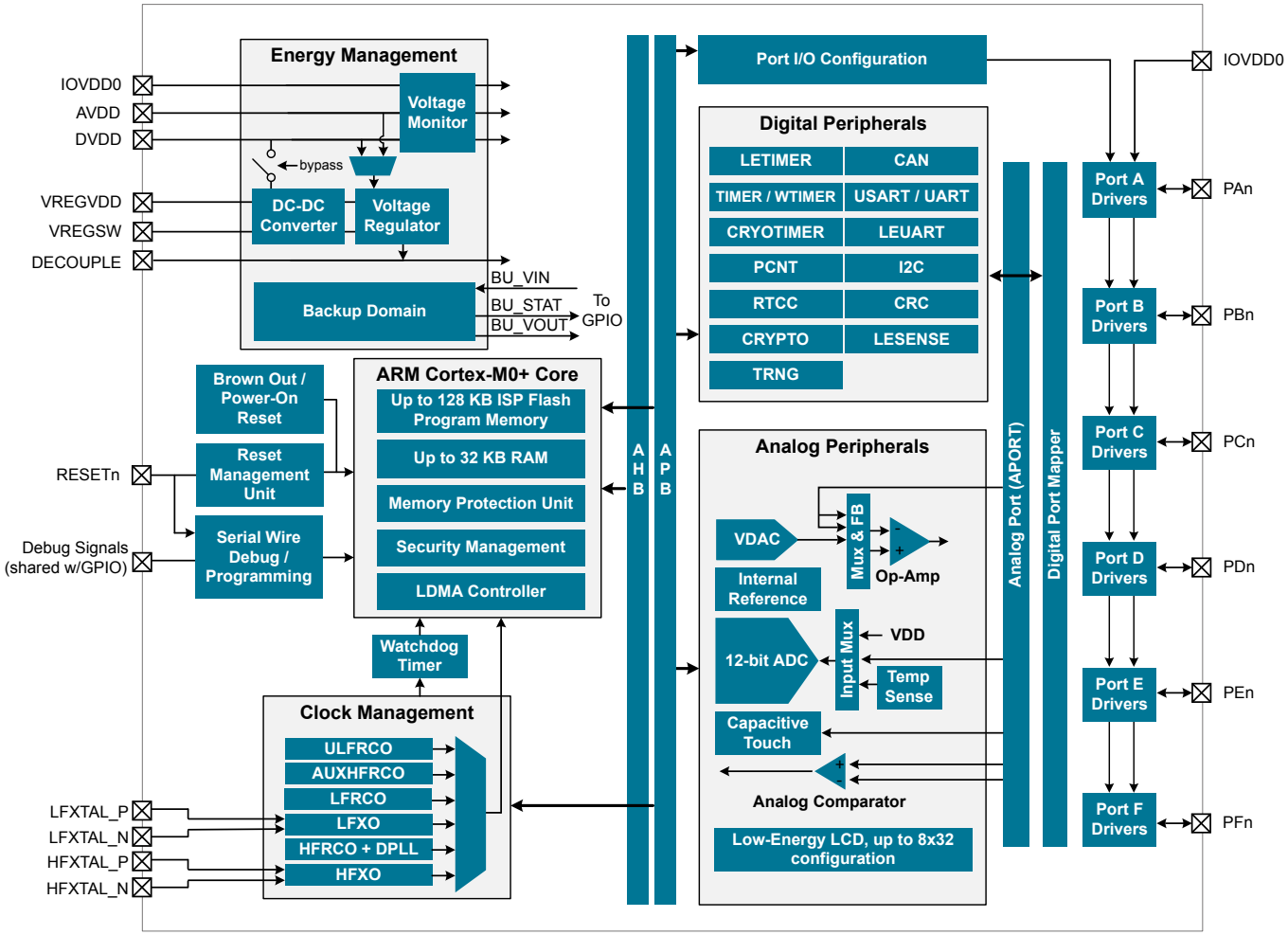

Figure 3.1. Detailed EFM32TG11 Block Diagram

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	—	°C/W
Thermal resistance, TQFP48 Package	$THETA_{JA\_TQFP48}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	43.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	—	°C/W
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	37.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	35.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	—	°C/W
Thermal resistance, QFN80 Package	$THETA_{JA\_QFN80}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP80 Package	$THETA_{JA\_TQFP80}$	4-Layer PCB, Air velocity = 0 m/s	—	49.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	44.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.6	—	°C/W

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	10	TBD	nA
		BU_VIN powering backup domain[1]	—	450	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.75	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.37	—	µA
		128 byte RAM retention, no RTCC	—	0.37	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.05	—	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.18	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.18	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

4.1.22 USART SPI

SPI Master Timing

Table 4.31. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}		-19.8	—	18.9	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}		-10	—	14.5	ns
MISO setup time [1] [3]	t_{SU_MI}	IOVDD = 1.62 V	75	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time [1] [3]	t_{H_MI}		-10	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

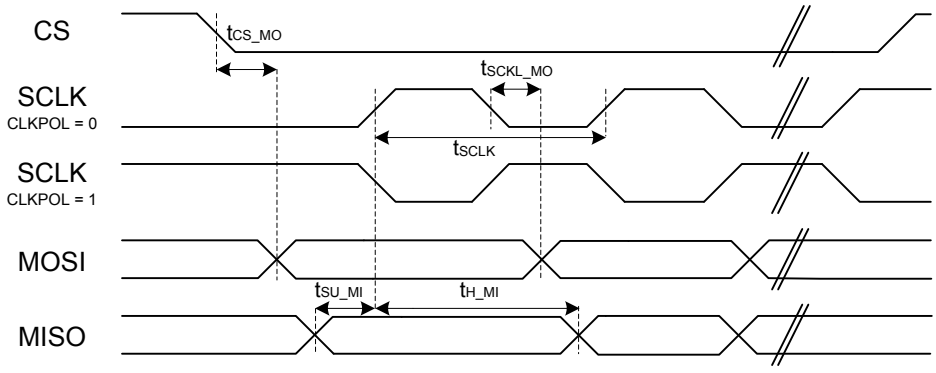

Figure 4.1. SPI Master Timing Diagram

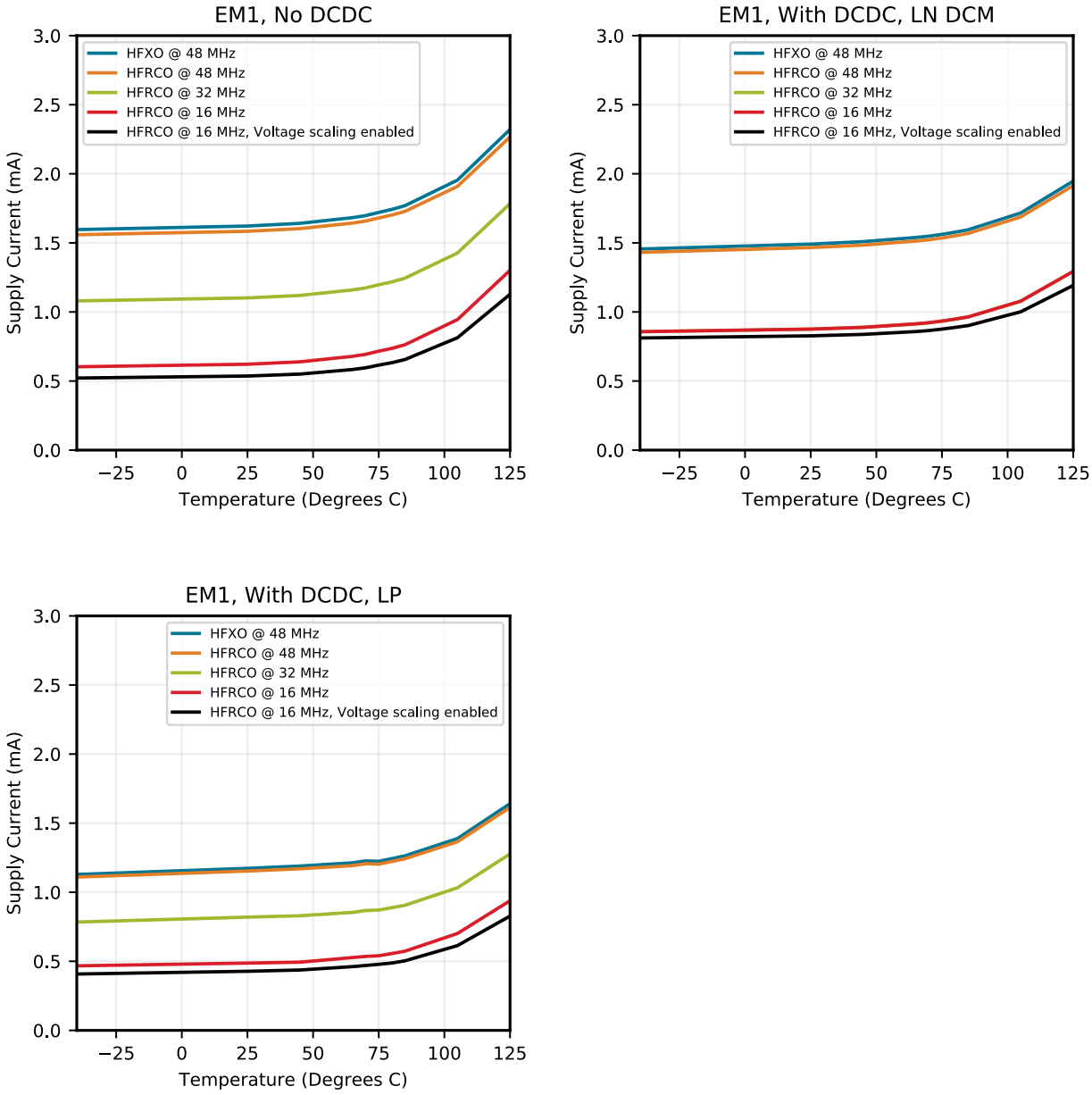

Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

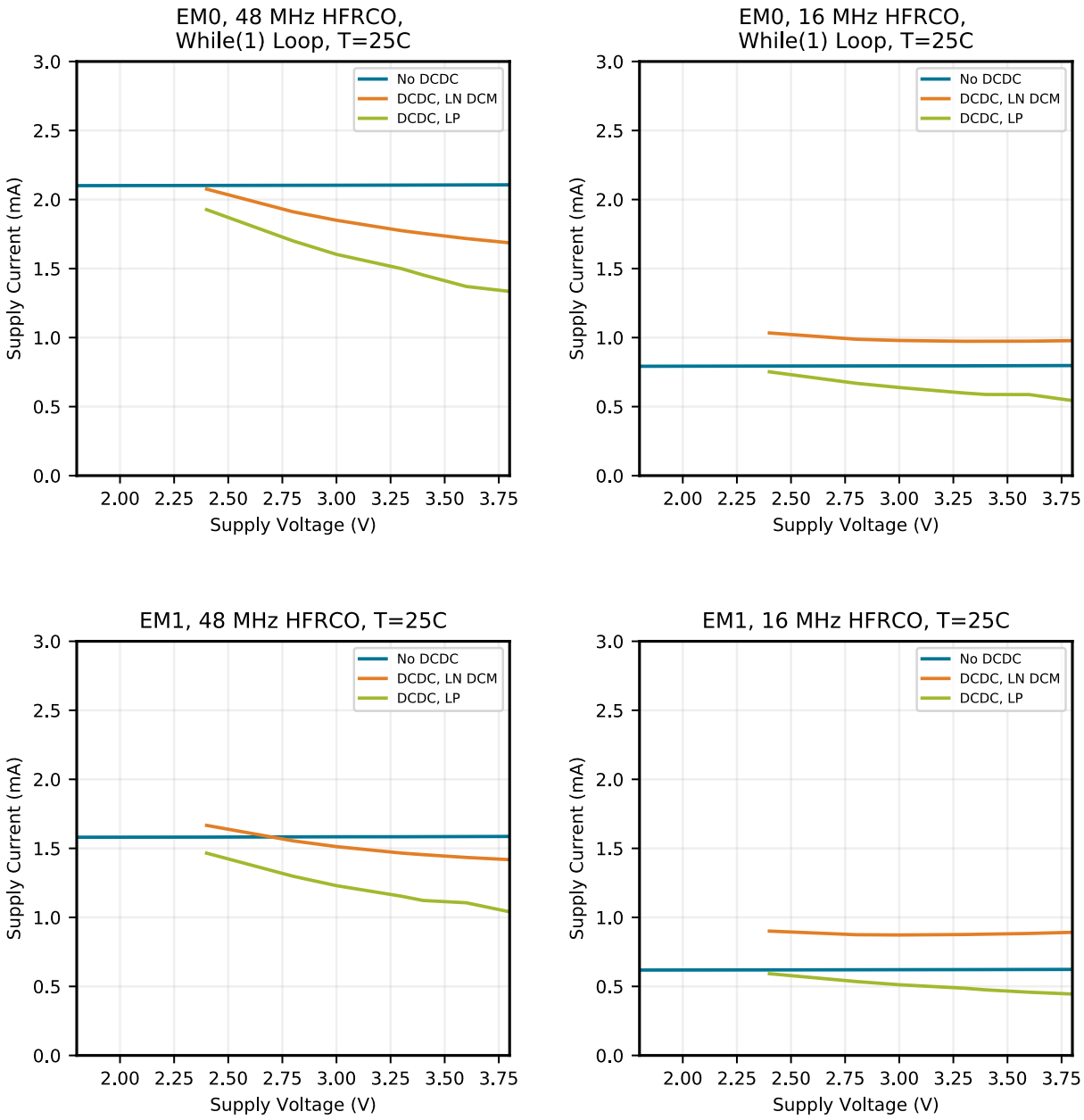

Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

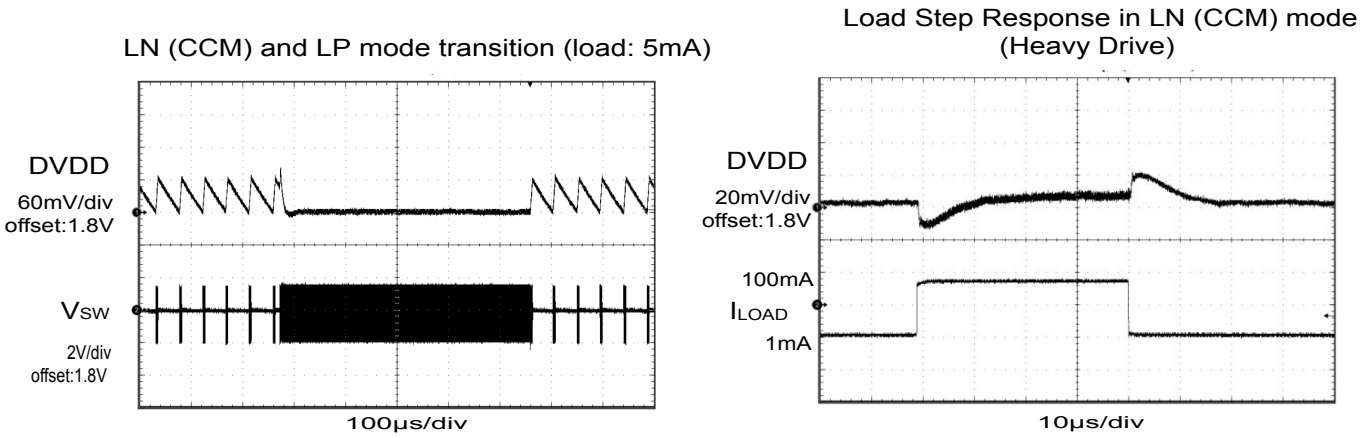

Figure 4.9. DC-DC Converter Transition Waveforms

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE12	76	GPIO	PE13	77	GPIO
PE14	78	GPIO	PE15	79	GPIO
PA15	80	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO
PC9	42	GPIO	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.10 EFM32TG11B3xx in QFP48 Device Pinout

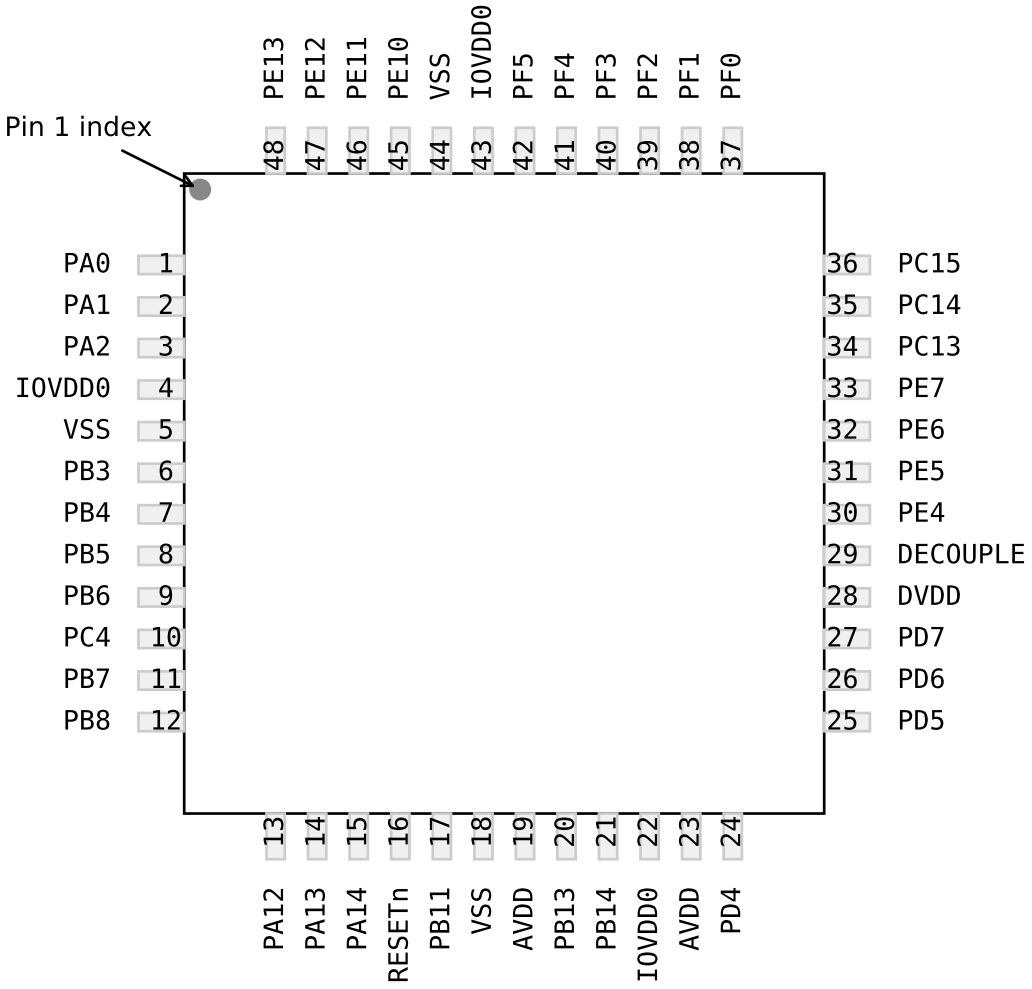

Figure 5.10. EFM32TG11B3xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.10. EFM32TG11B3xx in QFP48 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 22 43	Digital IO power supply 0.
VSS	5 18 44	Ground	PB3	6	GPIO
PB4	7	GPIO	PB5	8	GPIO
PB6	9	GPIO	PC4	10	GPIO

5.14 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.15 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.14. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PA0	BUSBY BUSAX LCD_SEG13	TIM0_CC0 #0 TIM0_CC1 #7 PCNT0_S0IN #4	US1_RX #5 US3_TX #0 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PA1	BUSAY BUSBX LCD_SEG14	TIM0_CC0 #7 TIM0_CC1 #0 PCNT0_S1IN #4	US3_RX #0 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PA2	BUSBY BUSAX LCD_SEG15	TIM0_CC2 #0	US1_RX #6 US3_CLK #0	CMU_CLK0 #0
PA3	BUSAY BUSBX LCD_SEG16	TIM0_CDTI0 #0	US3_CS #0 U0_TX #2	CMU_CLK2 #1 CMU_CLK2 #4 CMU_CLKI0 #1 LES_ALTEX2
PA4	BUSBY BUSAX LCD_SEG17	TIM0_CDTI1 #0	US3_CTS #0 U0_RX #2	LES_ALTEX3
PA5	BUSAY BUSBX LCD_SEG18	TIM0_CDTI2 #0	US3_RTS #0 U0_CTS #2	LES_ALTEX4 ACMP1_O #7
PA6	BUSBY BUSAX LCD_SEG19	WTIM0_CC0 #1	U0_RTS #2	PRS_CH6 #0 ACMP0_O #4 GPIO_EM4WU1
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	TIM1_CC3 #2 WTIM0_CC0 #6	US2_TX #1 US3_TX #2	ACMP0_O #7
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	WTIM0_CC1 #6	US2_RX #1	
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	WTIM0_CC2 #6 PCNT0_S0IN #6	US0_RTS #4 US2_CLK #1	
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	TIM0_CC0 #3 PCNT0_S1IN #6	US0_CTS #4 US2_CS #1	
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	TIM0_CC1 #3 PCNT0_S0IN #2	CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	TIM0_CC2 #3 WTIM0_CC0 #7 PCNT0_S1IN #2	CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	TIM0_CDTI0 #3 WTIM0_CC1 #7	US1_RX #4 US2_TX #0	LES_CH2
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X	TIM0_CDTI1 #3 WTIM0_CC2 #7	US1_CLK #4 US2_RX #0	LES_CH3

Table 7.1. QFN80 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions

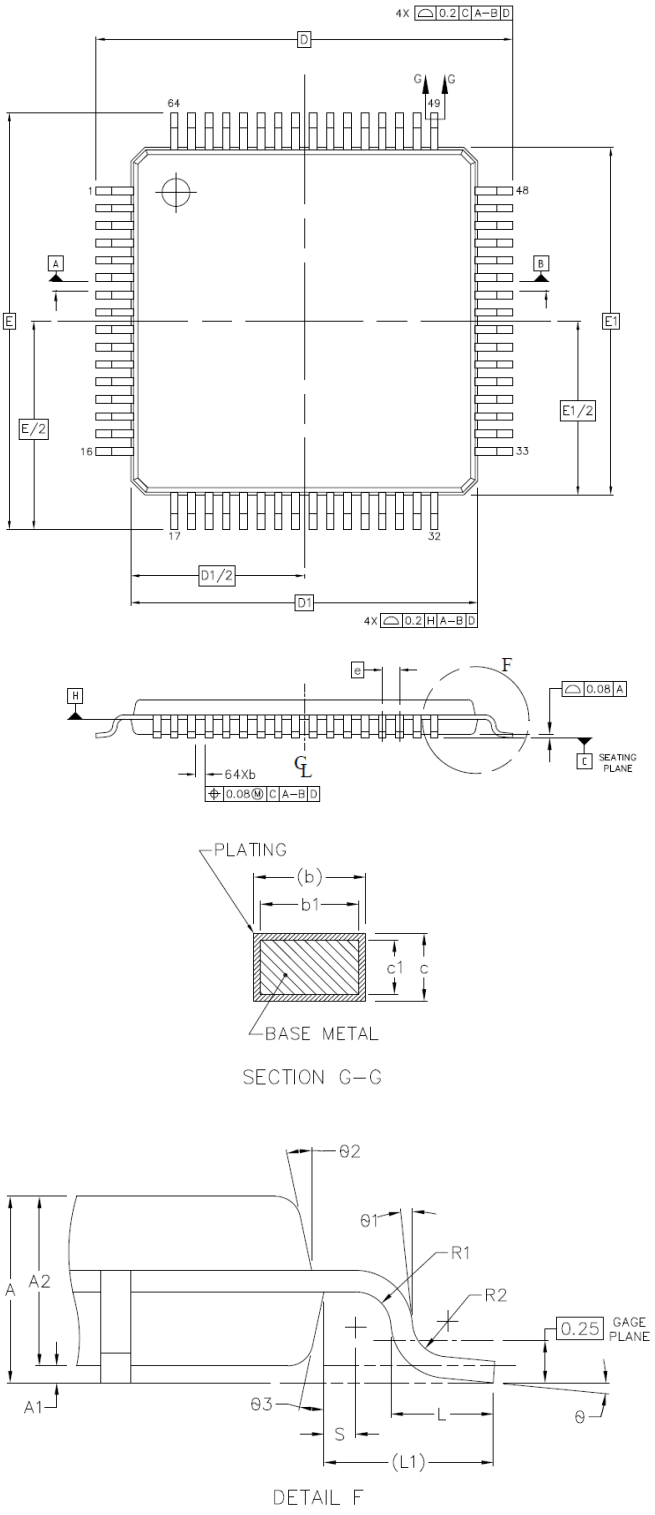

Figure 8.1. TQFP64 Package Drawing

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions

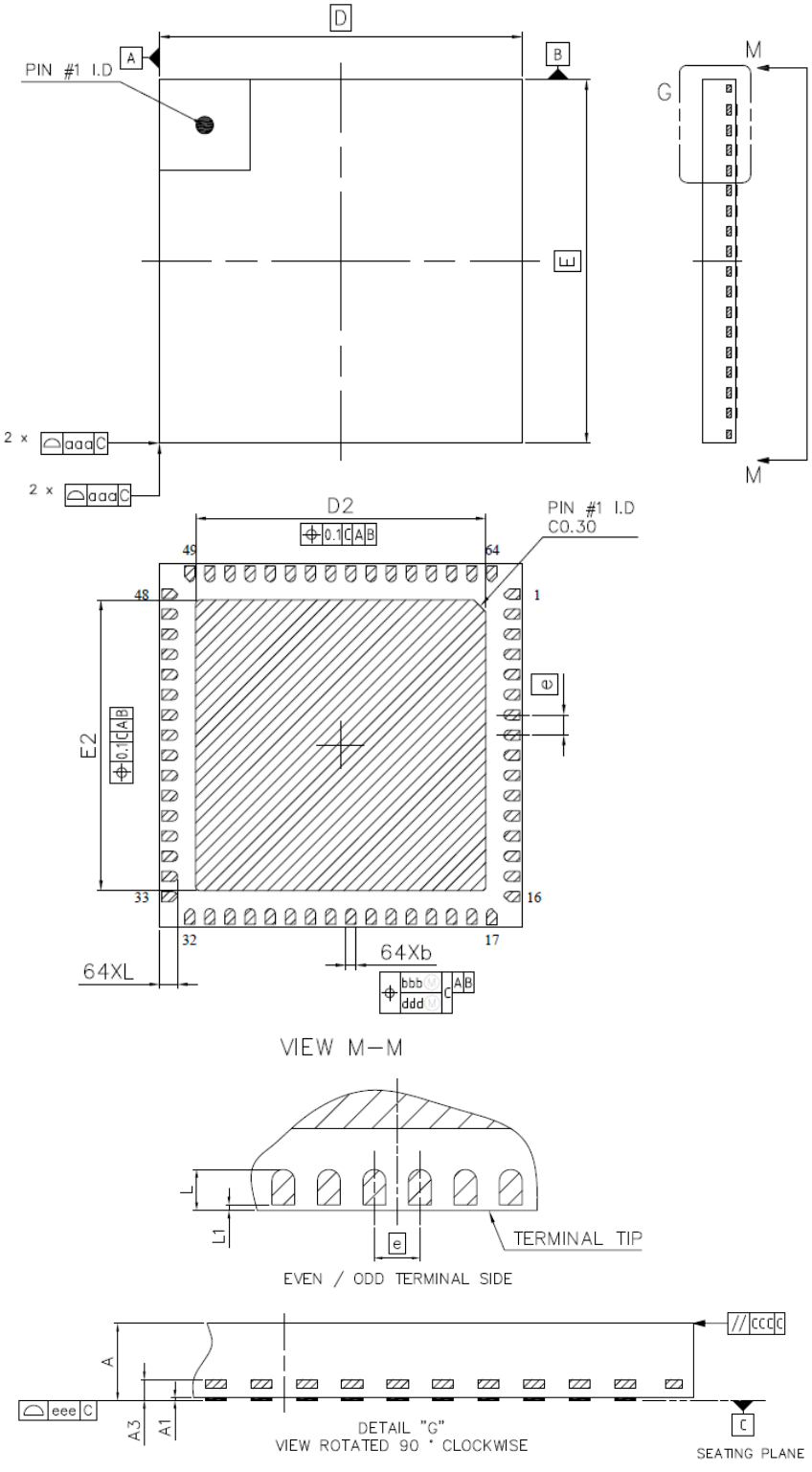

Figure 9.1. QFN64 Package Drawing

12. Revision History

Revision 0.5

February, 2018

- 4.1 Electrical Characteristics updated with latest characterization data and production test limits.
- Added 4.1.3 Thermal Characteristics.
- Added 4.2 Typical Performance Curves section.
- Corrected OPA / VDAC output connections in Figure 5.14 APORT Connection Diagram on page 119.

Revision 0.1

May 1st, 2017

Initial release.