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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64iq48-ar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1. Feature List

The EFM32TG11 highlighted features are listed below.

ARM Cortex-M0+ CPU platform

- High performance 32-bit processor @ up to 48 MHz
- Memory Protection Unit
- Wake-up Interrupt Controller
- Flexible Energy Management System
 - 37 µA/MHz in Active Mode (EM0)
 - 1.30 µA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- Integrated DC-DC buck converter
- Backup Power Domain
 - RTCC and retention registers in a separate power domain, available in all energy modes
 - Operation from backup battery when main power absent/ insufficient
- Up to 128 kB flash program memory
- Up to 32 kB RAM data memory
- Communication Interfaces
 - CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (24 MHz) operation on one instance
 - 1 × Universal Asynchronous Receiver/ Transmitter
 - 1 × Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - $2 \times I^2C$ Interface with SMBus support
 - Address recognition in EM3 Stop Mode

Up to 67 General Purpose I/O Pins

- Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
- Configurable peripheral I/O locations
- · 5 V tolerance on select pins
- Asynchronous external interrupts
- Output state retention and wake-up from Shutoff Mode
- Up to 8 Channel DMA Controller
- Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- Hardware Cryptography
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- Hardware CRC engine
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- Security Management Unit (SMU)
 - Fine-grained access control for on-chip peripherals
- Integrated Low-energy LCD Controller with up to 8 × 32 segments
 - Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- Ultra Low-Power Precision Analog Peripherals
 - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - On-chip temperature sensor
 - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Up to 2 × Analog Comparator (ACMP)
 - Up to 4 × Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
 - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

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3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Current consumption in EM4H mode, with voltage	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	_	0.75	—	μA
scaling enabled		128 byte RAM retention, CRYO- TIMER running from ULFRCO	—	0.37	_	μA
		128 byte RAM retention, no RTCC	_	0.37	_	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.05	—	μA
Current consumption of pe- ripheral power domain 1, with voltage scaling enabled	IPD1_VS	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ¹	_	0.18	_	μA
Current consumption of pe- ripheral power domain 2, with voltage scaling enabled	IPD2_VS	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ¹	_	0.18	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.

2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Wake up time from EM1	t _{EM1_WU}		_	3	_	AHB Clocks
Wake up from EM2	t _{EM2_WU}	Code execution from flash	—	10.1	_	μs
		Code execution from RAM	—	3.1	_	μs
Wake up from EM3	t _{EM3_WU}	Code execution from flash	—	10.1	_	μs
		Code execution from RAM	—	3.1	_	μs
Wake up from EM4H ¹	t _{EM4H_WU}	Executing from flash		88		μs
Wake up from EM4S ¹	t _{EM4S_WU}	Executing from flash	_	282	_	μs
Time from release of reset	t _{RESET}	Soft Pin Reset released	—	50	_	μs
ecution		Any other reset released	—	352		μs
Power mode scaling time	tSCALE	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2}	_	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ³	_	4.3	_	μs

Table 4.9. Wake Up Times

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.

2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/μs for approximately 20 μs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).

3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.

4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

4.1.22 USART SPI

SPI Master Timing

Table 4.31. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}		2 * t _{HFPERCLK}	_	_	ns
CS to MOSI ^{1 3}	t _{CS_MO}		-19.8		18.9	ns
SCLK to MOSI ^{1 3}	t _{SCLK_MO}		-10		14.5	ns
MISO setup time ^{1 3}	t _{SU_MI}	IOVDD = 1.62 V	75	—		ns
		IOVDD = 3.0 V	40		_	ns
MISO hold time ^{1 3}	t _{H_MI}		-10			ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2. t_{HFPERCLK} is one period of the selected HFPERCLK.

3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).



Figure 4.1. SPI Master Timing Diagram



Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz



Figure 4.8. DC-DC Converter Typical Performance Characteristics

	1 11(3)	Description
PE13	77	GPIO
PE15	79	GPIO
	PE13 PE15	PE13 77 PE15 79

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description										
	Analog	Timers	Communication	Other							
PD5	BUSADC0Y BUSADC0X OPA2_OUT	WTIM0_CDTI1 #4 WTIM1_CC3 #1	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3								
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT OPA1_P	TIM1_CC0 #4 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_AL- TEX0 PRS_CH5 #2 ACMP0_O #2							
PD7	BUSADC0Y BUSADC0X ADC0_EXTN OPA1_N	TIM1_CC1 #4 WTIM1_CC1 #2 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_AL- TEX1 ACMP1_O #2							
PD8	BU_VIN	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1							
PC6	BUSACMP0Y BU- SACMP0X OPA3_P LCD_SEG32	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 I2C0_SDA #2	LES_CH6							
PC7	BUSACMP0Y BU- SACMP0X OPA3_N LCD_SEG33	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 I2C0_SCL #2	LES_CH7							
PE4	BUSDY BUSCX LCD_COM0	WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 I2C0_SDA #7								
PE5	BUSCY BUSDX LCD_COM1	WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 I2C0_SCL #7								
PE6	BUSDY BUSCX LCD_COM2	WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2							
PE7	BUSCY BUSDX LCD_COM3	WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2							
PC8	BUSACMP1Y BU- SACMP1X LCD_SEG34		US0_CS #2	LES_CH8 PRS_CH4 #0							
PC9	BUSACMP1Y BU- SACMP1X LCD_SEG35		US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2							
PC10	BUSACMP1Y BU- SACMP1X		US0_RX #2	LES_CH10							
PC11	BUSACMP1Y BU- SACMP1X		US0_TX #2 I2C1_SDA #4	LES_CH11							
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BU- SACMP1Y BUSACMP1X	TIM1_CC3 #0	US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3	CMU_CLK0 #1 LES_CH12							
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BU- SACMP1Y BUSACMP1X	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3	LES_CH13							
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BU- SACMP1Y BUSACMP1X	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 LEU0_TX #5	LES_CH14 PRS_CH0 #2							

Alternate	LOCA	ATION					
Functionality	0 - 3	4 - 7	Description				
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.				
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.				
VDAC0_OUT1 / OPA1_OUT	0_OUT1 / _OUT Digital to Analog Converter DAC0 output channel number 1.						
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC154: PD1 Digital to Analog Converter DAC0 alternative output for channel 1.						
WTIM0_CC0	0: PE4 1: PA6	4: PC15 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.				
WTIM0_CC1	0: PE5	4: PF0 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.				
WTIM0_CC2	0: PE6	4: PF1 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.				
WTIM0_CDTI0	0: PE10 2: PA12	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.				
WTIM0_CDTI1	0: PE11 2: PA13	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.				
WTIM0_CDTI2	0: PE12 2: PA14	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.				
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	5: PE7	Wide timer 1 Capture Compare input / output channel 0.				
WTIM1_CC1	0: PB14 1: PD3 2: PD7	4: PE4	Wide timer 1 Capture Compare input / output channel 1.				
WTIM1_CC2	0: PD0 1: PD4 2: PD8	4: PE5	Wide timer 1 Capture Compare input / output channel 2.				

Alternate	LOCA	ATION						
Functionality	0 - 3	4 - 7	Description					
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.					

EFM32TG11 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VD	/DAC0_OUT1 / OPA1_OUT																																
APORT1Y	BUSAY			PB13		PB11						PB5		PB3				PA15		PA13				PA9				PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12						PB6		PB4						PA14				PA10				PA6		PA4		PA2		PA0
APORT3Y	BUSCY											PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5					
APORT4Y	BUSDY												PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				

8. TQFP64 Package Specifications

8.1 TQFP64 Package Dimensions



Figure 8.1. TQFP64 Package Drawing

Table 9.2. QFN64 PCB Land Pattern Dimensions

Dimension	Тур
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.

8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.

9. A No-Clean, Type-3 solder paste is recommended.

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. QFN32 Package Specifications

11.1 QFN32 Package Dimensions



Dimension	Min	Тур	Мах								
A	0.70	0.75	0.80								
A1	0.00	_	0.05								
A3	0.203 REF										
b	0.20	0.30									
D		5.0 BSC									
D2/E2	3.60	3.70	3.80								
E	5.0 BSC										
е		0.50 BSC									
L	0.35	0.40	0.45								
ааа		0.10									
bbb		0.10									
ссс		0.10									
ddd		0.05									
еее	0.08										

Table 11.1. QFN32 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.

4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Figure 11.2. QFN32 PCB Land Pattern Drawing

12. Revision History

Revision 0.5

February, 2018

- 4.1 Electrical Characteristics updated with latest characterization data and production test limits.
- Added 4.1.3 Thermal Characteristics.
- Added 4.2 Typical Performance Curves section.
- Corrected OPA / VDAC output connections in Figure 5.14 APORT Connection Diagram on page 119.

Revision 0.1

May 1st, 2017

Initial release.