Silicon Labs - EFM32TG11B540F64IQ80-AR Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	63
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32tg11b540f64iq80-ar

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

3.6.5 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmittion may be disabled in order to support Time Triggered CAN applications.

3.6.6 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.7 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Tiny Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

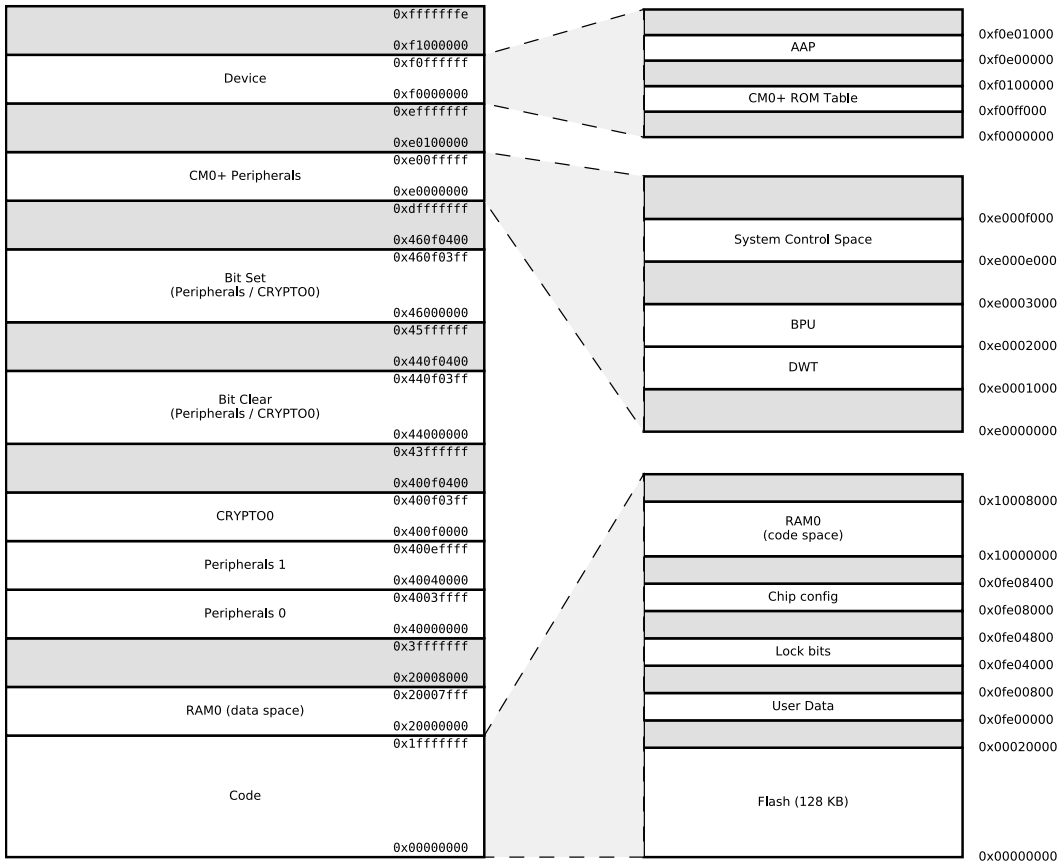

Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.82	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	µA
		128 byte RAM retention, no RTCC	—	0.45	TBD	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.07	TBD	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.18	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.18	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.3 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.9 Oscillators

4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.11. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.22. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}	Single-Ended	0	—	V_{VREF}	V
		Differential[2]	$-V_{VREF}$	—	V_{VREF}	V
Current consumption including references (2 channels)[1]	I_{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	396	—	µA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	72	—	µA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02	—	2	—	µA
Current from HFPERCLK[4]	I_{DAC_CLK}		—	5.8	—	µA/MHz
Sample rate	SR_{DAC}		—	—	500	ksps
DAC clock frequency	f_{DAC}		—	—	1	MHz
Conversion time	$t_{DACCONV}$	f_{DAC} = 1MHz	2	—	—	µs
Settling time	$t_{DACSETTLE}$	50% fs step settling to 5 LSB	—	2.5	—	µs
Startup time	$t_{DACSTARTUP}$	Enable to 90% fs output, settling to 10 LSB	—	—	12	µs
Output impedance	R_{OUT}	DRIVESTRENGTH = 2, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Full supply range	—	2	—	Ω
Power supply rejection ratio[6]	PSRR	Vout = 50% fs. DC	—	65.5	—	dB

4.1.21 I2C

4.1.21.1 I2C Standard-mode (Sm)[1]

Table 4.28. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	µs
STOP condition set-up time	t_{SU_STO}		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:
1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

SPI Slave Timing

Table 4.32. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [3] [2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [3] [2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		20	—	70	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		15	—	150	ns
MOSI setup time [1] [3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		7	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		14 + 1.5 * $t_{HFPERCLK}$	—	40 + 2.5 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

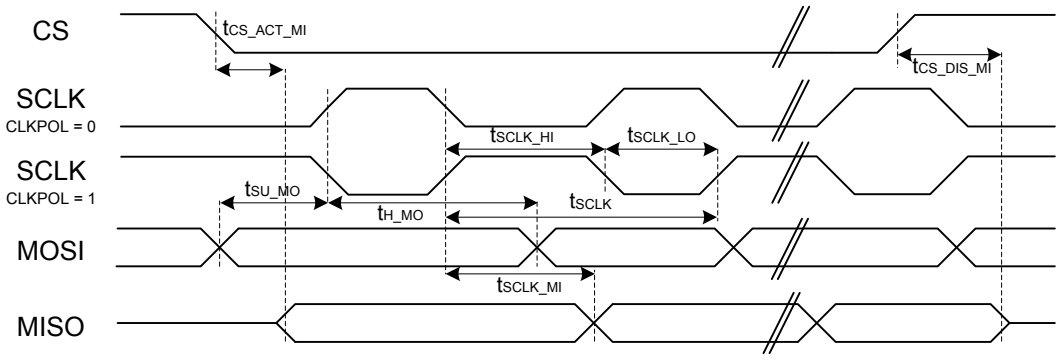

Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

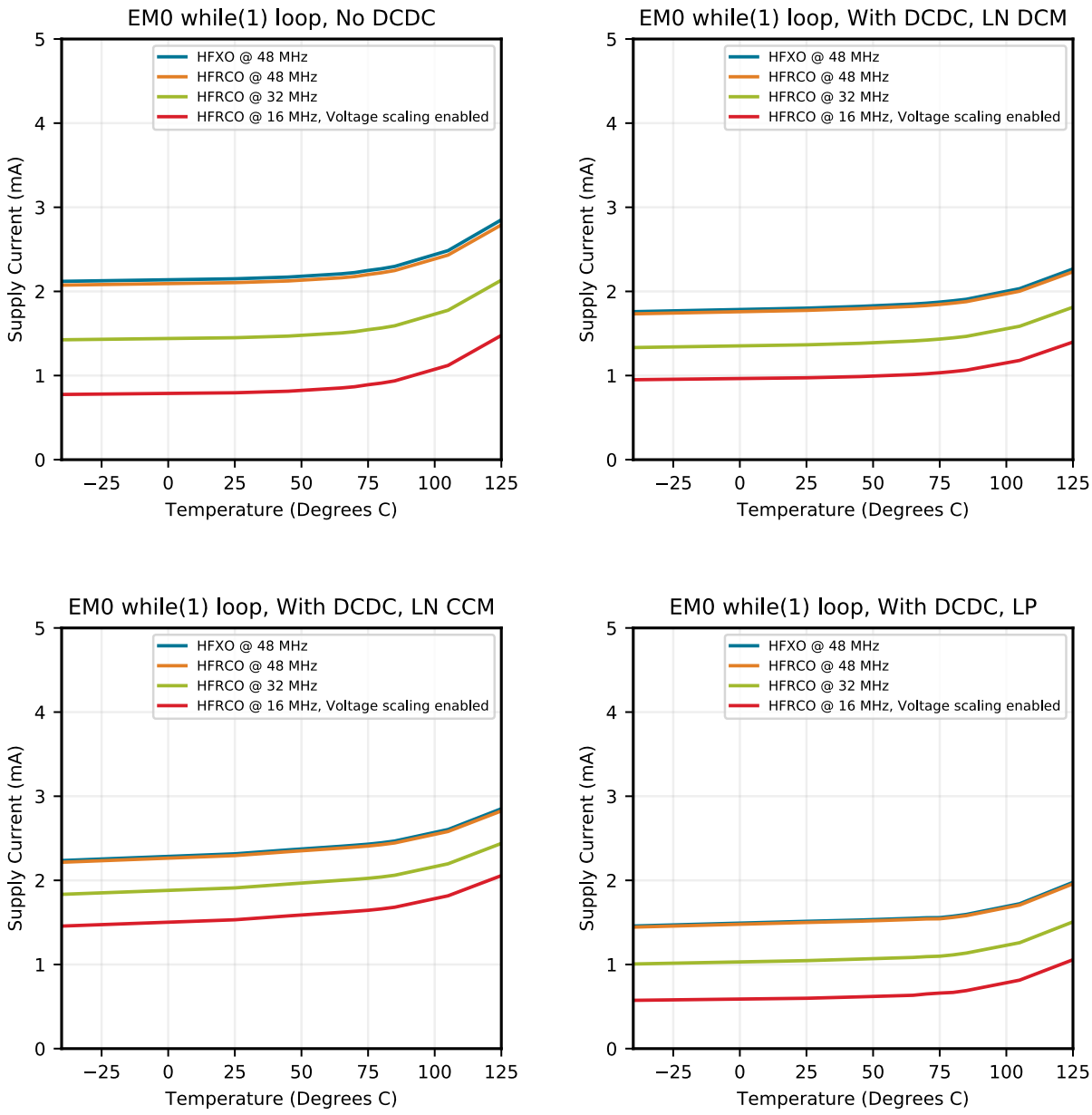

Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

5.9 EFM32TG11B5xx in QFP48 Device Pinout

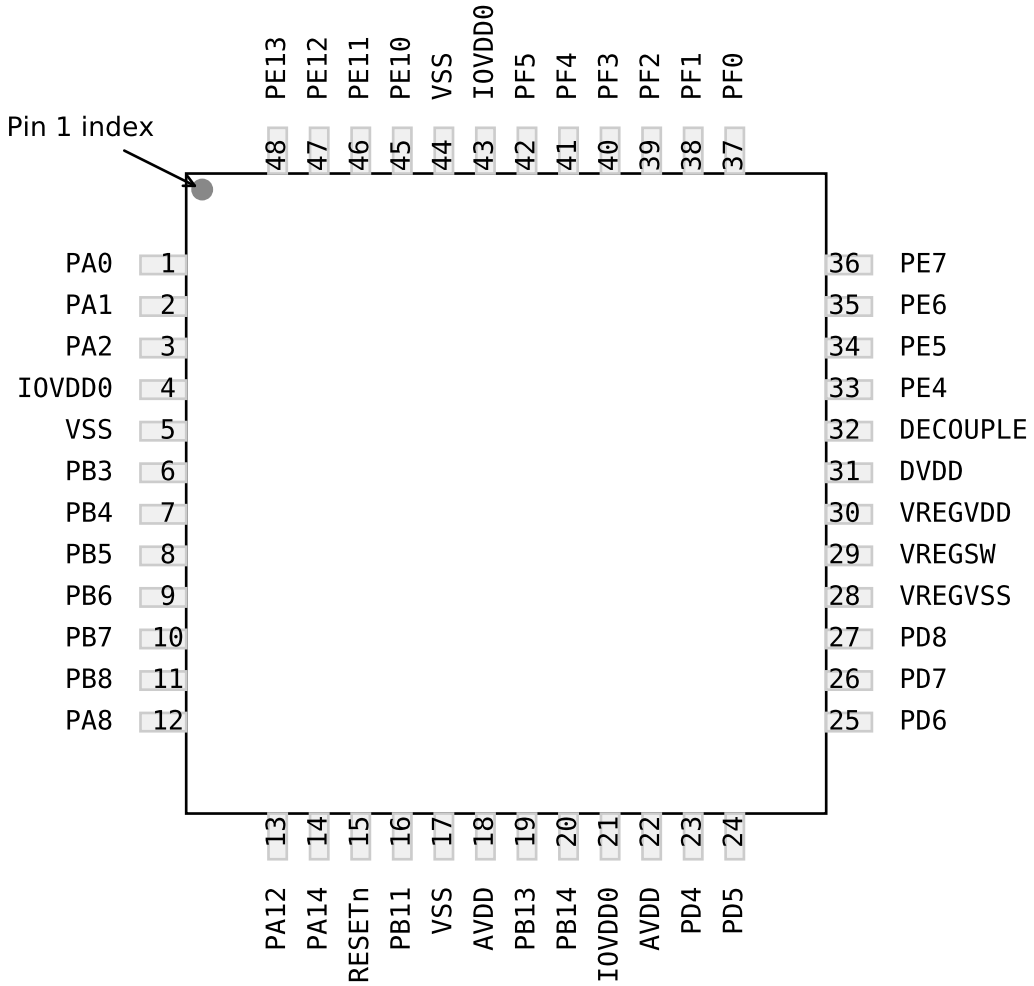

Figure 5.9. EFM32TG11B5xx in QFP48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.9. EFM32TG11B5xx in QFP48 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	IOVDD0	4 21 43	Digital IO power supply 0.
VSS	5 17 44	Ground	PB3	6	GPIO
PB4	7	GPIO	PB5	8	GPIO
PB6	9	GPIO	PB7	10	GPIO

5.12 EFM32TG11B5xx in QFN32 Device Pinout

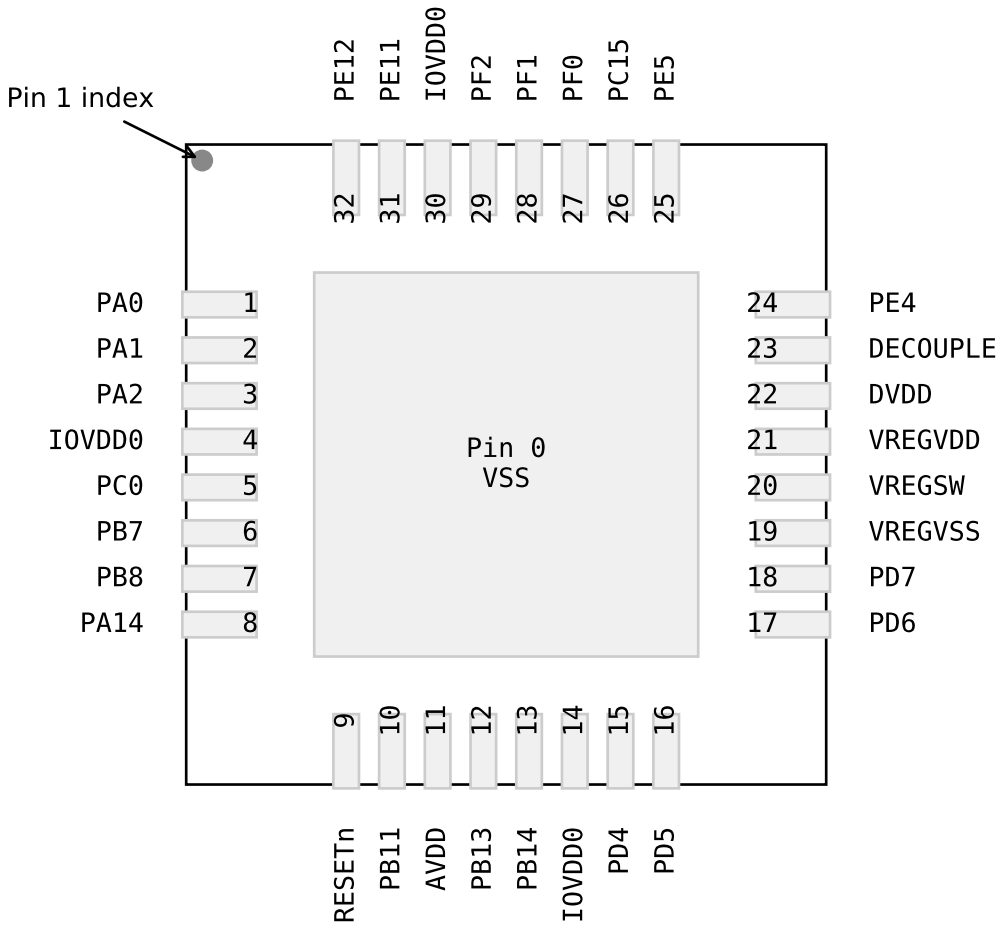

Figure 5.12. EFM32TG11B5xx in QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.14 GPIO Functionality Table or 5.15 Alternate Functionality Overview.

Table 5.12. EFM32TG11B5xx in QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVSS	0 19	Voltage regulator VSS	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
IOVDD0	4 14 30	Digital IO power supply 0.	PC0	5	GPIO (5V)
PB7	6	GPIO	PB8	7	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA14	8	GPIO	RESETn	9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	10	GPIO	AVDD	11	Analog power supply.
PB13	12	GPIO	PB14	13	GPIO
PD4	15	GPIO	PD5	16	GPIO
PD6	17	GPIO	PD7	18	GPIO
VREGSW	20	DCDC regulator switching node	VREGVDD	21	Voltage regulator VDD input
DVDD	22	Digital power supply.	DECOUPLE	23	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	24	GPIO	PE5	25	GPIO
PC15	26	GPIO (5V)	PF0	27	GPIO (5V)
PF1	28	GPIO (5V)	PF2	29	GPIO
PE11	31	GPIO	PE12	32	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.14 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.15 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.14. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description			
	Analog	Timers	Communication	Other
PA0	BUSBY BUSAX LCD_SEG13	TIM0_CC0 #0 TIM0_CC1 #7 PCNT0_S0IN #4	US1_RX #5 US3_TX #0 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PA1	BUSAY BUSBX LCD_SEG14	TIM0_CC0 #7 TIM0_CC1 #0 PCNT0_S1IN #4	US3_RX #0 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PA2	BUSBY BUSAX LCD_SEG15	TIM0_CC2 #0	US1_RX #6 US3_CLK #0	CMU_CLK0 #0
PA3	BUSAY BUSBX LCD_SEG16	TIM0_CDTI0 #0	US3_CS #0 U0_TX #2	CMU_CLK2 #1 CMU_CLK2 #4 CMU_CLKI0 #1 LES_ALTEX2
PA4	BUSBY BUSAX LCD_SEG17	TIM0_CDTI1 #0	US3_CTS #0 U0_RX #2	LES_ALTEX3
PA5	BUSAY BUSBX LCD_SEG18	TIM0_CDTI2 #0	US3_RTS #0 U0_CTS #2	LES_ALTEX4 ACMP1_O #7
PA6	BUSBY BUSAX LCD_SEG19	WTIM0_CC0 #1	U0_RTS #2	PRS_CH6 #0 ACMP0_O #4 GPIO_EM4WU1
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	TIM1_CC3 #2 WTIM0_CC0 #6	US2_TX #1 US3_TX #2	ACMP0_O #7
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	WTIM0_CC1 #6	US2_RX #1	
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	WTIM0_CC2 #6 PCNT0_S0IN #6	US0_RTS #4 US2_CLK #1	
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	TIM0_CC0 #3 PCNT0_S1IN #6	US0_CTS #4 US2_CS #1	
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	TIM0_CC1 #3 PCNT0_S0IN #2	CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	TIM0_CC2 #3 WTIM0_CC0 #7 PCNT0_S1IN #2	CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	TIM0_CDTI0 #3 WTIM0_CC1 #7	US1_RX #4 US2_TX #0	LES_CH2
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X	TIM0_CDTI1 #3 WTIM0_CC2 #7	US1_CLK #4 US2_RX #0	LES_CH3

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.
LCD_SEG7	0: PE11		LCD segment line 7.
LCD_SEG8	0: PE12		LCD segment line 8.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PC4		LCD segment line 24.
LCD_SEG25	0: PC5		LCD segment line 25.
LCD_SEG26	0: PA9		LCD segment line 26.
LCD_SEG27	0: PA10		LCD segment line 27.
LCD_SEG28	0: PB11		LCD segment line 28.
LCD_SEG29	0: PB12		LCD segment line 29.
LCD_SEG30	0: PD3		LCD segment line 30.
LCD_SEG31	0: PD4		LCD segment line 31.
LCD_SEG32	0: PC6		LCD segment line 32.
LCD_SEG33	0: PC7		LCD segment line 33.
LCD_SEG34	0: PC8		LCD segment line 34.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.
PCNT0_S0IN	0: PC13 2: PC0 3: PD6	4: PA0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 2: PC1 3: PD7	4: PA1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PB13 2: PE7		Peripheral Reflex System PRS, channel 7.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM1_CC3	0: PD1 1: PD5 2: PC6	4: PE6	Wide timer 1 Capture Compare input / output channel 3.

9. QFN64 Package Specifications

9.1 QFN64 Package Dimensions

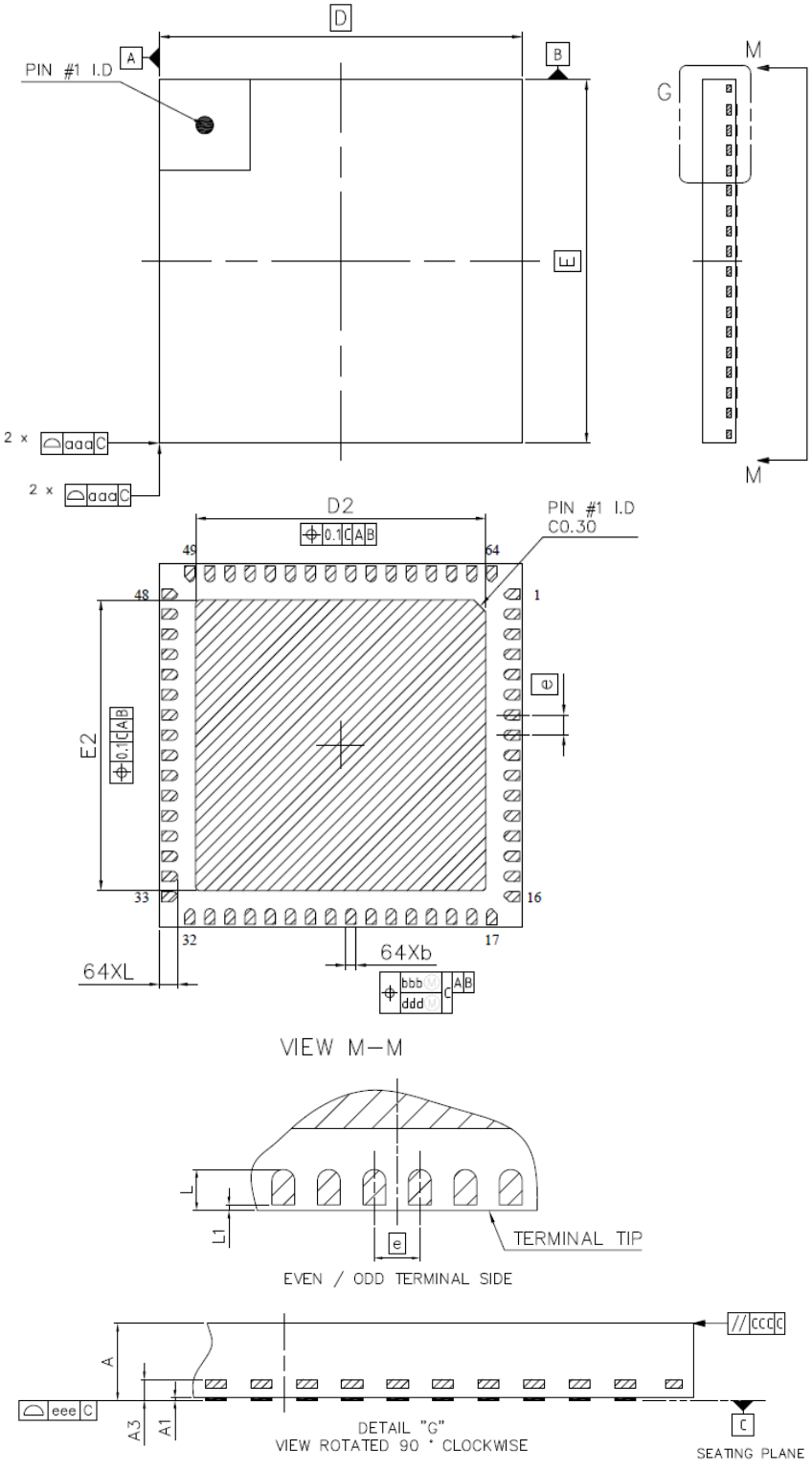

Figure 9.1. QFN64 Package Drawing

Table 9.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.