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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569cvjankgb

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Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDIC0	J2	I/O	GV_{DD}	27
D2_MDIC1	L2	I/O	GV_{DD}	27
D2_MDM0/D1_MDM4	A13	I/O	GV_{DD}	—
D2_MDM1/D1_MDM5	D13	I/O	GV_{DD}	—
D2_MDM2/D1_MDM6	G14	I/O	GV_{DD}	—
D2_MDM3/D1_MDM7	A9	I/O	GV_{DD}	—
D2_MDM8	E8	I/O	GV_{DD}	—
D2_MDQ0/D1_MDQ32	B14	I/O	GV_{DD}	—
D2_MDQ1/D1_MDQ33	C14	I/O	GV_{DD}	—
D2_MDQ2/D1_MDQ34	C11	I/O	GV_{DD}	—
D2_MDQ3/D1_MDQ35	B11	I/O	GV_{DD}	—
D2_MDQ4/D1_MDQ36	B15	I/O	GV_{DD}	—
D2_MDQ5/D1_MDQ37	A14	I/O	GV_{DD}	—
D2_MDQ6/D1_MDQ38	A12	I/O	GV_{DD}	—
D2_MDQ7/D1_MDQ39	A11	I/O	GV_{DD}	—
D2_MDQ8/D1_MDQ40	F14	I/O	GV_{DD}	—
D2_MDQ9/D1_MDQ41	F13	I/O	GV_{DD}	—
D2_MDQ10/D1_MDQ42	G11	I/O	GV_{DD}	—
D2_MDQ11/D1_MDQ43	F11	I/O	GV_{DD}	—
D2_MDQ12/D1_MDQ44	E14	I/O	GV_{DD}	—
D2_MDQ13/D1_MDQ45	D14	I/O	GV_{DD}	—
D2_MDQ14/D1_MDQ46	D12	I/O	GV_{DD}	—
D2_MDQ15/D1_MDQ47	E11	I/O	GV_{DD}	—
D2_MDQ16/D1_MDQ48	J15	I/O	GV_{DD}	—
D2_MDQ17/D1_MDQ49	J14	I/O	GV_{DD}	—
D2_MDQ18/D1_MDQ50	K13	I/O	GV_{DD}	—
D2_MDQ19/D1_MDQ51	J12	I/O	GV_{DD}	—
D2_MDQ20/D1_MDQ52	H15	I/O	GV_{DD}	—
D2_MDQ21/D1_MDQ53	G15	I/O	GV_{DD}	—
D2_MDQ22/D1_MDQ54	G13	I/O	GV_{DD}	—
D2_MDQ23/D1_MDQ55	H12	I/O	GV_{DD}	—
D2_MDQ24/D1_MDQ56	C10	I/O	GV_{DD}	—
D2_MDQ25/D1_MDQ57	C8	I/O	GV_{DD}	—
D2_MDQ26/D1_MDQ58	C7	I/O	GV_{DD}	—
D2_MDQ27/D1_MDQ59	B7	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D2_MDQ28/D1_MDQ60	B10	I/O	GV_{DD}	—
D2_MDQ29/D1_MDQ61	A10	I/O	GV_{DD}	—
D2_MDQ30/D1_MDQ62	A8	I/O	GV_{DD}	—
D2_MDQ31/D1_MDQ63	A7	I/O	GV_{DD}	—
D2_MDQS0/D1_MDQS4	C12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$	C13	I/O	GV_{DD}	—
D2_MDQS1/D1_MDQS5	G12	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$	F12	I/O	GV_{DD}	—
D2_MDQS2/D1_MDQS6	J13	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$	K14	I/O	GV_{DD}	—
D2_MDQS3/D1_MDQS7	D9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$	C9	I/O	GV_{DD}	—
D2_MDQS8	H9	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	G9	I/O	GV_{DD}	—
D2_MECC0	G10	I/O	GV_{DD}	—
D2_MECC1	H8	I/O	GV_{DD}	—
D2_MECC2	G8	I/O	GV_{DD}	—
D2_MECC3	F7	I/O	GV_{DD}	—
D2_MECC4	F10	I/O	GV_{DD}	—
D2_MECC5	D8	I/O	GV_{DD}	—
D2_MECC6	E7	I/O	GV_{DD}	—
D2_MECC7	D7	I/O	GV_{DD}	—
D2_MODT0	C1	O	GV_{DD}	—
D2_MODT1	A3	O	GV_{DD}	—
D2_MODT2	H3	O	GV_{DD}	—
D2_MODT3	E1	O	GV_{DD}	—
D2_MAPAR_OUT	F1	O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	G1	I	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	G4	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	E2	O	GV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK0}}$	AF23	O	OV_{DD}	2
$\overline{\text{DMA\_DACK1}}$/MSRCID1	AD27	O	OV_{DD}	11
$\overline{\text{DMA\_DACK2}}$/SD_CMD	AD24	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE0}}$	AD25	O	OV_{DD}	2

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PC25	P3	I/O	$LV_{DD}1$	—
QE_PC26	W8	I/O	OV_{DD}	—
QE_PC27	W9	I/O	OV_{DD}	—
QE_PC28	AF13	I/O	OV_{DD}	—
QE_PC29	V7	I/O	OV_{DD}	—
QE_PC30	AA14	I/O	OV_{DD}	—
QE_PC31	AA13	I/O	OV_{DD}	—
QE_PD0	AH6	I/O	OV_{DD}	11
QE_PD1	AF6	I/O	OV_{DD}	—
QE_PD2	AG6	I/O	OV_{DD}	—
QE_PD3	AF5	I/O	OV_{DD}	—
QE_PD4	AE4	I/O	OV_{DD}	22
QE_PD5	AD4	I/O	OV_{DD}	—
QE_PD6	AB6	I/O	OV_{DD}	—
QE_PD7	AD7	I/O	OV_{DD}	—
QE_PD8	AC6	I/O	OV_{DD}	—
QE_PD9	AD6	I/O	OV_{DD}	—
QE_PD10	AB5	I/O	OV_{DD}	—
QE_PD11	AC4	I/O	OV_{DD}	—
QE_PD12	AE5	I/O	OV_{DD}	—
QE_PD13	AE6	I/O	OV_{DD}	—
QE_PD14	AC7	I/O	OV_{DD}	—
QE_PD15	AB7	I/O	OV_{DD}	—
QE_PD16	AB8	I/O	OV_{DD}	—
QE_PD17	AA9	I/O	OV_{DD}	—
QE_PD18	Y8	I/O	OV_{DD}	—
QE_PD19	AA8	I/O	OV_{DD}	—
QE_PD20	AA12	I/O	OV_{DD}	—
QE_PD21	Y11	I/O	OV_{DD}	—
QE_PD22	AA11	I/O	OV_{DD}	—
QE_PD23	AB11	I/O	OV_{DD}	—
QE_PD24	AA7	I/O	OV_{DD}	—
QE_PD25	AB10	I/O	OV_{DD}	—
QE_PD26	Y9	I/O	OV_{DD}	—
QE_PD27	AA10	I/O	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Power Management				
ASLEEP	M23	O	OV_{DD}	11
Thermal Management				
THERM0	U21	—	Internal temperature diode cathode	32
THERM1	U20	—	Internal temperature diode anode	32
Reserved	T22	—	—	9
Analog				
D1_MVREF	N27	Reference voltage for DDR	MV_{REF}	—
D2_MVREF	J1			—
Power and Ground				
V_{DD}	L13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P16	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GV_{DD}	H13	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H16	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H2	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H20	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H24	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H27	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	H5	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J19	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	J3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K10	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K11	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K18	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K22	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K26	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K3	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K4	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K6	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	K9	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L15	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L21	1.8-/1.5-V DDR power supply	GV_{DD}	—
GV_{DD}	L23	1.8-/1.5-V DDR power supply	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to GV_{DD} through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to OV_{DD}.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Range	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD}_CORE AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	ScoreVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR2 and DDR3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	2
QUICC Engine block Ethernet interface I/O voltage	$LV_{DD}1$	–0.3 to 3.63 –0.3 to 2.75	V	—

Table 5. RESET Initialization Timing Specifications (continued)

Parameter	Min	Max	Unit	Notes
Maximum rise/fall time of $\overline{\text{HRESET}}$	—	1	SYSCLK	5
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLK	4
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	2	—	SYSCLK	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLK	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of $\overline{\text{HRESET}}$	8	—	SYSCLK	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLK	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in *AN4232 MPC8569E PowerQUICC III Design Checklist*.
4. SYSCLK is the primary clock input for the MPC8569E.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following table provides the PLL lock times.

Table 6. PLL Lock Times

Parameter	Min	Max	Unit
Core PLL lock time	—	100	µs
Platform PLL lock time	—	100	µs
QUICC Engine block PLL lock time	—	100	µs
DDR PLL lock times	—	100	µs

2.4.1 DDR2 and DDR3 SDRAM Interface DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Table 13. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.125	—	V	5
Input low voltage	V_{IL}	—	MVREF*n* – 0.125	V	5
Output high current (V_{OUT} = 1.320 V)	I_{OH}	—	–13.4	mA	6, 7
Output low current (V_{OUT} = 0.380 V)	I_{OL}	13.4	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed the MVREF*n* DC level by more than ±2% of GV_{DD} (that is, ± 36 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must meet the specifications stated in Table 16.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. I_{OH} and I_{OL} are measured at GV_{DD} = 1.7 V.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 14. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4

Table 20. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications[6]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz		280[7] 320[8]	—		
667 MHz		400[7] 450[8]	—		
533 MHz		538	—		
400 MHz		700	—		

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rate and in DDR3 mode to 667 and 800 MHz data rate.
7. DDR3 only
8. DDR2 only

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

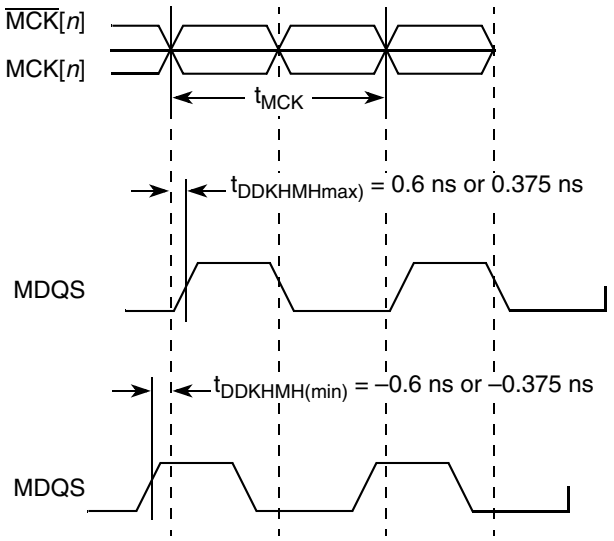

Figure 9. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

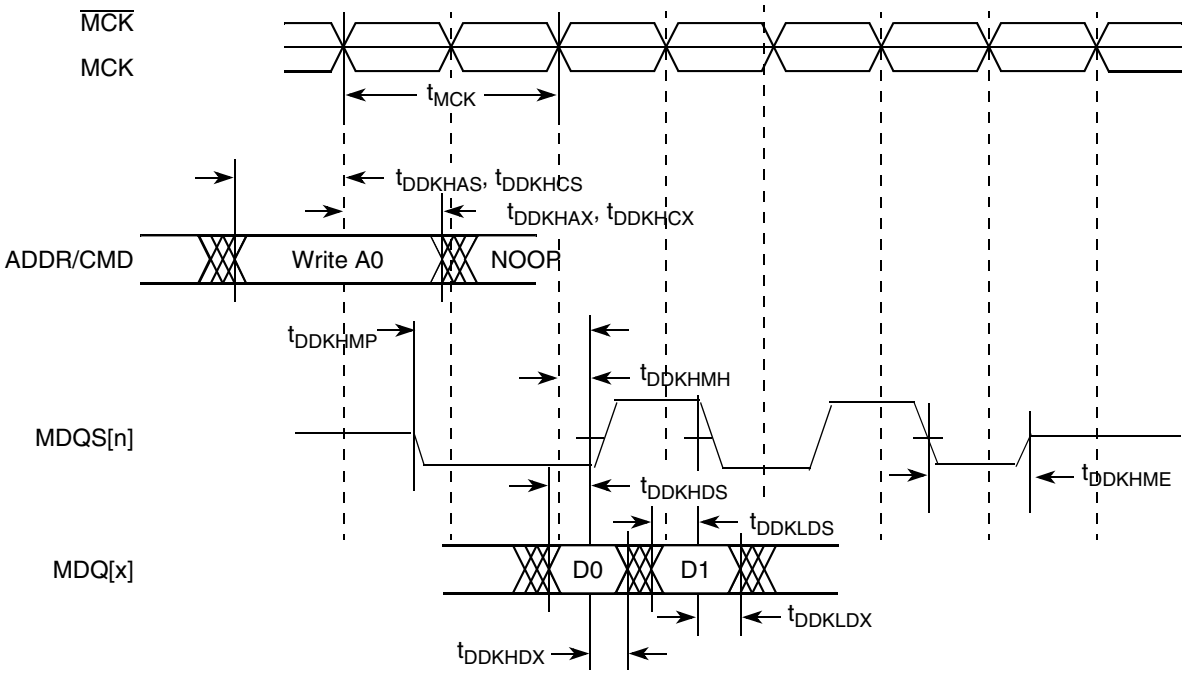

Figure 10. DDR2 and DDR3 Output Timing Diagram

The following figure provides the AC test load for the DDR2 and DDR3 controller bus.

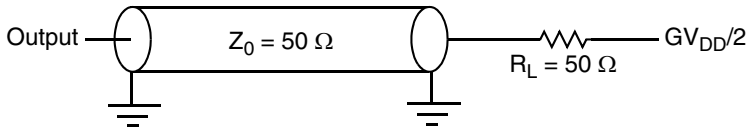

Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.5 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8569E.

2.5.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.5.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	—	3

Notes:

1. f_{CCB} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

Table 35. RGMII and RTBI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	6
Rise time (20%–80%)	t_{RGTR}	—	—	1.75	ns	6
Fall time (20%–80%)	t_{RGTF}	—	—	1.75	ns	6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of gigabit ethernet reference clock by more than 300 ppm.
6. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1.3	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

Table 46. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol[1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock high Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock high Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

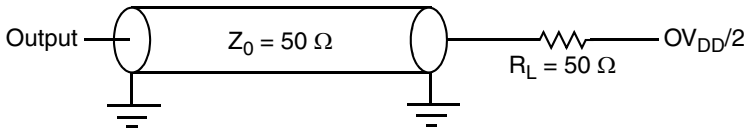

Figure 35. AC Test Load

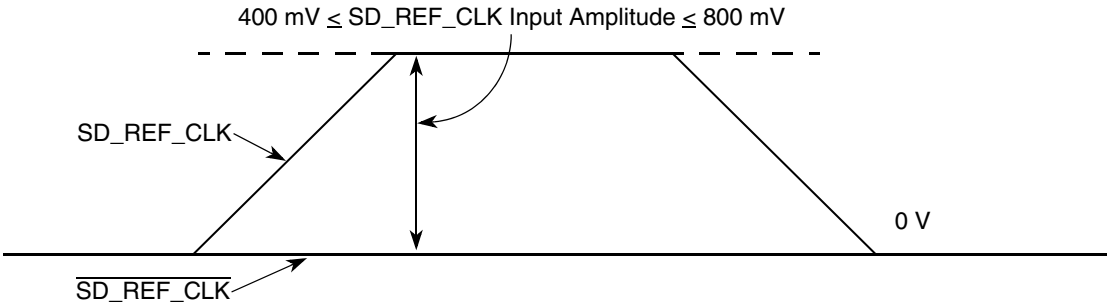

Figure 42. Single-Ended Reference Clock Input DC Requirements

2.9.2.4 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express, SGMII, and Serial RapidIO SerDes reference clocks to be guaranteed by the customer's application design.

Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2, 7
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3, 7

2.10.4 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

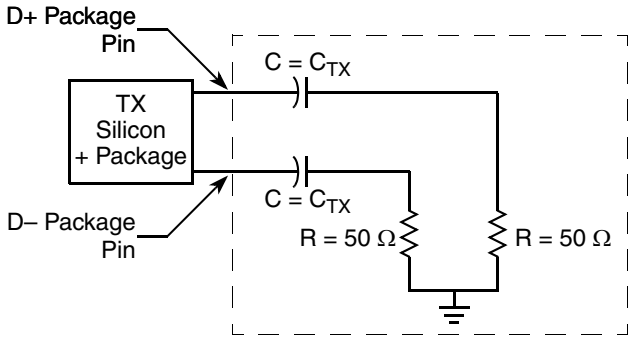

Figure 46. Compliance Test/Measurement Load

2.11 Serial RapidIO (SRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the MPC8569E, for the LP-serial physical layer. The electrical specifications cover both single- and multiple-lane links. Two transmitters (short and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short- and long-run transmitter specifications.

The short-run transmitter must be used mainly for chip-to-chip connections on either the same printed-circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short-run specification reduce the overall power used by the transceivers.

The long-run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC-coupling at the receiver input must be used.Signal Definitions

2.11.1 Signal Definitions

This section defines terms used in the description and specification of differential signals used by the LP-Serial links. Figure 47 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input

2.13 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.13.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the GPIO interface when operating from a 3.3 V supply

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.13.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

The following figure provides the AC test load for the GPIO.

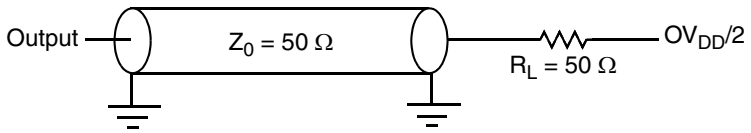

Figure 51. GPIO AC Test Load

The following figure shows the UTOPIA/POS timing with internal clock.

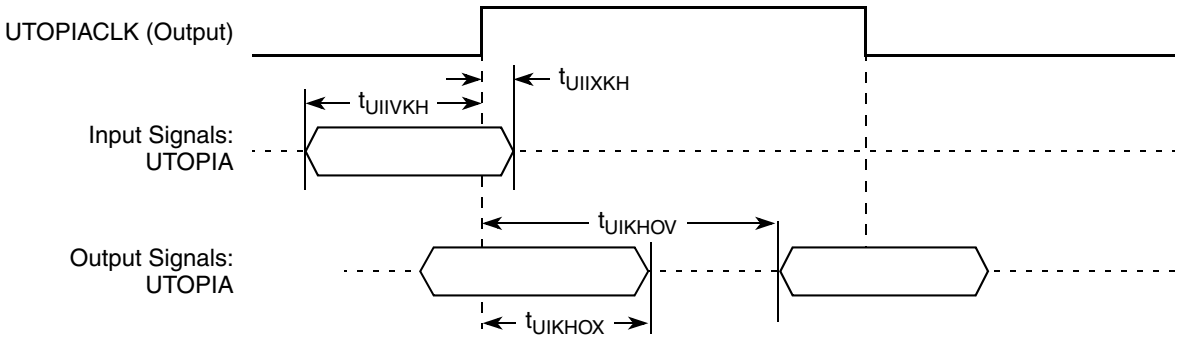

Figure 72. UTOPIA/POS AC Timing (Internal Clock) Diagram

3 Thermal

This section describes the thermal specifications of the MPC8569E.

3.1 Thermal Characteristics

The following table provides the package thermal characteristics of the MPC8569E.

Table 82. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	16	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	12	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	9	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	5	°C/W	3
Junction-to-case thermal	—	$R_{\theta JC}$	1.0	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.2 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.