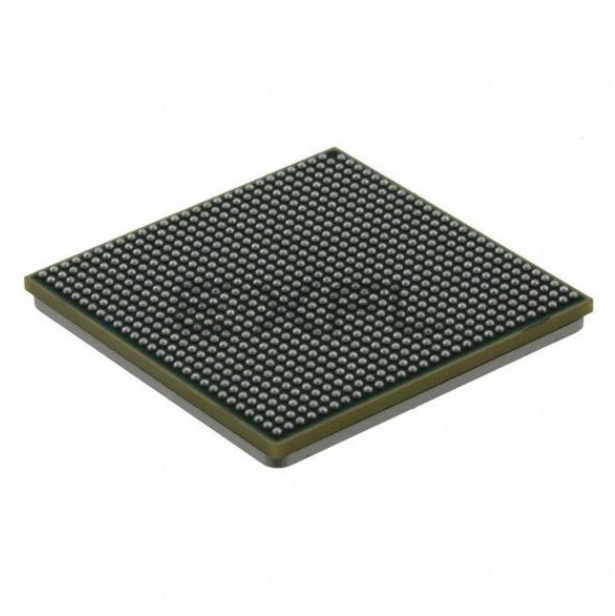

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.067GHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8569cvjaqljb

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

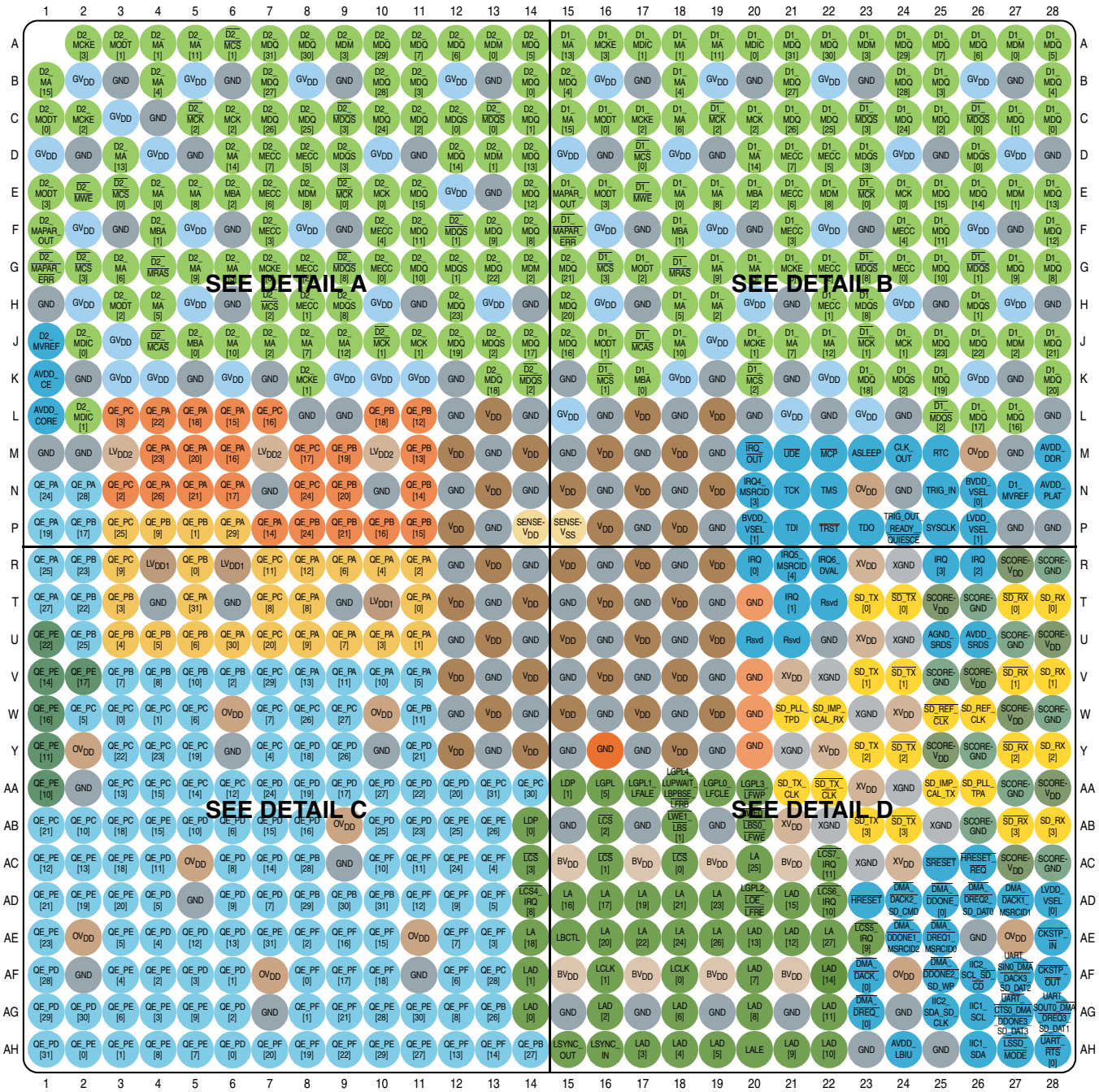


Figure 2. MPC8569E Top View Ballmap

The following figure provides detailed view D of the MPC8569E 783-pin BGA ball map diagram.

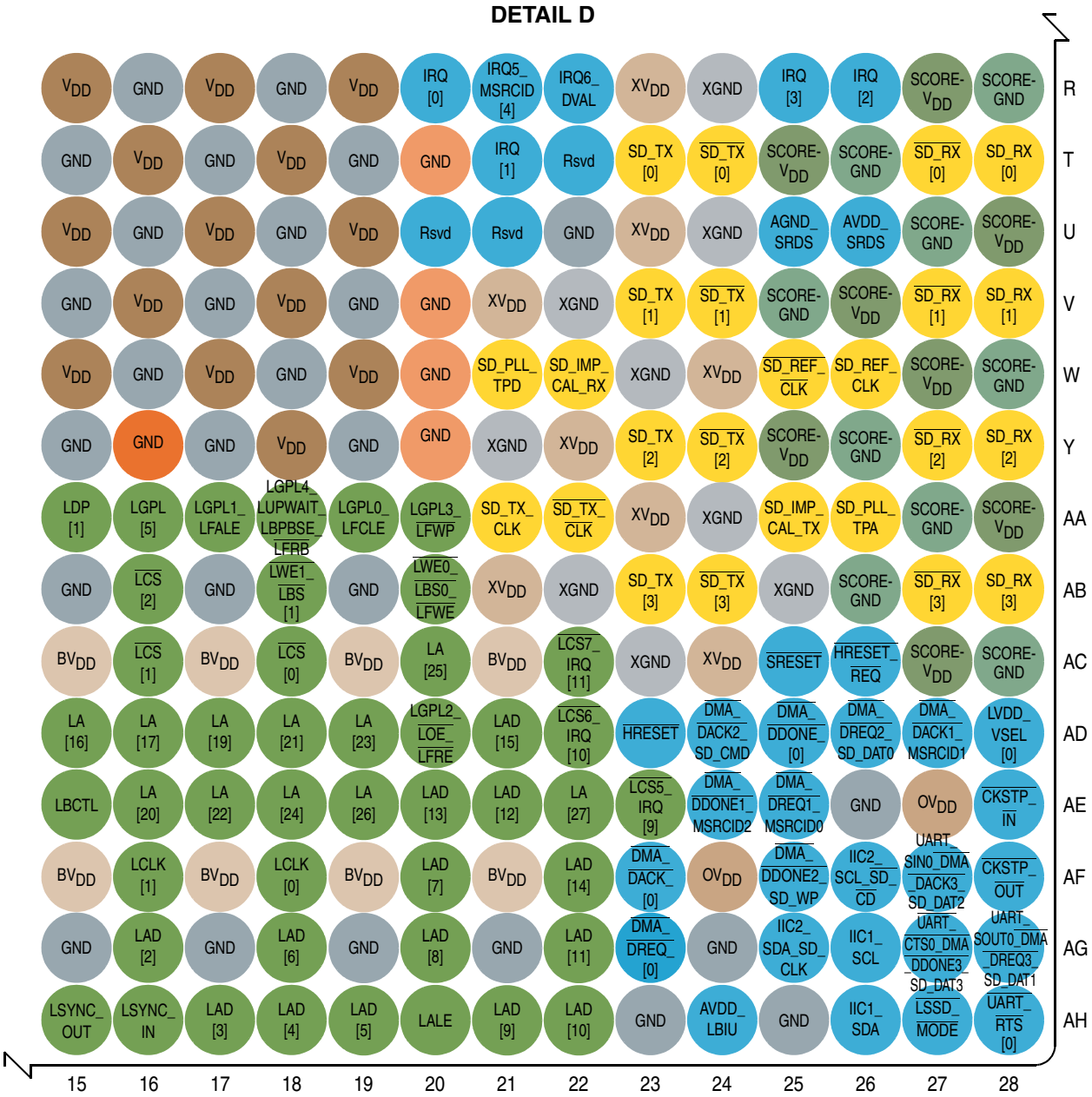


Figure 6. MPC8569E Detail D Ball Map

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MCKE2	C17	O	GV_{DD}	—
D1_MCKE3	A16	O	GV_{DD}	—
$\overline{\text{D1\_MCS0}}$	D17	O	GV_{DD}	—
$\overline{\text{D1\_MCS1}}$	K16	O	GV_{DD}	—
$\overline{\text{D1\_MCS2}}$	K20	O	GV_{DD}	—
$\overline{\text{D1\_MCS3}}$	G16	O	GV_{DD}	—
D1_MDIC0	A20	I/O	GV_{DD}	27
D1_MDIC1	A17	I/O	GV_{DD}	27
D1_MDM0	A27	I/O	GV_{DD}	—
D1_MDM1	E27	I/O	GV_{DD}	—
D1_MDM2	J27	I/O	GV_{DD}	—
D1_MDM3	A23	I/O	GV_{DD}	—
D1_MDM8	E22	I/O	GV_{DD}	—
D1_MDQ0	C28	I/O	GV_{DD}	—
D1_MDQ1	C27	I/O	GV_{DD}	—
D1_MDQ2	C25	I/O	GV_{DD}	—
D1_MDQ3	B25	I/O	GV_{DD}	—
D1_MDQ4	B28	I/O	GV_{DD}	—
D1_MDQ5	A28	I/O	GV_{DD}	—
D1_MDQ6	A26	I/O	GV_{DD}	—
D1_MDQ7	A25	I/O	GV_{DD}	—
D1_MDQ8	G28	I/O	GV_{DD}	—
D1_MDQ9	G27	I/O	GV_{DD}	—
D1_MDQ10	G25	I/O	GV_{DD}	—
D1_MDQ11	F25	I/O	GV_{DD}	—
D1_MDQ12	F28	I/O	GV_{DD}	—
D1_MDQ13	E28	I/O	GV_{DD}	—
D1_MDQ14	E26	I/O	GV_{DD}	—
D1_MDQ15	E25	I/O	GV_{DD}	—
D1_MDQ16	L27	I/O	GV_{DD}	—
D1_MDQ17	L26	I/O	GV_{DD}	—
D1_MDQ18	K23	I/O	GV_{DD}	—
D1_MDQ19	K25	I/O	GV_{DD}	—
D1_MDQ20	K28	I/O	GV_{DD}	—
D1_MDQ21	J28	I/O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
Power Management				
ASLEEP	M23	O	OV_{DD}	11
Thermal Management				
THERM0	U21	—	Internal temperature diode cathode	32
THERM1	U20	—	Internal temperature diode anode	32
Reserved	T22	—	—	9
Analog				
D1_MVREF	N27	Reference voltage for DDR	MV_{REF}	—
D2_MVREF	J1			—
Power and Ground				
V_{DD}	L13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	L19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M14	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M16	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	M18	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N13	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N15	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N17	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	N19	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P12	1.0-V/1.1-V core power supply	V_{DD}	—
V_{DD}	P16	1.0-V/1.1-V core power supply	V_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
GND	N16	—	—	—
GND	N18	—	—	—
GND	N24	—	—	—
GND	N7	—	—	—
GND	P13	—	—	—
GND	P17	—	—	—
GND	P19	—	—	—
GND	P27	—	—	—
GND	P28	—	—	—
GND	R12	—	—	—
GND	R14	—	—	—
GND	R16	—	—	—
GND	R18	—	—	—
GND	T13	—	—	—
GND	T15	—	—	—
GND	T17	—	—	—
GND	T19	—	—	—
GND	T4	—	—	—
GND	T6	—	—	—
GND	T9	—	—	—
GND	U12	—	—	—
GND	U14	—	—	—
GND	U16	—	—	—
GND	U18	—	—	—
GND	U22	—	—	—
GND	V13	—	—	—
GND	V15	—	—	—
GND	V17	—	—	—
GND	V19	—	—	—
GND	W12	—	—	—
GND	W14	—	—	—
GND	W16	—	—	—
GND	W18	—	—	—
GND	Y6	—	—	—
GND	Y10	—	—	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
XGND	U24	SerDes Transceiver Pad GND	—	—
XGND	V22	SerDes Transceiver Pad GND	—	—
XGND	W23	SerDes Transceiver Pad GND	—	—
XGND	Y21	SerDes Transceiver Pad GND	—	—
AGND_SRDS	U25	SerDes PLL GND	—	—

Notes:

1. All multiplexed signals are listed only once and do not reoccur.
2. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed.
3. When configured as I2C, this pin is an open drain signal and recommend a pull-up resistor (1 kΩ) be placed on this pin to OV_{DD}. When configured as SD, this pin is not open drain and does not require a pull-up.
4. This pin has a weak internal pull-up resistor (~20 kΩ).
5. This pin is an open drain signal.
6. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
7. This pin requires a 200-Ω pull-down to ground.
8. Do not connect.
9. Recommend a weak pull-down resistor (2–10 kΩ) be placed on this pin to GND.
10. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.
11. These pins must not be pulled down during power-on reset.
12. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for the required PLL filters to be attached to the AV_{DD} pin.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. This pin selects the voltage of eLBC interface (BV_{DD}). This pin has internal weak pull down.
15. This pin selects the voltage of UCC1 and UCC3 interfaces ($LV_{DD}1$). This pin has internal weak pull down.
16. This pin selects the voltage of UCC2 and UCC4 interfaces ($LV_{DD}2$). This pin has internal weak pull down.
17. This pin requires a 100-Ω pull down to ground.
18. The value of LA[24:27] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
19. The value of QE_PE[27:29] during reset sets the DDR clock PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
20. The value of LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
21. The value of $\overline{\text{LCS}}$[3:7] at reset sets the QE PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
22. The value of QE_PB[27:28], QE_PC4 and QE_PD4 at reset sets the Boot ROM location. These pins require 4.7-kΩ pull up or pull down resistors. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for details
23. These pins are sampled at reset for general-purpose configuration use by software. The value of LAD[0:15] at reset sets the upper 16 bits of the GPPORCR
24. These pins must not be pulled up during power-on reset.
25. This output is actively driven during reset rather than being three-stated during reset.

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Range	Unit	Notes
QUICC Engine block Ethernet interface I/O voltage		$LV_{DD}2$	–0.3 to 3.63 –0.3 to 2.75	V	—
Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Enhanced local bus I/O voltage		BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 3
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	—
	Ethernet signals	LV_{IN}	–0.3 to ($LV_{DD}n$ + 0.3)	V	3
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	3
	Debug, DMA, DUART, PIC, I^2C, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	SerDes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)V_{IN} must not exceed (B,G,L,O,X)V_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

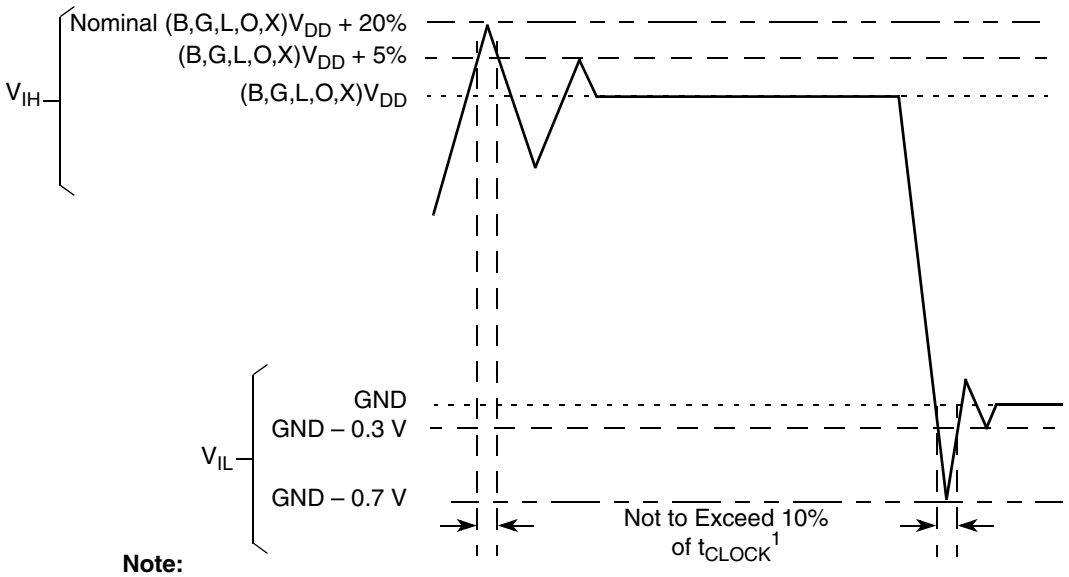
2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 30 mV 1.1 V ± 33 mV	V	1
PLL supply voltage	AV_{DD}_CORE, AV_{DD}_DDR, AV_{DD}_LBIU, AV_{DD}_PLAT, AV_{DD}_QE, AV_{DD}_SRDS	1.0 V ± 30 mV 1.1 V ± 33 mV	V	2

The following figure shows the undershoot and overshoot voltages at the interfaces of the MPC8569E.



Note:

1. Note that t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references Dn_MCK.
   For eLBC, t_{CLOCK} references LCLKn
   For eLBC, t_{CLOCK} references LCLKn
   For SerDes XV_{DD}, t_{CLOCK} references SD_REF_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/XV_{DD}$

The core voltage must always be provided at nominal 1.0 or 1.1 V. See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. $(B,M,L,O)V_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 and DDR3 SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MVREF signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.8 electrical signaling standard for DDR2 or 1.5-V electrical signaling for DDR3. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

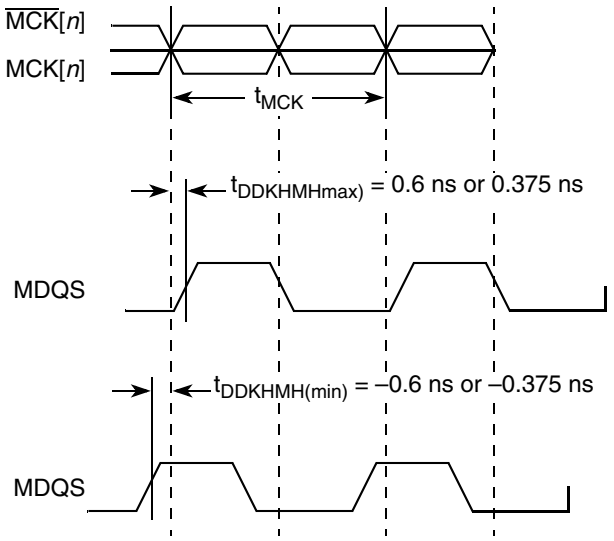


Figure 9. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

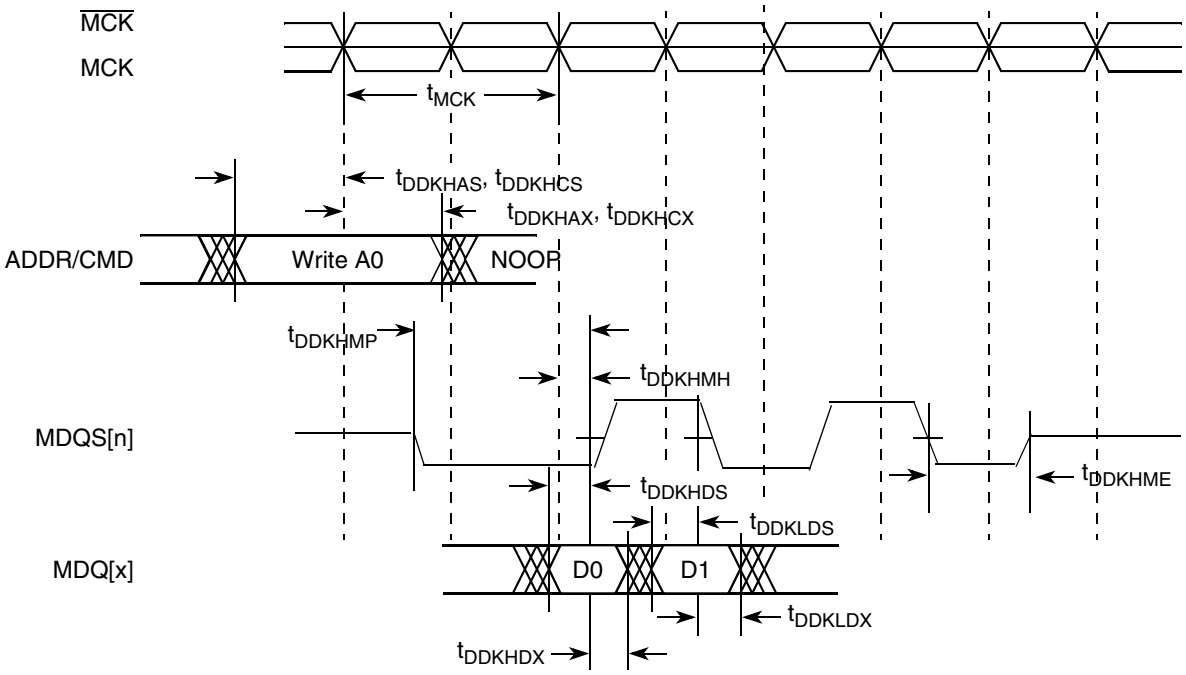


Figure 10. DDR2 and DDR3 Output Timing Diagram

The following figure provides the AC test load for the DDR2 and DDR3 controller bus.

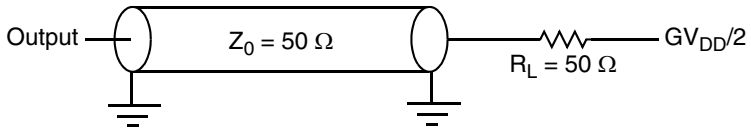


Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.5 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8569E.

2.5.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.5.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Value	Unit	Notes
Minimum baud rate	f_{CCB}/1,048,576	baud	1
Maximum baud rate	f_{CCB}/16	baud	1, 2
Oversample rate	16	—	3

Notes:

1. f_{CCB} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.6.3.6 TBI Single-Clock Mode AC Specifications

The following table shows the TBI single-clock mode receive AC timing specifications.

Table 34. TBI Single-Clock Mode Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Note
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	1
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	2
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	2
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	—	ns	2
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	—	ns	2
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

Note:

1. The frequency of RX_CLK should not exceed the frequency of gigabit Ethernet reference clock by more than 300 ppm.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure shows the TBI single-clock mode receive AC timing diagram.

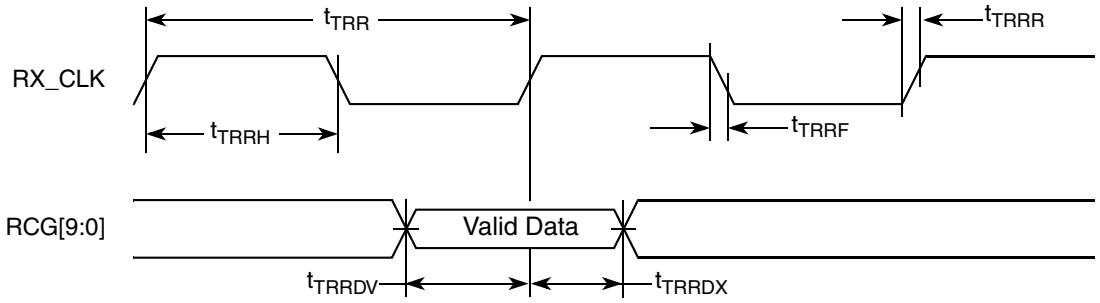


Figure 25. TBI Single-Clock Mode Receive AC Timing Diagram

2.6.3.7 RGMII and RTBI AC Timing Specifications

The following table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.2	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4, 6

The following figure shows the data and command input AC timing diagram.

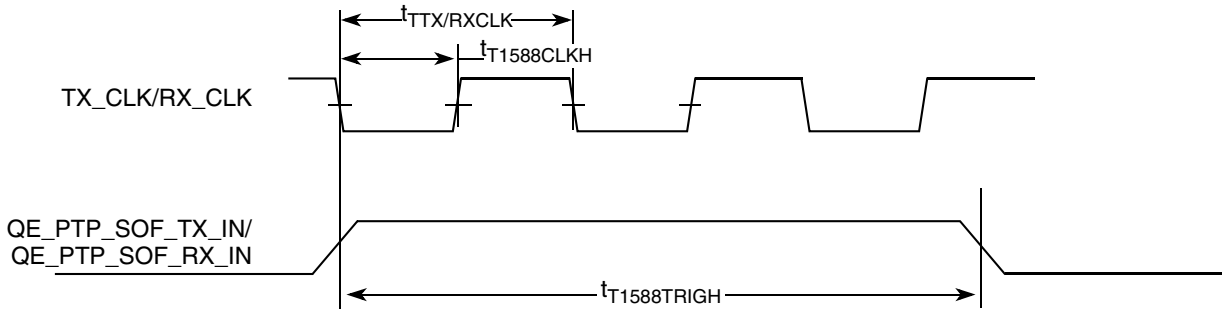


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

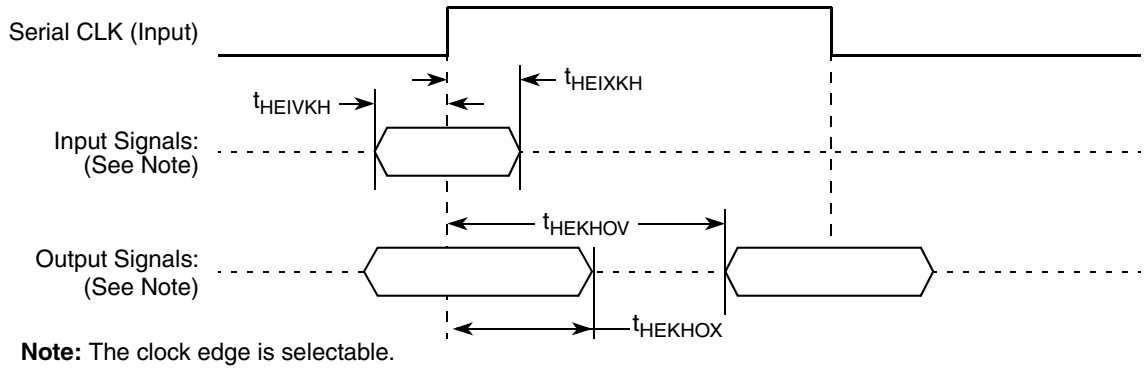
Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

Figure 36 and Figure 37 represent the AC timing from Table 45 and Table 46. Note that although the specifications generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also note that the clock edge is selectable.

The following figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 36. AC Timing (External Clock) Diagram

The following figure shows the timing with internal clock.

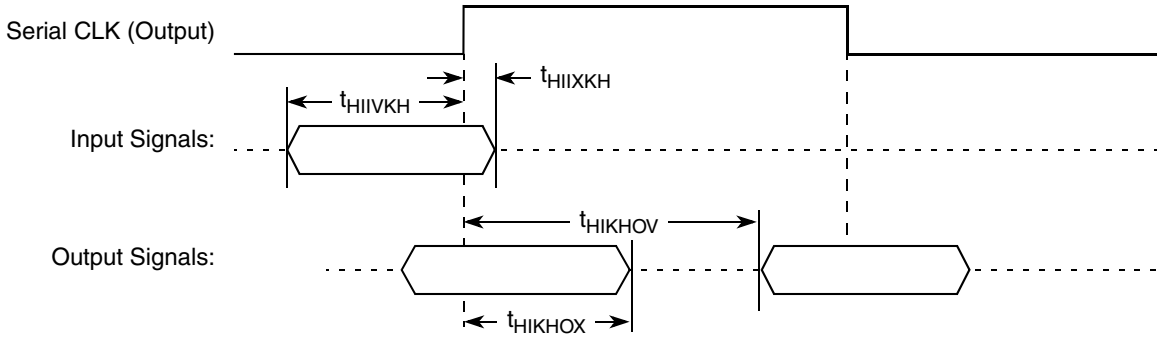


Figure 37. AC Timing (Internal Clock) Diagram

2.9 High-Speed SerDes Interfaces (HSSI)

The MPC859E features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications.The SerDes interface can be used for PCI Express and/or Serial RapidIO and/or SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

The below figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. The following figure shows the waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

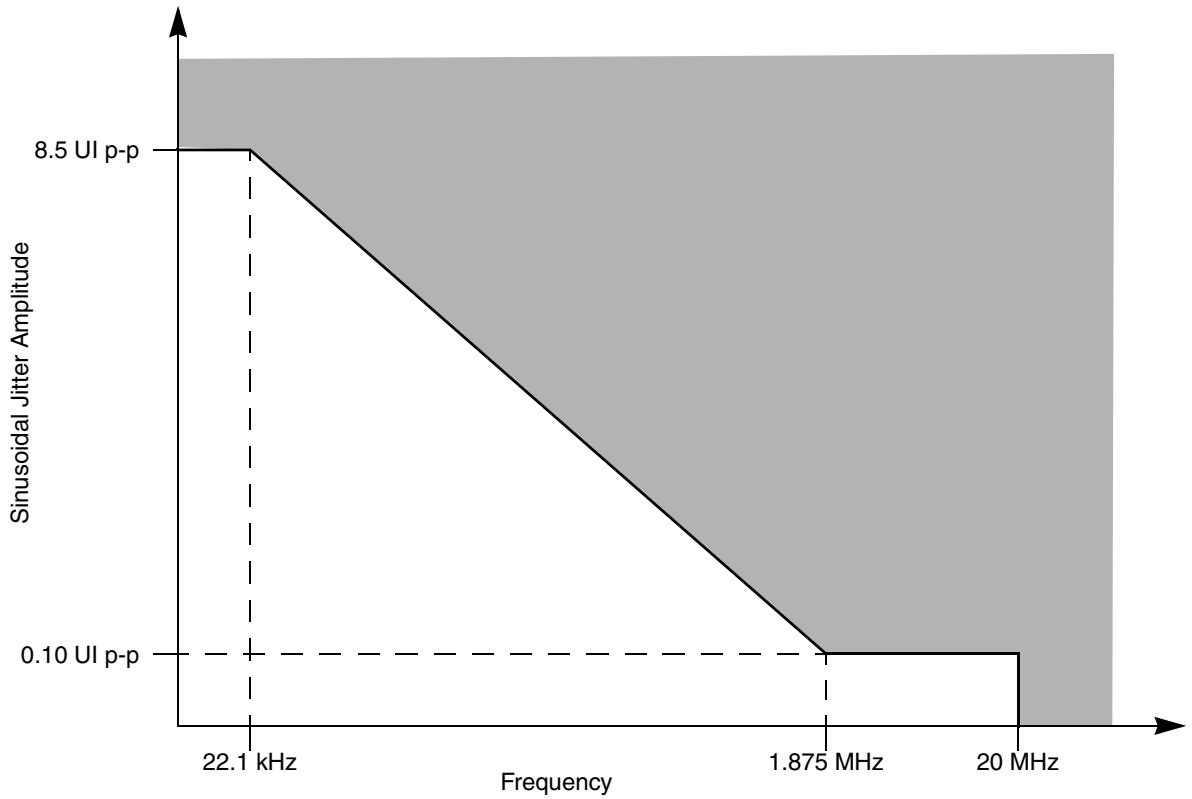


Figure 48. Single Frequency Sinusoidal Jitter Limits

2.12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8569E.

2.12.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface.

Table 57. I²C DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2

2.13 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.13.1 GPIO DC Electrical Characteristics

The following table provides the DC electrical characteristics for the GPIO interface when operating from a 3.3 V supply

Table 59. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.13.2 GPIO AC Timing Specifications

The following table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs must be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

The following figure provides the AC test load for the GPIO.

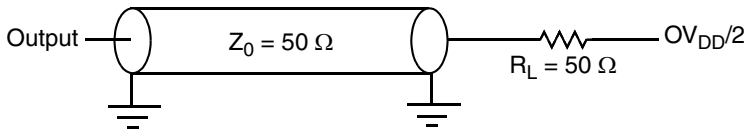


Figure 51. GPIO AC Test Load

2.15.2.2 Enhanced Local Bus AC Timing Specifications for PLL Enable Mode

For PLL enable mode, all timings are relative to the rising edge of LSYNC_IN.

The following table describes the timing specifications of the enhanced local bus interface at BV_{DD} = 3.3 V, 2.5 V and 1.8 V for PLL enable mode.

Table 66. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V 2.5 V and 1.8 V) —PLL Enabled Mode

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
Enhanced local bus cycle time	t_{LBK}	7.5	12	ns	—
Enhanced local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	5
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	680	ps	2
Input setup	t_{LBIVKH}	2	—	ns	—
Input hold	t_{LBIXKH}	1.0	—	ns	—
Output delay (Except LALE)	t_{LBKHOV}	—	3.8	ns	—
Output hold (Except LALE)	t_{LBKHOX}	0.6	—	ns	—
Enhanced local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	1 – 0.475 ns (LBCR[AHD]=0) ½ – 0.475 ns (LBCR[AHD] = 1)	—	eLBC controller clock cycle (= 1 platform clock cycle in ns)	4

Notes:

1. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle. The eLBC controller clock refers to the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

2.18.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 73. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.19 SPI Interface

This section describes the SPI DC and AC electrical specifications of the MPC8569E.

2.19.1 SPI DC Electrical Characteristics

The following table provides the SPI DC electrical characteristics.

Table 74. SPI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 75. SPI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	9	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2

3.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in the following figure. The heat sink must be attached to the printed-circuit board with the spring force centered over the package. This spring force should not exceed 10 pounds force (45 Newtons).

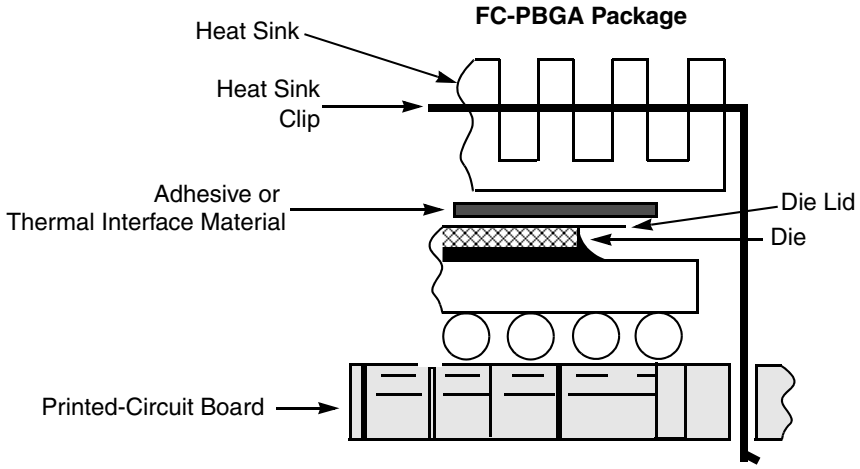


Figure 73. Package Exploded Cross-Sectional View

The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.3.1 Internal Package Conduction Resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

5 Ordering Information

Contact your local Freescale sales office or regional marketing team for ordering information.

Ordering information for the parts fully covered by this specification document is provided in Section 5.1, "Part Numbers Fully Addressed by This Document."

5.1 Part Numbers Fully Addressed by This Document

The following table shows the device nomenclature.

Table 84. Device Nomenclature

MPC	nnnn	E	C	Vx	AA	X	G	R
Product Code[1]	**Part Identifier**	**Security Engine**	**Temperature Range**	**Package** [2]	**Processor Frequency** [3]	**DDR Frequency**[4]	**QE Frequency**	**Revision Level**
MPC PPC	8569	E = included	Blank = 0° to 105°C C = –40° to 105°C	VT = FC-PBGA, Pb free, C5 spheres VJ = FC-PBGA, Pb free C4 bumps and pb free C5 spheres	AN = 800 MHz AQ = 1067 MHz AU = 1333 MHz	K = 600 MHz L = 667 MHz N = 800 MHz	G = 400 MHz J = 533 MHz L = 667 MHz	Blank = Rev. 1.0 (SVR = 0x8088_0010 A = Rev. 2.0 (SVR = 0x8088_0020 B = Rev. 2.1 (SVR = 0x8088_0021
		Blank = not included						A = Rev. 2.0 (SVR = 0x8080_0020 B = Rev. 2.1 (SVR = 0x8080_0021

Notes:

1. MPC stands for "qualified." PPC stands for pre-production samples.
2. See Section 4, "Package Description," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
4. See Table 85 for the corresponding maximum platform frequency.
5. C5 spheres are used by customer to attach to pcb. C4 bumps are bumps used on die of the device to connect between die and package substrate.