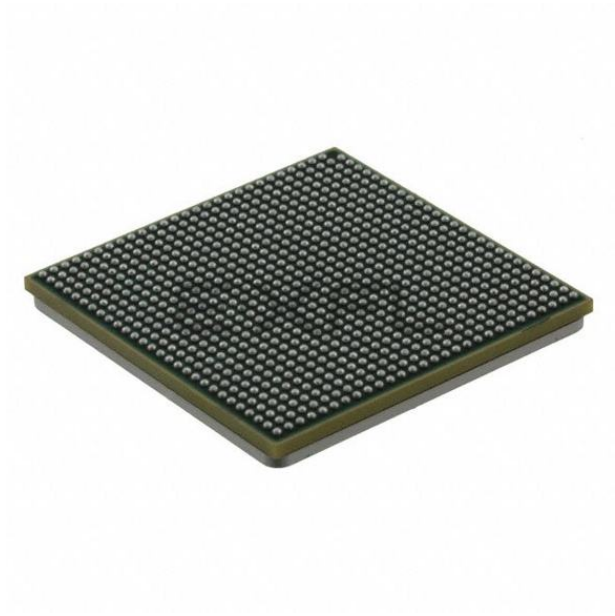


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2, DDR3, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (8), 1Gbps (4)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.0V, 1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569cvtankgb

NOTE

The MPC8569E is also available without a security engine in a configuration known as the MPC8569. All specifications other than those relating to security apply to the MPC8569 exactly as described in this document.

The following figure shows the major functional units within the MPC8569E.

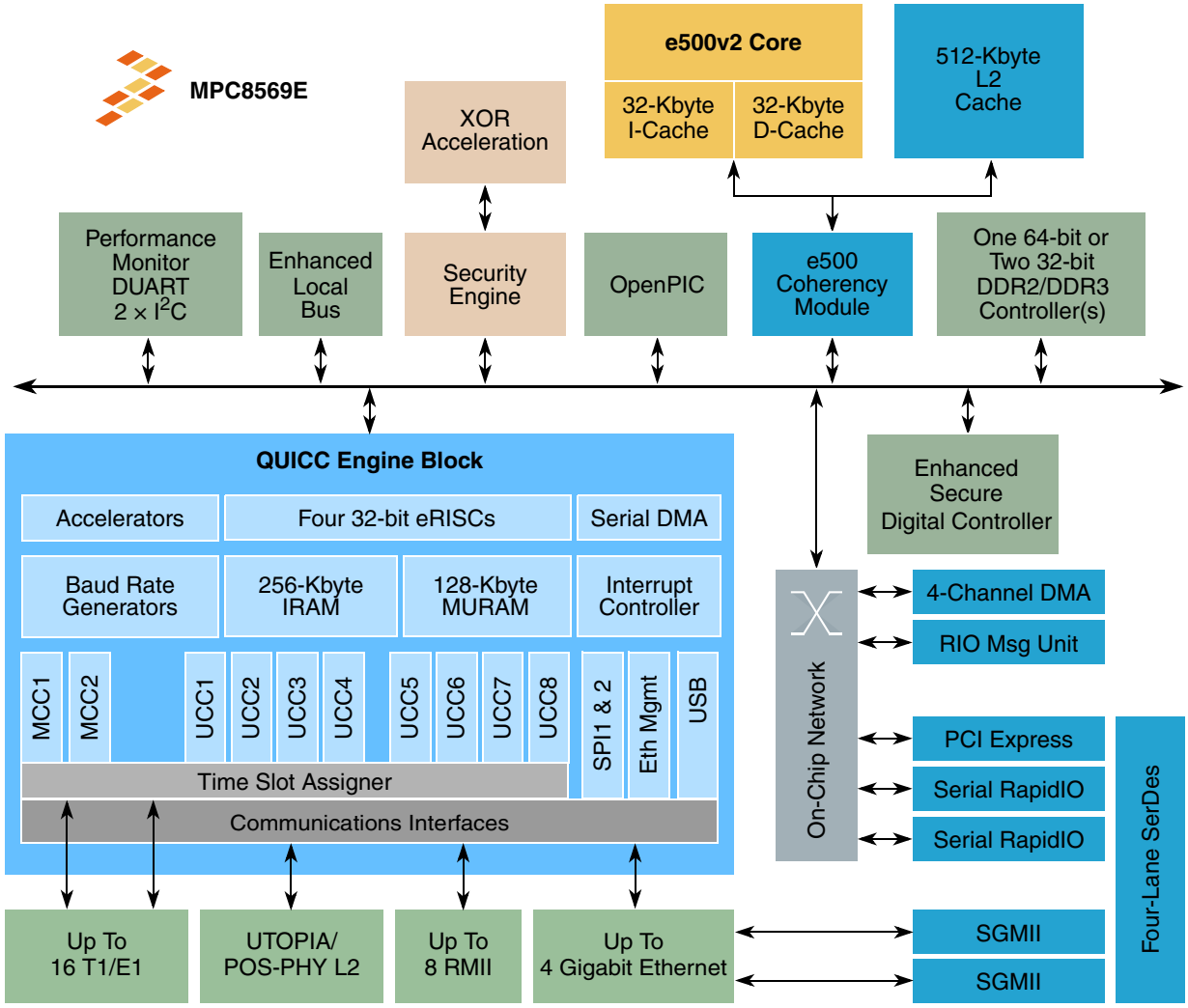


Figure 1. MPC8569E Block Diagram

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figure shows the top view of the MPC8569E 783-pin BGA ball map diagram.

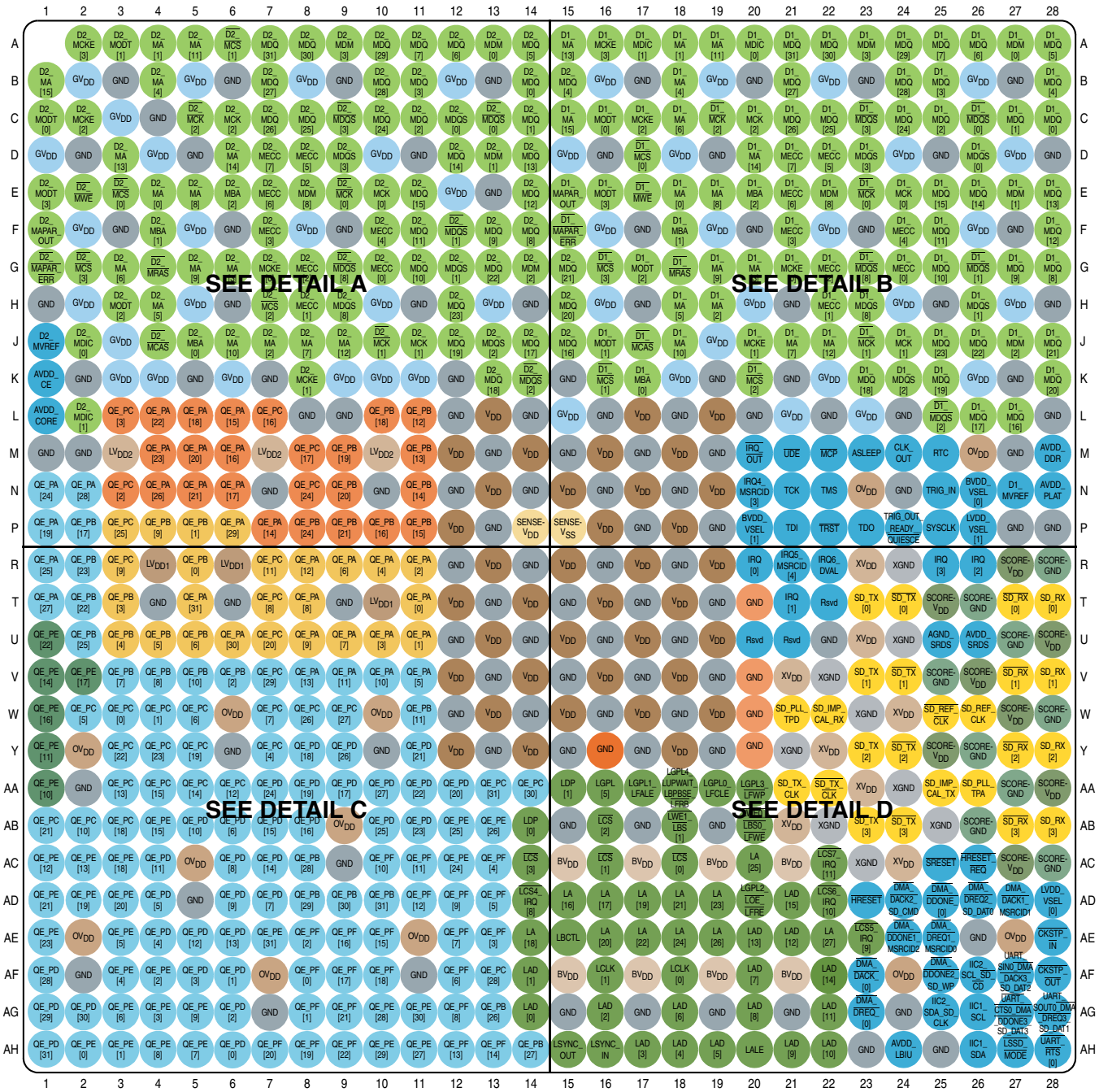


Figure 2. MPC8569E Top View Ballmap

The following figure provides detailed view D of the MPC8569E 783-pin BGA ball map diagram.

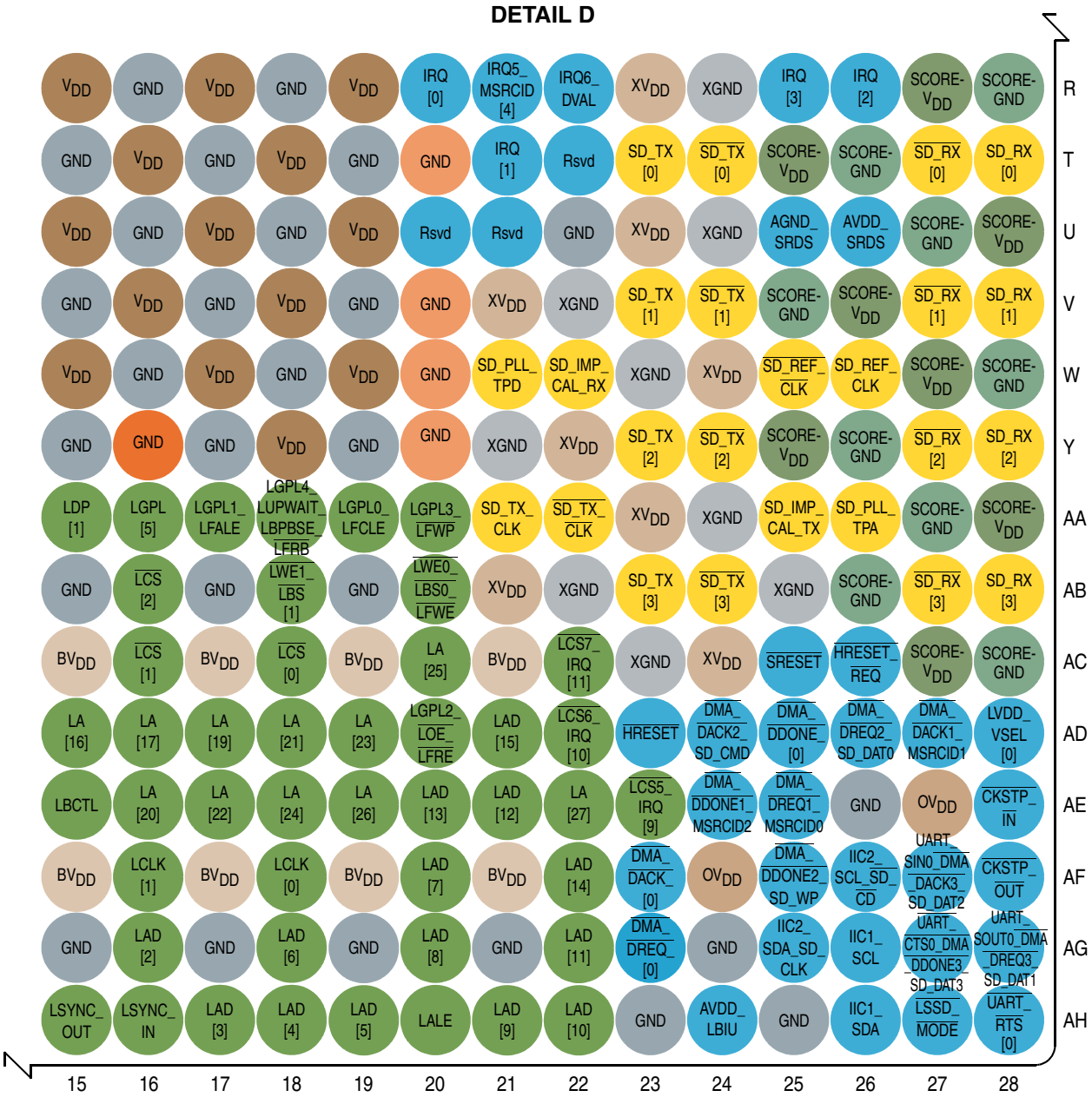


Figure 6. MPC8569E Detail D Ball Map

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
D1_MDQ22	J26	I/O	GV_{DD}	—
D1_MDQ23	J25	I/O	GV_{DD}	—
D1_MDQ24	C24	I/O	GV_{DD}	—
D1_MDQ25	C22	I/O	GV_{DD}	—
D1_MDQ26	C21	I/O	GV_{DD}	—
D1_MDQ27	B21	I/O	GV_{DD}	—
D1_MDQ28	B24	I/O	GV_{DD}	—
D1_MDQ29	A24	I/O	GV_{DD}	—
D1_MDQ30	A22	I/O	GV_{DD}	—
D1_MDQ31	A21	I/O	GV_{DD}	—
D1_MDQS0	D26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	C26	I/O	GV_{DD}	—
D1_MDQS1	H26	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	G26	I/O	GV_{DD}	—
D1_MDQS2	K24	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	L25	I/O	GV_{DD}	—
D1_MDQS3	D23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	C23	I/O	GV_{DD}	—
D1_MDQS8	H23	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS8}}$	G23	I/O	GV_{DD}	—
D1_MECC0	G24	I/O	GV_{DD}	—
D1_MECC1	H22	I/O	GV_{DD}	—
D1_MECC2	G22	I/O	GV_{DD}	—
D1_MECC3	F21	I/O	GV_{DD}	—
D1_MECC4	F24	I/O	GV_{DD}	—
D1_MECC5	D22	I/O	GV_{DD}	—
D1_MECC6	E21	I/O	GV_{DD}	—
D1_MECC7	D21	I/O	GV_{DD}	—
D1_MODT0	C16	O	GV_{DD}	—
D1_MODT1	J16	O	GV_{DD}	—
D1_MODT2	G17	O	GV_{DD}	—
D1_MODT3	E16	O	GV_{DD}	—
D1_MAPAR_OUT	E15	O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	F15	I	GV_{DD}	—
$\overline{\text{D1\_MRAS}}$	G18	O	GV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PA19	P1	I/O	OV_{DD}	—
QE_PA20	M5	I/O	$LV_{DD}2$	—
QE_PA21	N5	I/O	$LV_{DD}2$	—
QE_PA22	L4	I/O	$LV_{DD}2$	—
QE_PA23	M4	I/O	$LV_{DD}2$	—
QE_PA24	N1	I/O	OV_{DD}	—
QE_PA25	R1	I/O	OV_{DD}	—
QE_PA26	N4	I/O	$LV_{DD}2$	—
QE_PA27	T1	I/O	OV_{DD}	—
QE_PA28	N2	I/O	OV_{DD}	—
QE_PA29	P6	I/O	$LV_{DD}1$	—
QE_PA30	U6	I/O	$LV_{DD}1$	—
QE_PA31	T5	I/O	$LV_{DD}1$	—
QE_PB0	R5	I/O	$LV_{DD}1$	—
QE_PB1	P5	I/O	$LV_{DD}1$	—
QE_PB2	V6	I/O	OV_{DD}	—
QE_PB3	T3	I/O	$LV_{DD}1$	—
QE_PB4	U3	I/O	$LV_{DD}1$	—
QE_PB5	U4	I/O	$LV_{DD}1$	—
QE_PB6	U5	I/O	$LV_{DD}1$	—
QE_PB7	V3	I/O	OV_{DD}	11
QE_PB8	V4	I/O	OV_{DD}	—
QE_PB9	P4	I/O	$LV_{DD}1$	—
QE_PB10	V5	I/O	OV_{DD}	—
QE_PB11	W11	I/O	OV_{DD}	—
QE_PB12	L11	I/O	$LV_{DD}2$	—
QE_PB13	M11	I/O	$LV_{DD}2$	—
QE_PB14	N11	I/O	$LV_{DD}2$	—
QE_PB15	P11	I/O	$LV_{DD}2$	—
QE_PB16	P10	I/O	$LV_{DD}2$	—
QE_PB17	P2	I/O	OV_{DD}	—
QE_PB18	L10	I/O	$LV_{DD}2$	—
QE_PB19	M9	I/O	$LV_{DD}2$	—
QE_PB20	N9	I/O	$LV_{DD}2$	—
QE_PB21	P9	I/O	$LV_{DD}2$	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
QE_PC25	P3	I/O	$LV_{DD}1$	—
QE_PC26	W8	I/O	OV_{DD}	—
QE_PC27	W9	I/O	OV_{DD}	—
QE_PC28	AF13	I/O	OV_{DD}	—
QE_PC29	V7	I/O	OV_{DD}	—
QE_PC30	AA14	I/O	OV_{DD}	—
QE_PC31	AA13	I/O	OV_{DD}	—
QE_PD0	AH6	I/O	OV_{DD}	11
QE_PD1	AF6	I/O	OV_{DD}	—
QE_PD2	AG6	I/O	OV_{DD}	—
QE_PD3	AF5	I/O	OV_{DD}	—
QE_PD4	AE4	I/O	OV_{DD}	22
QE_PD5	AD4	I/O	OV_{DD}	—
QE_PD6	AB6	I/O	OV_{DD}	—
QE_PD7	AD7	I/O	OV_{DD}	—
QE_PD8	AC6	I/O	OV_{DD}	—
QE_PD9	AD6	I/O	OV_{DD}	—
QE_PD10	AB5	I/O	OV_{DD}	—
QE_PD11	AC4	I/O	OV_{DD}	—
QE_PD12	AE5	I/O	OV_{DD}	—
QE_PD13	AE6	I/O	OV_{DD}	—
QE_PD14	AC7	I/O	OV_{DD}	—
QE_PD15	AB7	I/O	OV_{DD}	—
QE_PD16	AB8	I/O	OV_{DD}	—
QE_PD17	AA9	I/O	OV_{DD}	—
QE_PD18	Y8	I/O	OV_{DD}	—
QE_PD19	AA8	I/O	OV_{DD}	—
QE_PD20	AA12	I/O	OV_{DD}	—
QE_PD21	Y11	I/O	OV_{DD}	—
QE_PD22	AA11	I/O	OV_{DD}	—
QE_PD23	AB11	I/O	OV_{DD}	—
QE_PD24	AA7	I/O	OV_{DD}	—
QE_PD25	AB10	I/O	OV_{DD}	—
QE_PD26	Y9	I/O	OV_{DD}	—
QE_PD27	AA10	I/O	OV_{DD}	—

Table 1. MPC8569E Pinout Listing (continued)

Signal[1]	Package Pin Number	Pin Type	Power Supply	Note
SD_RX0	T28	I	ScoreVDD	30
$\overline{\text{SD\_RX0}}$	T27	I	ScoreVDD	30
SD_RX1	V28	I	ScoreVDD	30
$\overline{\text{SD\_RX1}}$	V27	I	ScoreVDD	30
SD_RX2	Y28	I	ScoreVDD	30
$\overline{\text{SD\_RX2}}$	Y27	I	ScoreVDD	30
SD_RX3	AB28	I	ScoreVDD	30
$\overline{\text{SD\_RX3}}$	AB27	I	ScoreVDD	30
SD_TX0	T23	O	XV_{DD}	31
$\overline{\text{SD\_TX0}}$	T24	O	XV_{DD}	31
SD_TX1	V23	O	XV_{DD}	31
$\overline{\text{SD\_TX1}}$	V24	O	XV_{DD}	31
SD_TX2	Y23	O	XV_{DD}	31
$\overline{\text{SD\_TX2}}$	Y24	O	XV_{DD}	31
SD_TX3	AB23	O	XV_{DD}	31
$\overline{\text{SD\_TX3}}$	AB24	O	XV_{DD}	31
SD_TX_CLK	AA21	O	XV_{DD}	8
$\overline{\text{SD\_TX\_CLK}}$	AA22	O	XV_{DD}	8
System Control				
$\overline{\text{CKSTP\_IN}}$	AE28	I	OV_{DD}	4
$\overline{\text{CKSTP\_OUT}}$	AF28	O	OV_{DD}	5, 6, 11
$\overline{\text{HRESET}}$	AD23	I	OV_{DD}	4
$\overline{\text{HRESET\_REQ}}$	AC26	O	OV_{DD}	11
$\overline{\text{SRESET}}$	AC25	I	OV_{DD}	4
Debug				
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	P24	O	OV_{DD}	11
CLK_OUT	M24	O	OV_{DD}	—
TRIG_IN	N25	I	OV_{DD}	—
Voltage Control				
LVDD_VSEL0	AD28	I	OV_{DD}	15
LVDD_VSEL1	P26	I	OV_{DD}	16
BVDD_VSEL0	N26	I	OV_{DD}	14
BVDD_VSEL1	P20	I	OV_{DD}	14
Design for Test				
$\overline{\text{LSSD\_MODE}}$	AH27	I	OV_{DD}	10

2.4.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.4.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 17. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 533 MHz data rate	V_{ILAC}	—	MVREF*n* – 0.20	V	—
	≤ 533 MHz data rate		—	MVREF*n* – 0.25		
AC input high voltage	> 533 MHz data rate	V_{IHAC}	MVREF*n* + 0.20	—	V	—
	≤ 533 MHz data rate		MVREF*n* + 0.25	—		

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.175	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.175	—	V	—

The following table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 19. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications[3]

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
800 MHz data rate		–200	200		1
667 MHz data rate		–240	240		1
533 MHz data rate		–300	300		1
400 MHz data rate		–365	365		1

Table 19. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications[3] (continued)

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Note
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
800 MHz data rate		–425	425		2
667 MHz data rate		–510	510		2
533 MHz data rate		–635	635		2
400 MHz data rate		–885	885		2

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. Parameters tested in DDR2 mode are to 400, 533, 667, and 800 MHz data rates and in DDR3 mode to 667 and 800 MHz data rates.

The following figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

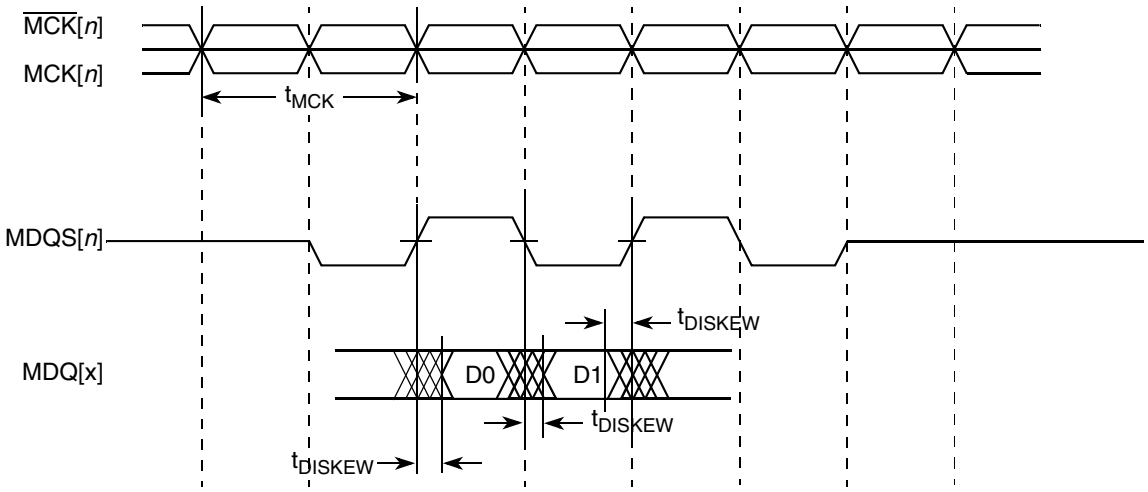


Figure 8. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

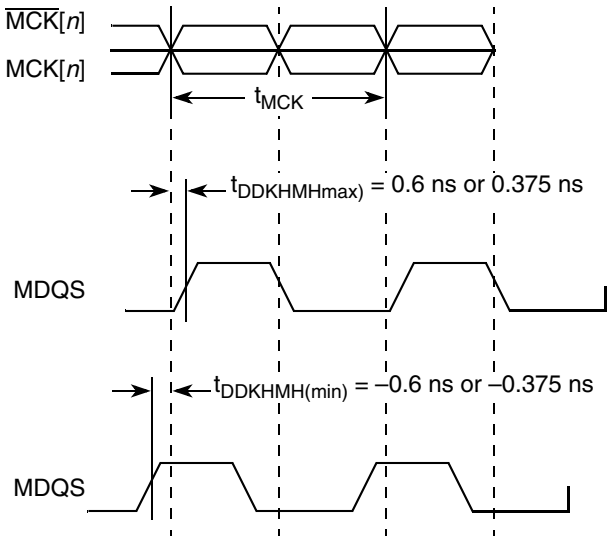


Figure 9. Timing Diagram for t_{DDKHMH}

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

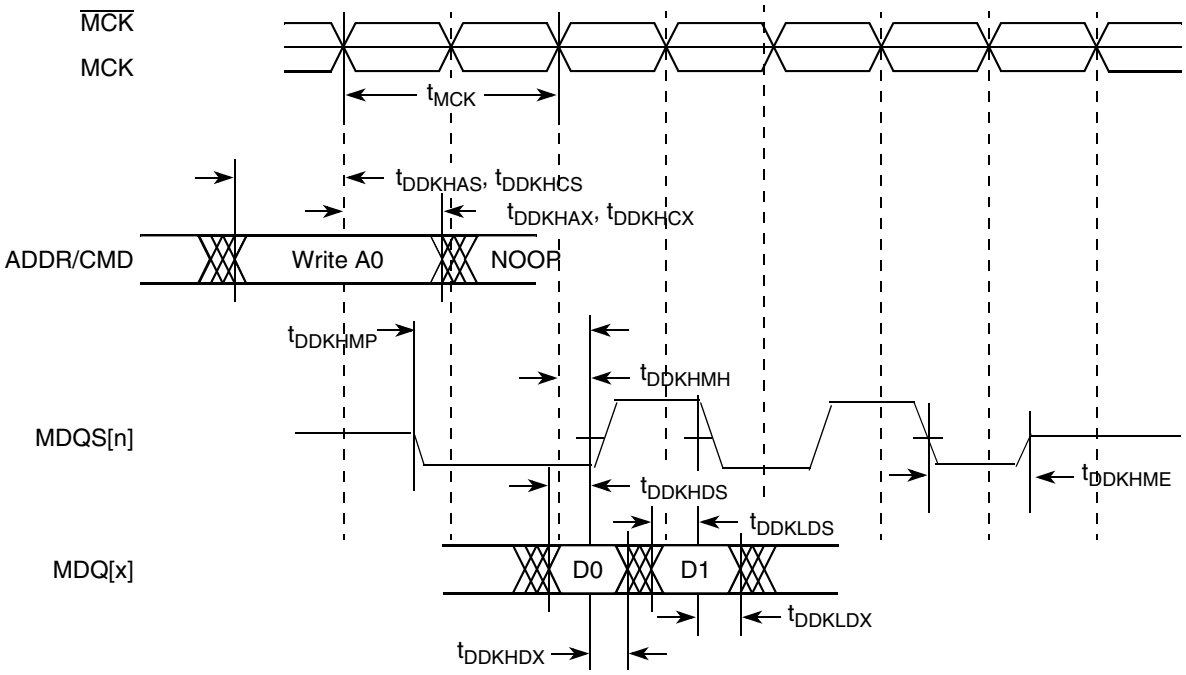


Figure 10. DDR2 and DDR3 Output Timing Diagram

2.6.4.1.2 SGMII Transmit DC Timing Specifications

Table 36 and Table 37 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs, SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*], as shown in Figure 28.

Table 36. SGMII DC Transmitter Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	320.0	500.0	725.0	mV	Equalization setting: 1.0×
		293.8	459.0	665.6		Equalization setting: 1.09×
		266.9	417.0	604.7		Equalization setting: 1.2×
		240.6	376.0	545.2		Equalization setting: 1.33×
		213.1	333.0	482.9		Equalization setting: 1.5×
		186.9	292.0	423.4		Equalization setting: 1.71×
		160.0	250.0	362.5		Equalization setting: 2.0×

2.6.4.1.3 SGMII DC Receiver Electrical Characteristics

The following table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 37. SGMII DC Receiver Electrical Characteristics

At recommended operating conditions with XV_{DD} = 1.0 V ± 3% and 1.1 V ± 3%.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 001	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	LSTS = 100		175	—			
Loss of signal threshold	LSTS = 001	V_{LOS}	30	—	100	mV	3, 4
	LSTS = 100		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See Section 2.10.2, "PCI Express DC Physical Layer Specifications," and Section 2.10.3, "PCI Express AC Physical Layer Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**2** or LSTS**3** bit field of the MPC8569E's SerDes control register SRDSCR4.

2.6.4.2 SGMII AC Timing Specifications

This section discusses the AC timing specifications for the SGMII interface.

2.6.4.2.1 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.9.2.4, "AC Requirements for SerDes Reference Clocks."

The following figure shows the data and command input AC timing diagram.

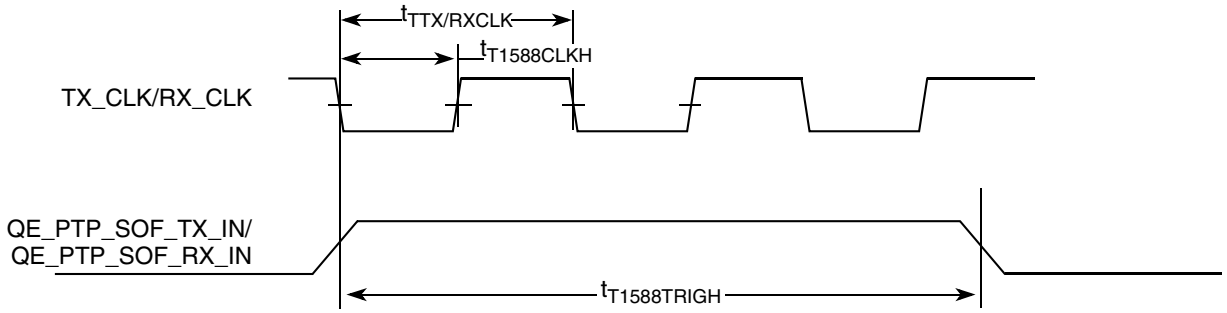


Figure 33. QUICC Engine Block IEEE 1588 Input AC Timing (SOF TRIG)

2.7 Ethernet Management Interface

The electrical characteristics specified in this section apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 2.6, "Ethernet Interface."

2.7.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The following table provides the DC electrical characteristics for MDIO and MDC.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

2.10.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

The following table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 49. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000[2]/ 1100[3]	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential TX impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	TX DC Differential mode Low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required TX D+ as well as D– DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 46 and measured over any 250 consecutive TX UIs.
2. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.0 V
3. Typ-$V_{TX-DIFFp-p}$ with XV_{DD} = 1.1 V

2.10.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 Gb/s

The following table defines the DC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	175	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$. See note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	RX DC Differential mode impedance. See Note 2.

2.11.3 DC Requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.11.3.1 DC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clocks of the SRIO interface are described in Section 2.9.2.3, "DC Level Requirement for SerDes Reference Clocks."

2.11.3.2 DC Serial RapidIO Timing Transmitter Specifications

The LP-serial transmitter electrical and timing specifications are given in the following sections.

The differential return loss, S11, of the transmitter in each case are better than the following:

- –10 dB for (Baud Frequency) ÷ 10 < Freq(f) < 625 MHz
- –10 dB + 10log(f ÷ 625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

The following table defines the serial RapidIO transmitter DC specifications.

Table 53. SRIO Transmitter DC Timing Specifications—1.25, 2.5, and 3.125 GBauds

At recommended operating conditions with XV_{DD} = 1.0 V ± 3%. and 1.1 V ± 3%

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.11.3.3 DC Serial RapidIO Receiver Specifications

The LP-serial receiver electrical and timing specifications are given in the following sections.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (baud frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

2.14 JTAG Controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.14.1 JTAG DC Electrical Characteristics

The following table provides the JTAG DC electrical characteristics.

Table 61. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

The following table provides the JTAG AC timing specifications as defined in Figure 52 through Figure 55.

Table 62. JTAG AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	4
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—

The following figure shows the AC timing diagram for PLL-enabled mode.

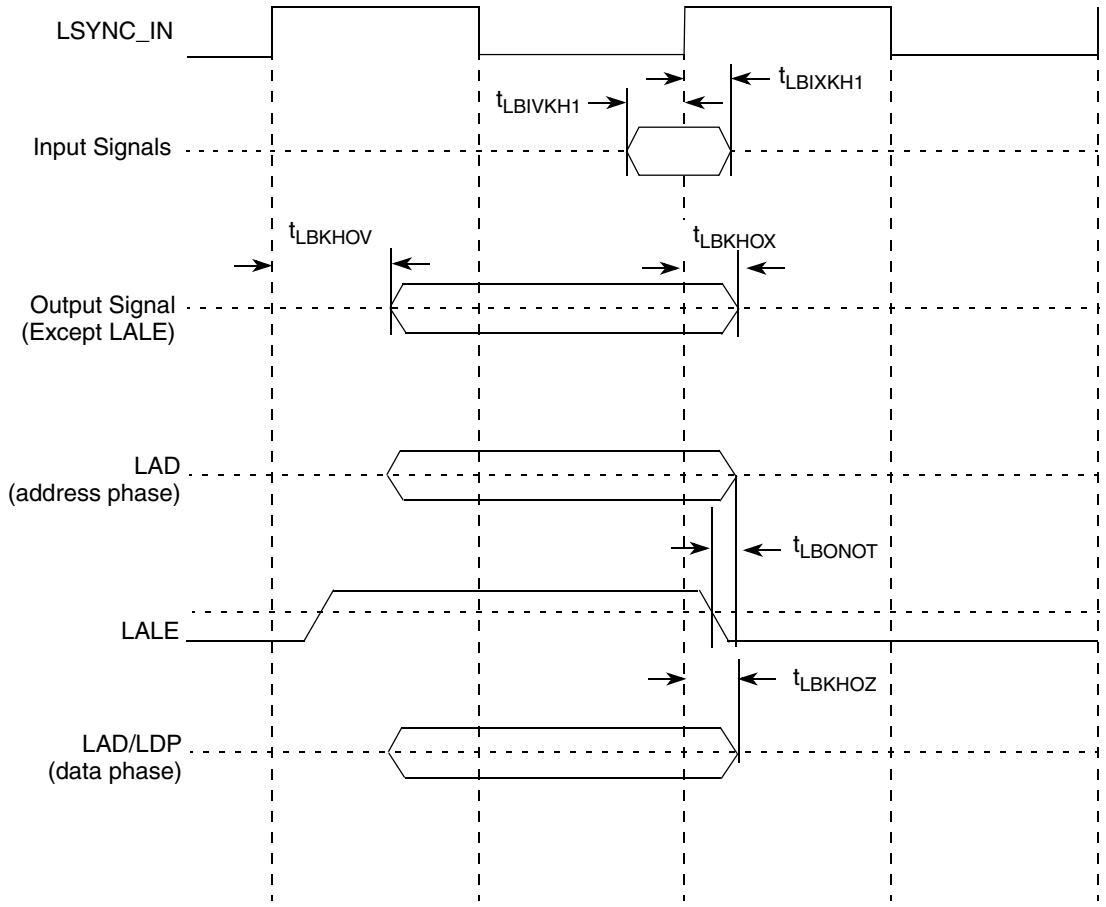


Figure 57. Local Bus AC Timing Diagram (PLL Enabled)

The above figure applies to all three controllers that eLBC supports: GPCM, UPM and FCM.

For input signals, the AC timing data is used directly for all three controllers.

2.18.2 PIC AC Timing Specifications

The following table provides the PIC input and output AC timing specifications.

Table 73. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs must be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.19 SPI Interface

This section describes the SPI DC and AC electrical specifications of the MPC8569E.

2.19.1 SPI DC Electrical Characteristics

The following table provides the SPI DC electrical characteristics.

Table 74. SPI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.19.2 SPI AC Timing Specifications

The following table and provide the SPI input and output AC timing specifications.

Table 75. SPI AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	9	ns	2
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns	2

Table 75. SPI AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns	—

Note:

1 The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load for the SPI.

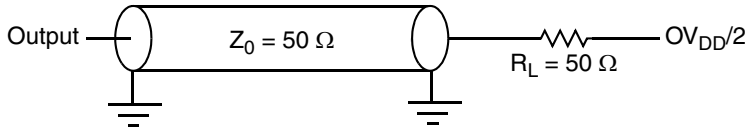
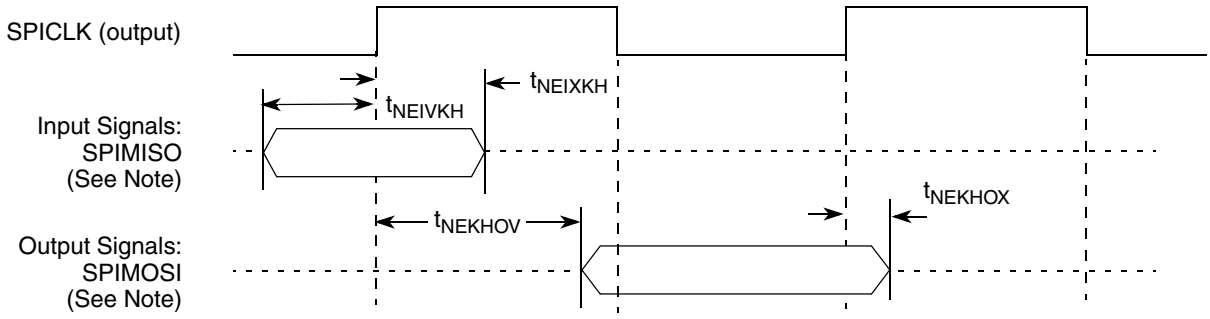


Figure 64. SPI AC Test Load

Figure 65 and Figure 66 represent the AC timing from Table 75. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 65. SPI AC Timing in Slave Mode (External Clock) Diagram

2.21 USB Interface

This section provides the AC and DC electrical specifications for the USB interface of the MPC8569E.

2.21.1 USB DC Electrical Characteristics

The following table provides the USB DC electrical characteristics.

Table 78. USB DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—
Differential input sensitivity	V_{DI}	0.2	—	V	3
Differential common mode range	V_{CM}	0.8	2.5	V	3

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.
3. Applies to low/full speed

2.21.2 USB AC Electrical Specifications

The following table describes the general USB timing specifications.

Table 79. USB General Timing Parameters

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	2
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full-speed transitions, 2
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low-speed transitions, 2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.