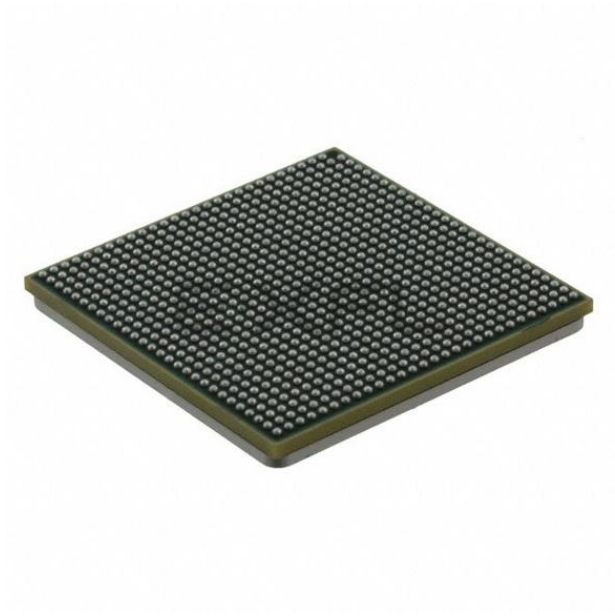

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## Understanding Embedded - Microprocessors

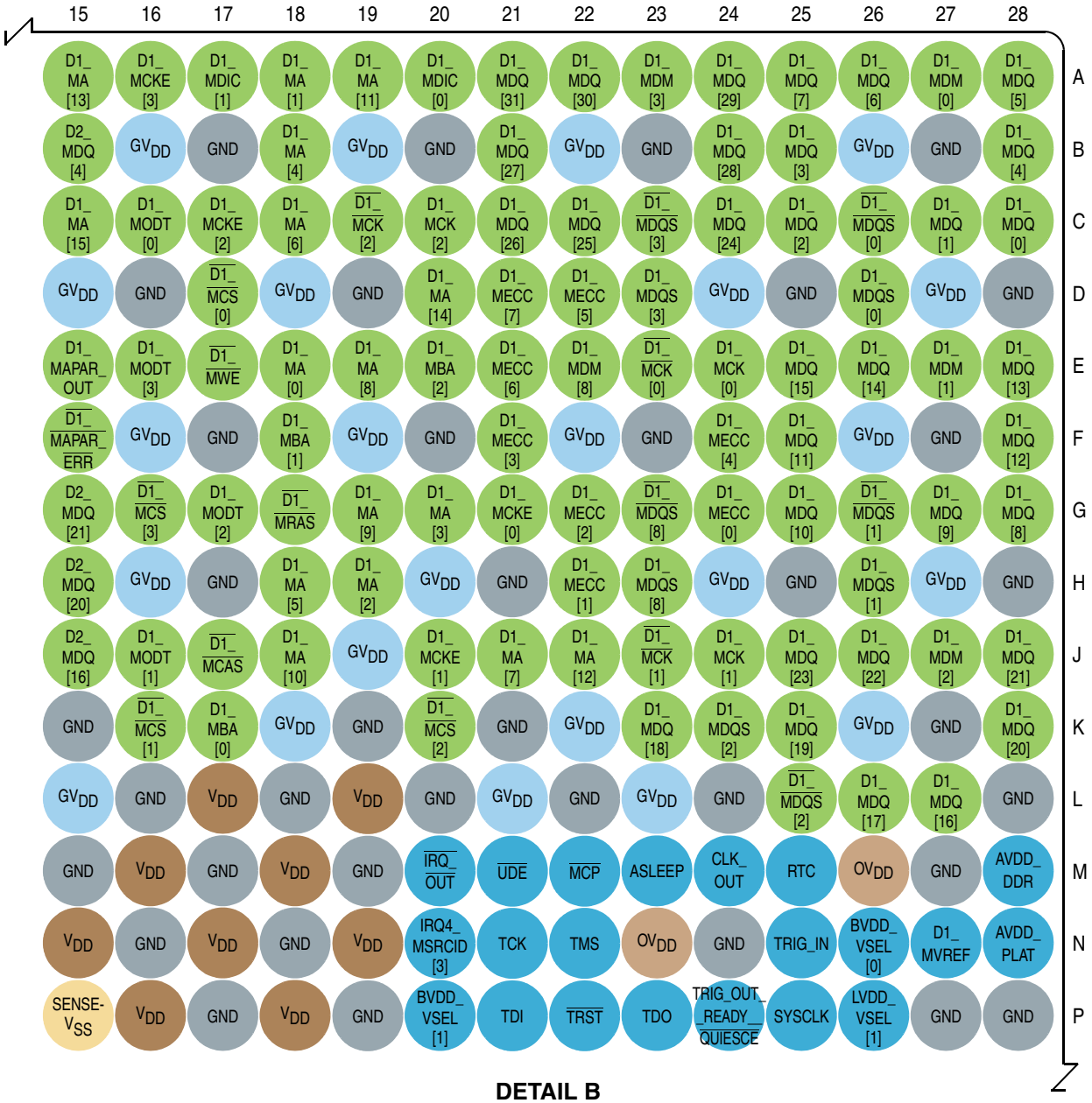
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500v2 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.067GHz |
| Co-Processors/DSP | Communications; QUICC Engine |
| RAM Controllers | DDR2, DDR3, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (8), 1Gbps (4) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.0V, 1.5V, 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8569cvtaqljb |

The following figure provides detailed view B of the MPC8569E 783-pin BGA ball map diagram.




**DETAIL B**

**Figure 4. MPC8569E Detail B Ball Map**

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| D2_MDQ28/D1_MDQ60 | B10 | I/O | $GV_{DD}$ | — |
| D2_MDQ29/D1_MDQ61 | A10 | I/O | $GV_{DD}$ | — |
| D2_MDQ30/D1_MDQ62 | A8 | I/O | $GV_{DD}$ | — |
| D2_MDQ31/D1_MDQ63 | A7 | I/O | $GV_{DD}$ | — |
| D2_MDQS0/D1_MDQS4 | C12 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MDQS0}}$/$\overline{\text{D1\_MDQS4}}$ | C13 | I/O | $GV_{DD}$ | — |
| D2_MDQS1/D1_MDQS5 | G12 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MDQS1}}$/$\overline{\text{D1\_MDQS5}}$ | F12 | I/O | $GV_{DD}$ | — |
| D2_MDQS2/D1_MDQS6 | J13 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MDQS2}}$/$\overline{\text{D1\_MDQS6}}$ | K14 | I/O | $GV_{DD}$ | — |
| D2_MDQS3/D1_MDQS7 | D9 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MDQS3}}$/$\overline{\text{D1\_MDQS7}}$ | C9 | I/O | $GV_{DD}$ | — |
| D2_MDQS8 | H9 | I/O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MDQS8}}$ | G9 | I/O | $GV_{DD}$ | — |
| D2_MECC0 | G10 | I/O | $GV_{DD}$ | — |
| D2_MECC1 | H8 | I/O | $GV_{DD}$ | — |
| D2_MECC2 | G8 | I/O | $GV_{DD}$ | — |
| D2_MECC3 | F7 | I/O | $GV_{DD}$ | — |
| D2_MECC4 | F10 | I/O | $GV_{DD}$ | — |
| D2_MECC5 | D8 | I/O | $GV_{DD}$ | — |
| D2_MECC6 | E7 | I/O | $GV_{DD}$ | — |
| D2_MECC7 | D7 | I/O | $GV_{DD}$ | — |
| D2_MODT0 | C1 | O | $GV_{DD}$ | — |
| D2_MODT1 | A3 | O | $GV_{DD}$ | — |
| D2_MODT2 | H3 | O | $GV_{DD}$ | — |
| D2_MODT3 | E1 | O | $GV_{DD}$ | — |
| D2_MAPAR_OUT | F1 | O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MAPAR\_ERR}}$ | G1 | I | $GV_{DD}$ | — |
| $\overline{\text{D2\_MRAS}}$ | G4 | O | $GV_{DD}$ | — |
| $\overline{\text{D2\_MWE}}$ | E2 | O | $GV_{DD}$ | — |
| **DMA** | | | | |
| $\overline{\text{DMA\_DACK0}}$ | AF23 | O | $OV_{DD}$ | 2 |
| $\overline{\text{DMA\_DACK1}}$/MSRCID1 | AD27 | O | $OV_{DD}$ | 11 |
| $\overline{\text{DMA\_DACK2}}$/SD_CMD | AD24 | O | $OV_{DD}$ | — |
| $\overline{\text{DMA\_DDONE0}}$ | AD25 | O | $OV_{DD}$ | 2 |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **Power Management** | | | | |
| ASLEEP | M23 | O | $OV_{DD}$ | 11 |
| **Thermal Management** | | | | |
| THERM0 | U21 | — | Internal temperature diode cathode | 32 |
| THERM1 | U20 | — | Internal temperature diode anode | 32 |
| Reserved | T22 | — | — | 9 |
| **Analog** | | | | |
| D1_MVREF | N27 | Reference voltage for DDR | $MV_{REF}$ | — |
| D2_MVREF | J1 | | | — |
| **Power and Ground** | | | | |
| $V_{DD}$ | L13 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | L17 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | L19 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | M12 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | M14 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | M16 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | M18 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | N13 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | N15 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | N17 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | N19 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | P12 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | P16 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $V_{DD}$ | Y12 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | Y14 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $V_{DD}$ | Y18 | 1.0-V/1.1-V core power supply | $V_{DD}$ | — |
| $BV_{DD}$ | AC15 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC17 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC19 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AC21 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF15 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF17 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF19 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $BV_{DD}$ | AF21 | 3.3-/2.5-/1.8-V enhanced local bus controller (eLBC) power supply | $BV_{DD}$ | — |
| $GV_{DD}$ | B12 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B16 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B19 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |
| $GV_{DD}$ | B2 | 1.8-/1.5-V DDR power supply | $GV_{DD}$ | — |

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| XGND | U24 | SerDes Transceiver Pad GND | — | — |
| XGND | V22 | SerDes Transceiver Pad GND | — | — |
| XGND | W23 | SerDes Transceiver Pad GND | — | — |
| XGND | Y21 | SerDes Transceiver Pad GND | — | — |
| AGND_SRDS | U25 | SerDes PLL GND | — | — |

**Notes:**

1. All multiplexed signals are listed only once and do not reoccur.
2. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed.
3. When configured as I2C, this pin is an open drain signal and recommend a pull-up resistor (1 kΩ) be placed on this pin to $OV_{DD}$. When configured as SD, this pin is not open drain and does not require a pull-up.
4. This pin has a weak internal pull-up resistor (~20 kΩ).
5. This pin is an open drain signal.
6. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to $OV_{DD}$.
7. This pin requires a 200-Ω pull-down to ground.
8. Do not connect.
9. Recommend a weak pull-down resistor (2–10 kΩ) be placed on this pin to GND.
10. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to $OV_{DD}$ for normal machine operation.
11. These pins must not be pulled down during power-on reset.
12. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for the required PLL filters to be attached to the $AV_{DD}$ pin.
13. These pins are connected to the $V_{DD}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. This pin selects the voltage of eLBC interface ($BV_{DD}$). This pin has internal weak pull down.
15. This pin selects the voltage of UCC1 and UCC3 interfaces ($LV_{DD}1$). This pin has internal weak pull down.
16. This pin selects the voltage of UCC2 and UCC4 interfaces ($LV_{DD}2$). This pin has internal weak pull down.
17. This pin requires a 100-Ω pull down to ground.
18. The value of LA[24:27] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
19. The value of QE_PE[27:29] during reset sets the DDR clock PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
20. The value of LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
21. The value of $\overline{\text{LCS}}$[3:7] at reset sets the QE PLL settings. These pins require 4.7-kΩ pull up or pull down resistors. See *AN4232 MPC8569E PowerQUICC III Design Checklist* for more details.
22. The value of QE_PB[27:28], QE_PC4 and QE_PD4 at reset sets the Boot ROM location. These pins require 4.7-kΩ pull up or pull down resistors. See the *MPC8569E PowerQUICC III Integrated Host Processor Family Reference Manual* for details
23. These pins are sampled at reset for general-purpose configuration use by software. The value of LAD[0:15] at reset sets the upper 16 bits of the GPPORCR
24. These pins must not be pulled up during power-on reset.
25. This output is actively driven during reset rather than being three-stated during reset.

**Table 1. MPC8569E Pinout Listing (continued)**

| Signal[1] | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|

26. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
27. When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to $GV_{DD}$ through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor and connect Dn_MDIC[1] to $GV_{DD}$ through a 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
28. Recommend a pull-up resistor (1 kΩ) to be placed on this pin to $OV_{DD}$.
29. For systems which boot from local bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.
30. If unused, these pins must be connected to GND.
31. If unused, these pins must be left unconnected.
32. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8569E. This device is currently targeted to these specifications, some of which are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the DC ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

**Table 2. Absolute Maximum Ratings[1]**

| Characteristic | Symbol | Range | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | –0.3 to 1.21 | V | — |
| PLL supply voltage | $AV_{DD}\_CORE$<br>$AV_{DD}\_DDR$,<br>$AV_{DD}\_LBIU$,<br>$AV_{DD}\_PLAT$,<br>$AV_{DD}\_QE$,<br>$AV_{DD}\_SRDS$ | –0.3 to 1.21 | V | — |
| Core power supply for SerDes transceiver | ScoreVDD | –0.3 to 1.21 | V | — |
| Pad power supply for SerDes transceiver | $XV_{DD}$ | –0.3 to 1.21 | V | — |
| DDR2 and DDR3 DRAM I/O voltage | $GV_{DD}$ | –0.3 to 1.98<br>–0.3 to 1.65 | V | 2 |
| QUICC Engine block Ethernet interface I/O voltage | $LV_{DD}1$ | –0.3 to 3.63<br>–0.3 to 2.75 | V | — |

**Table 2. Absolute Maximum Ratings[1] (continued)**

| Characteristic | | Symbol | Range | Unit | Notes |
|---|---|---|---|---|---|
| QUICC Engine block Ethernet interface I/O voltage | | $LV_{DD}2$ | –0.3 to 3.63<br>–0.3 to 2.75 | V | — |
| Debug, DMA, DUART, PIC, $I^2C$, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Enhanced local bus I/O voltage | | $BV_{DD}$ | –0.3 to 3.63<br>–0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Input voltage | DDR2/DDR3 DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 3 |
| | DDR2/DDR3 DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | — |
| | Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}n$ + 0.3) | V | 3 |
| | Enhanced local bus signals | $BV_{IN}$ | –0.3 to ($BV_{DD}$ + 0.3) | — | 3 |
| | Debug, DMA, DUART, PIC, $I^2C$, JTAG, power management, QUICC Engine block, eSDHC, GPIO, clocking, SPI, I/O voltage select and system control I/O voltage | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3 |
| | SerDes signals | $XV_{IN}$ | –0.3 to ($XV_{DD}$ + 0.3) | V | — |
| Storage junction temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. The –0.3 to 1.98 V range is for DDR2, and the –0.3 to 1.65 V range is for DDR3.
3. **Caution:** (B,M,L,O,X)$V_{IN}$ must not exceed (B,G,L,O,X)$V_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

### 2.1.1.1 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Proper device operation outside these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 1.0 V ± 30 mV<br>1.1 V ± 33 mV | V | 1 |
| PLL supply voltage | $AV_{DD}$_CORE,<br>$AV_{DD}$_DDR,<br>$AV_{DD}$_LBIU,<br>$AV_{DD}$_PLAT,<br>$AV_{DD}$_QE,<br>$AV_{DD}$_SRDS | 1.0 V ± 30 mV<br>1.1 V ± 33 mV | V | 2 |

The following figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

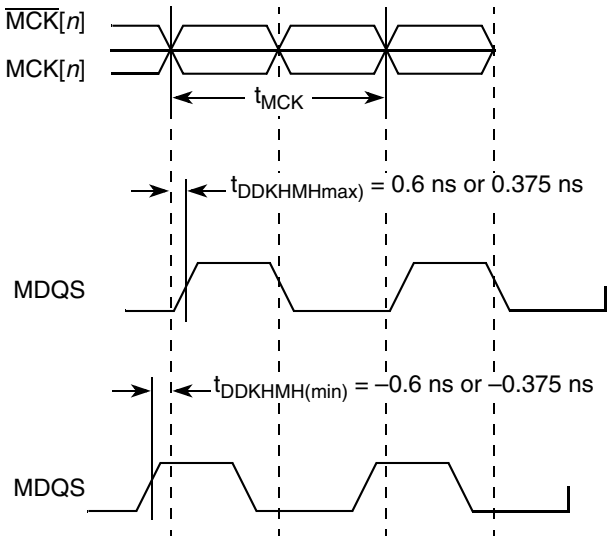



**Figure 9. Timing Diagram for $t_{DDKHMH}$**

The following figure shows the DDR2 and DDR3 SDRAM output timing diagram.

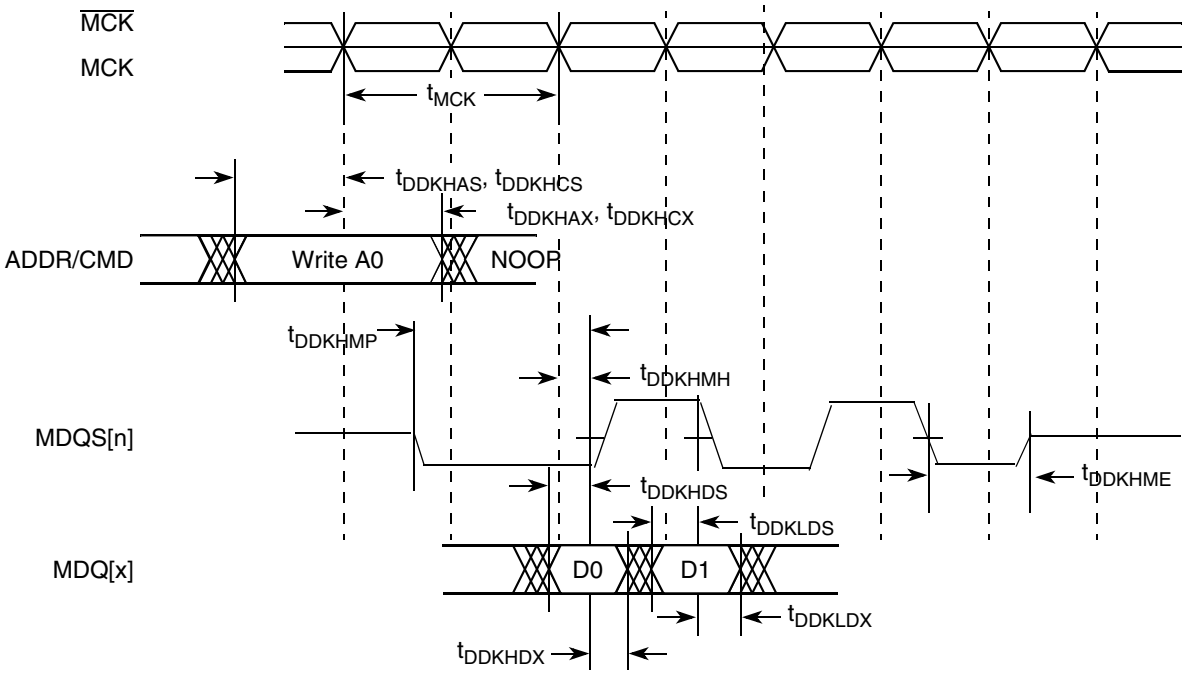



**Figure 10. DDR2 and DDR3 Output Timing Diagram**

**Table 31. RMII Receive AC Timing Specifications (continued)**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Fall time REF_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 4.0 | ns | 1 |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns | — |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns | — |

**Note:**

1. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The following figure provides the AC test load.

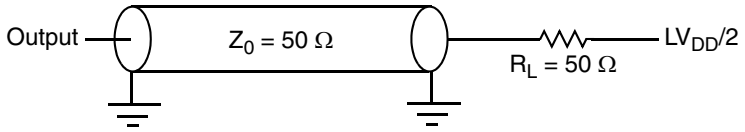



**Figure 20. AC Test Load**

The following figure shows the RMII receive AC timing diagram.

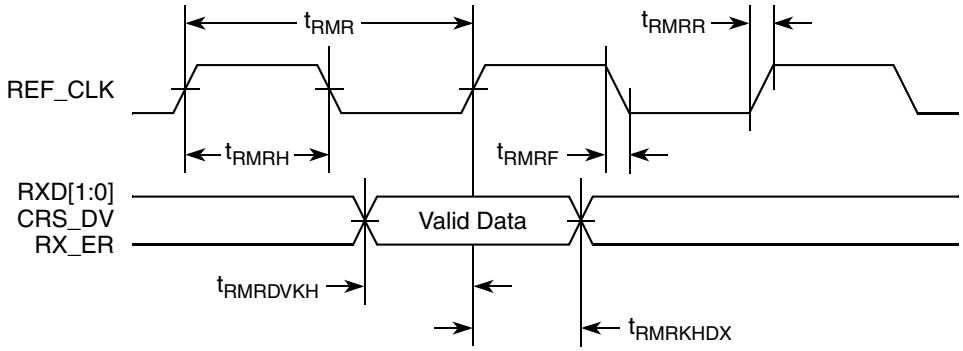



**Figure 21. RMII Receive AC Timing Diagram**

## 2.6.3.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

The following figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

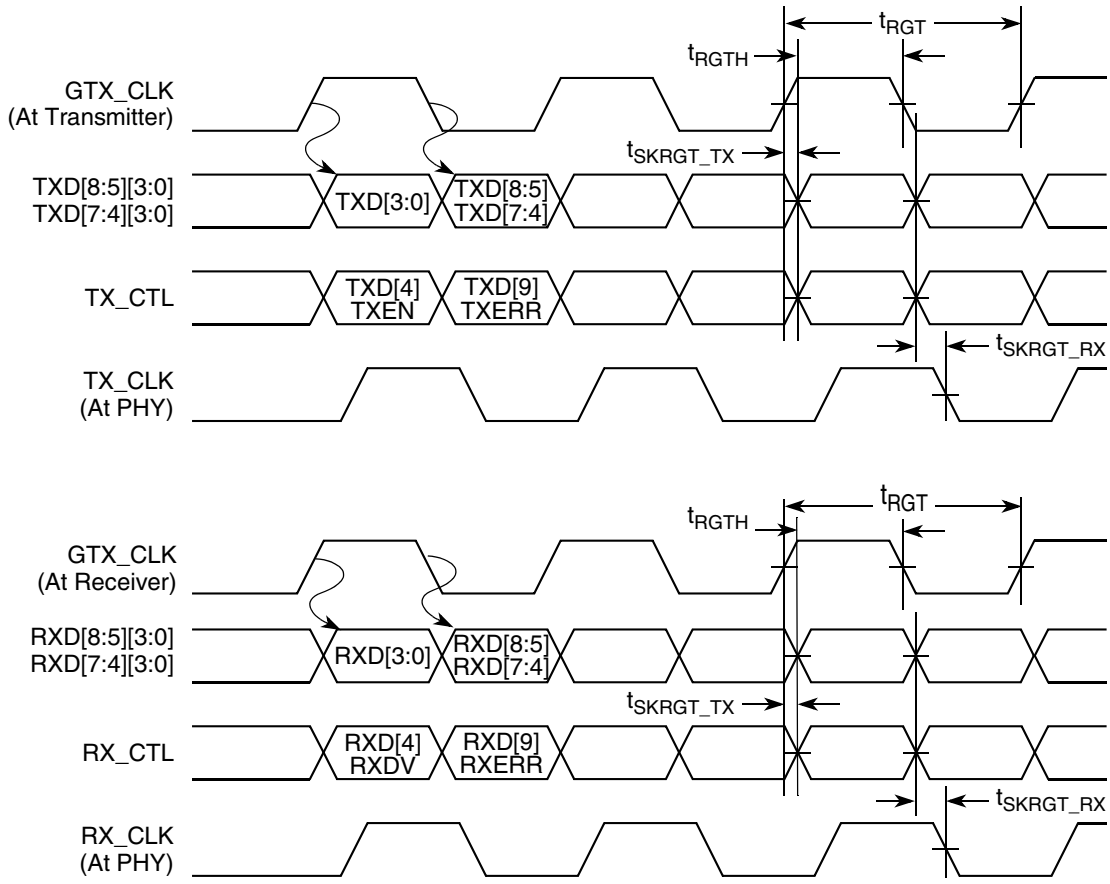



**Figure 26. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 2.6.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of MPC8569E as shown in Figure 27, where $C_{TX}$ is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 45.

### 2.6.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

#### 2.6.4.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.9.2.3, “DC Level Requirement for SerDes Reference Clocks.”

### 2.6.4.2.2 SGMII Transmit AC Timing Specifications

The following table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

**Table 38. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with $XV_{DD}$ = 1.0 V ± 3% and 1.1 V ± 3%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic jitter | JD | — | — | 0.17 | UI p-p | — |
| Total jitter | JT | — | — | 0.35 | UI p-p | 2 |
| Unit interval | UI | 799.92 | 800 | 800.08 | ps | 1 |
| AC coupling capacitor | $C_{TX}$ | 10 | — | 200 | nF | 3 |

**Notes:**
1. Each UI is 800 ps ± 100 ppm.
2. See Figure 30 for single frequency sinusoidal jitter limits.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

### 2.6.4.2.3 SGMII AC Measurement Details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$), as depicted in the following figure, respectively.

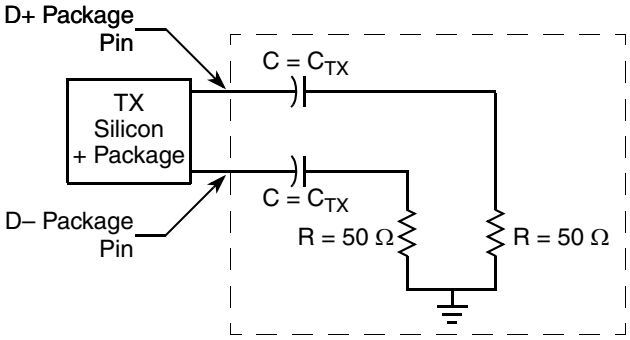



**Figure 29. SGMII AC Test/Measurement Load**

#### 2.6.4.2.4 SGMII Receiver AC Timing Specifications

The following table provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

**Table 39. SGMII Receive AC Timing Specifications**

At recommended operating conditions with $XV_{DD}$ = 1.0 V ± 3%. and 1.1 V ± 3%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1, 2, 4 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1, 2, 4 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1, 2, 4 |
| Bit Error Ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit Interval | UI | 799.92 | 800.00 | 800.08 | ps | 3 |

**Notes:**
1. Measured at receiver.
2. See *RapidIO 1x/4x LP Serial Physical Layer Specification* for interpretation of jitter specifications.
3. Each UI is 800 ps ± 100 ppm.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of the following figure.

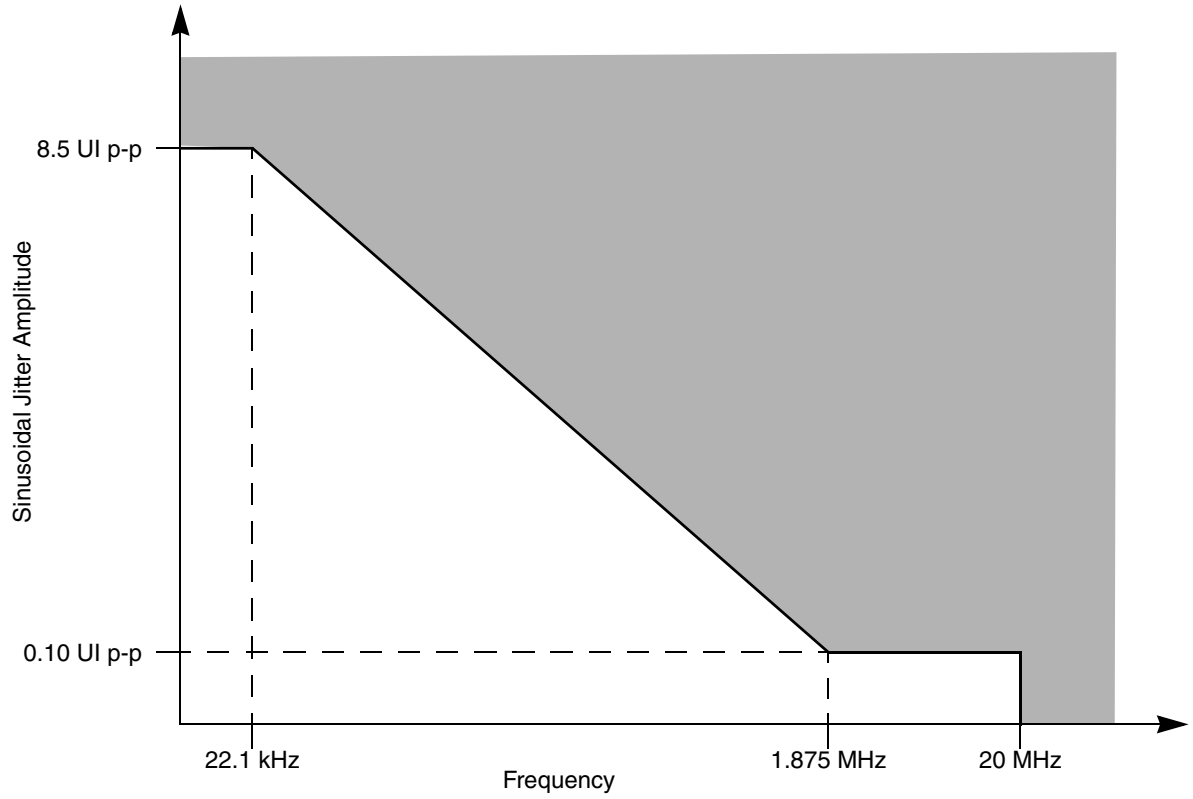



**Figure 30. Single Frequency Sinusoidal Jitter Limits**

## 2.6.5 QUICC Engine Block IEEE 1588 Electrical Characteristics

### 2.6.5.1 QUICC Engine Block IEEE 1588 DC Specifications

The following table shows the QUICC Engine block IEEE 1588 DC specifications when operating from a 3.3 V supply.

**Table 40. QUICC Engine Block IEEE 1588 DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ = 3.3 V

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($V_{IN}$ = $OV_{DD}$) | $I_{IH}$ | — | 40 | μA | 2 |
| Input low current ($V_{IN}$ = GND) | $I_{IL}$ | –600 | — | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –4.0 mA) | $V_{OH}$ | 2.1 | $OV_{DD}$ + 0.3 | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 4.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |

**Note:**

1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbols referenced in Table 2 and Table 3.

### 2.6.5.2 QUICC Engine Block IEEE 1588 AC Specifications

The following table provides the QUICC Engine block IEEE 1588 AC timing specifications.

**Table 41. QUICC Engine Block IEEE 1588 AC Timing Specifications**

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| QE_1588_CLK clock period | $t_{T1588CLK}$ | 3.8 | — | $T_{RX\_CLK} \times 7$ | ns | 1, 3 |
| QE_1588_CLK duty cycle | $t_{T1588CLKH}/t_{T1588CLK}$ | 40 | 50 | 60 | % | 5 |
| QE_1588_CLK peak-to-peak jitter | $t_{T1588CLKINJ}$ | — | — | 250 | ps | 5 |
| Rise time QE_1588_CLK (20%–80%) | $t_{T1588CLKINR}$ | 1.0 | — | 2.0 | ns | 5 |
| Fall time QE_1588_CLK (80%–20%) | $t_{T1588CLKINF}$ | 1.0 | — | 2.0 | ns | 5 |
| QE_1588_CLK_OUT clock period | $t_{T1588CLKOUT}$ | $2 \times t_{T1588CLK}$ | — | — | ns | — |
| QE_1588_CLK_OUT duty cycle | $t_{T1588CLKOTH}/t_{T1588CLKOUT}$ | 30 | 50 | 70 | % | — |
| QE_1588_PPS_OUT | $t_{T1588OV}$ | 0.5 | — | 4.0 | ns | — |

**Table 45. HDLC, BISYNC, and Transparent AC Timing Specifications (continued)**

For recommended operating conditions, see Table 3

| Characteristic | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Inputs—External clock input setup time | $t_{HEIVKH}$ | 4 | — | ns | — |
| Inputs—Internal clock input hold time | $t_{HIIXKH}$ | 0 | — | ns | — |
| Inputs—External clock input hold time | $t_{HEIXKH}$ | 1.3 | — | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{HIKHOX}$ symbolizes the outputs internal timing (HI) for the time $t_{serial}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following table provides the input and output AC timing specifications for the synchronous UART protocols.

**Table 46. Synchronous UART AC Timing Specifications**

For recommended operating conditions, see Table 3

| Characteristic | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Outputs—Internal clock delay | $t_{HIKHOV}$ | 0 | 11 | ns | 2 |
| Outputs—External clock delay | $t_{HEKHOV}$ | 1 | 14 | ns | 2 |
| Outputs—Internal clock high Impedance | $t_{HIKHOX}$ | 0 | 11 | ns | 2 |
| Outputs—External clock high Impedance | $t_{HEKHOX}$ | 1 | 14 | ns | 2 |
| Inputs—Internal clock input setup time | $t_{HIIVKH}$ | 10 | — | ns | — |
| Inputs—External clock input setup time | $t_{HEIVKH}$ | 8 | — | ns | — |
| Inputs—Internal clock input hold time | $t_{HIIXKH}$ | 0 | — | ns | — |
| Inputs—External clock input hold time | $t_{HEIXKH}$ | 1 | — | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{HIKHOX}$ symbolizes the outputs internal timing (HI) for the time $t_{serial}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

The following figure provides the AC test load.

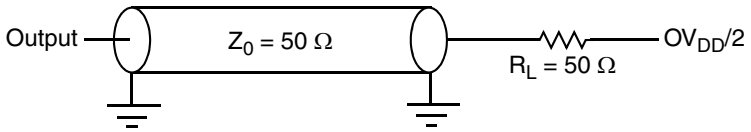



**Figure 35. AC Test Load**

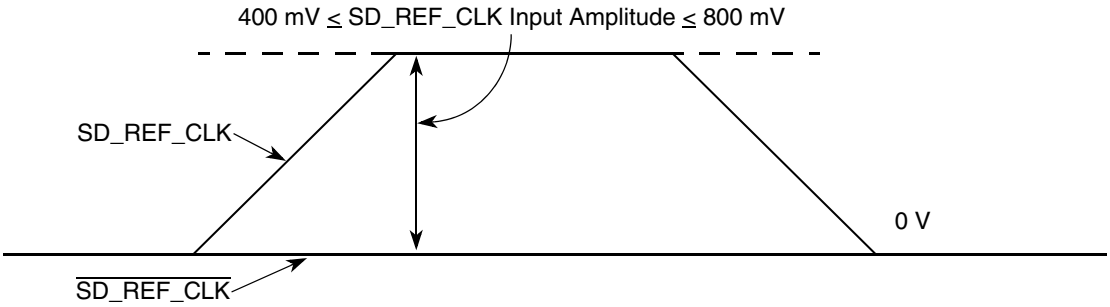



**Figure 42. Single-Ended Reference Clock Input DC Requirements**

### 2.9.2.4 AC Requirements for SerDes Reference Clocks

The following table lists AC requirements for the PCI Express, SGMII, and Serial RapidIO SerDes reference clocks to be guaranteed by the customer's application design.

**Table 48. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements**

At recommended operating conditions with ScoreVDD = 1.0 V ± 3%. and 1.1 V ± 3%

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | –350 | — | 350 | ppm | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | 7 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at $10^{-6}$ BER | $t_{CLK\_DJ}$ | — | — | 42 | ps | 7 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at $10^{-6}$ BER (peak-to-peak jitter at refClk input) | $t_{CLK\_TJ}$ | — | — | 86 | ps | 2, 7 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate | $t_{CLKRR}/t_{CLKFR}$ | 1 | — | 4 | V/ns | 3, 7 |

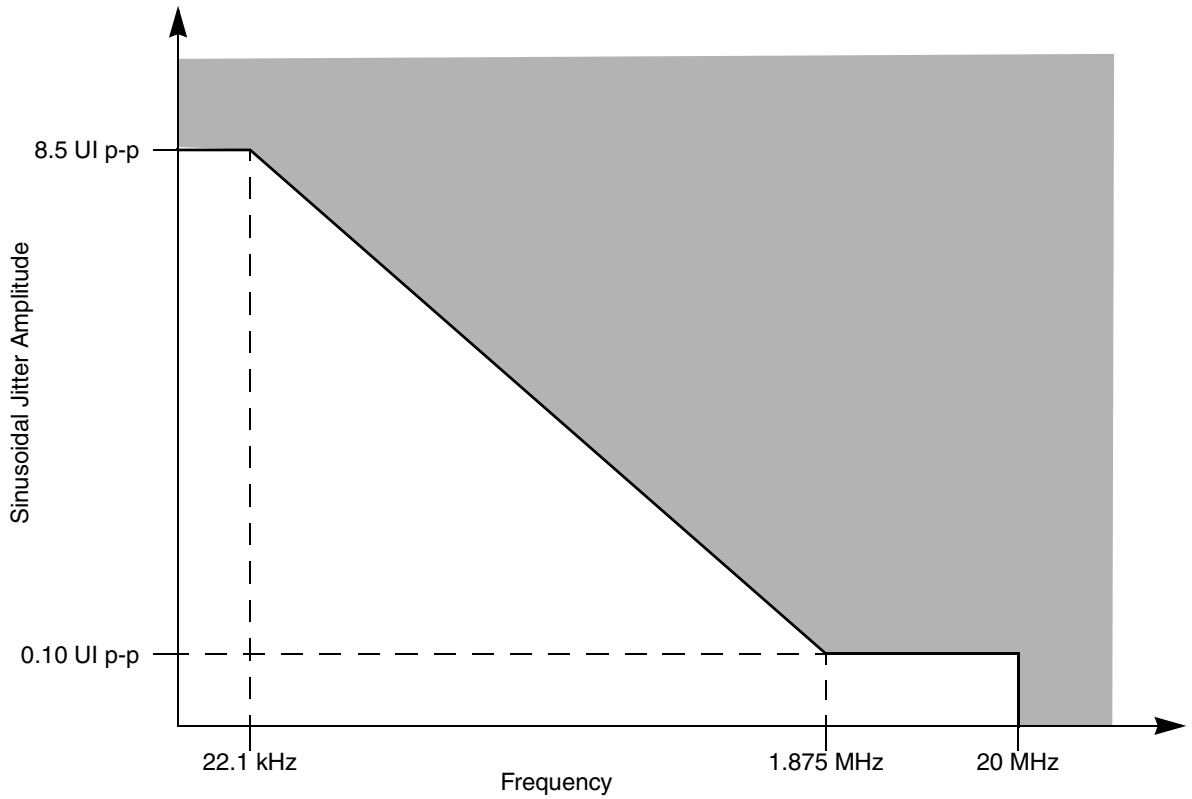



**Figure 48. Single Frequency Sinusoidal Jitter Limits**

## 2.12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8569E.

### 2.12.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface.

**Table 57. I²C DC Electrical Characteristics**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | 0 | 0.4 | V | 2 |

The following figure shows the AC timing diagram for PLL bypass mode.

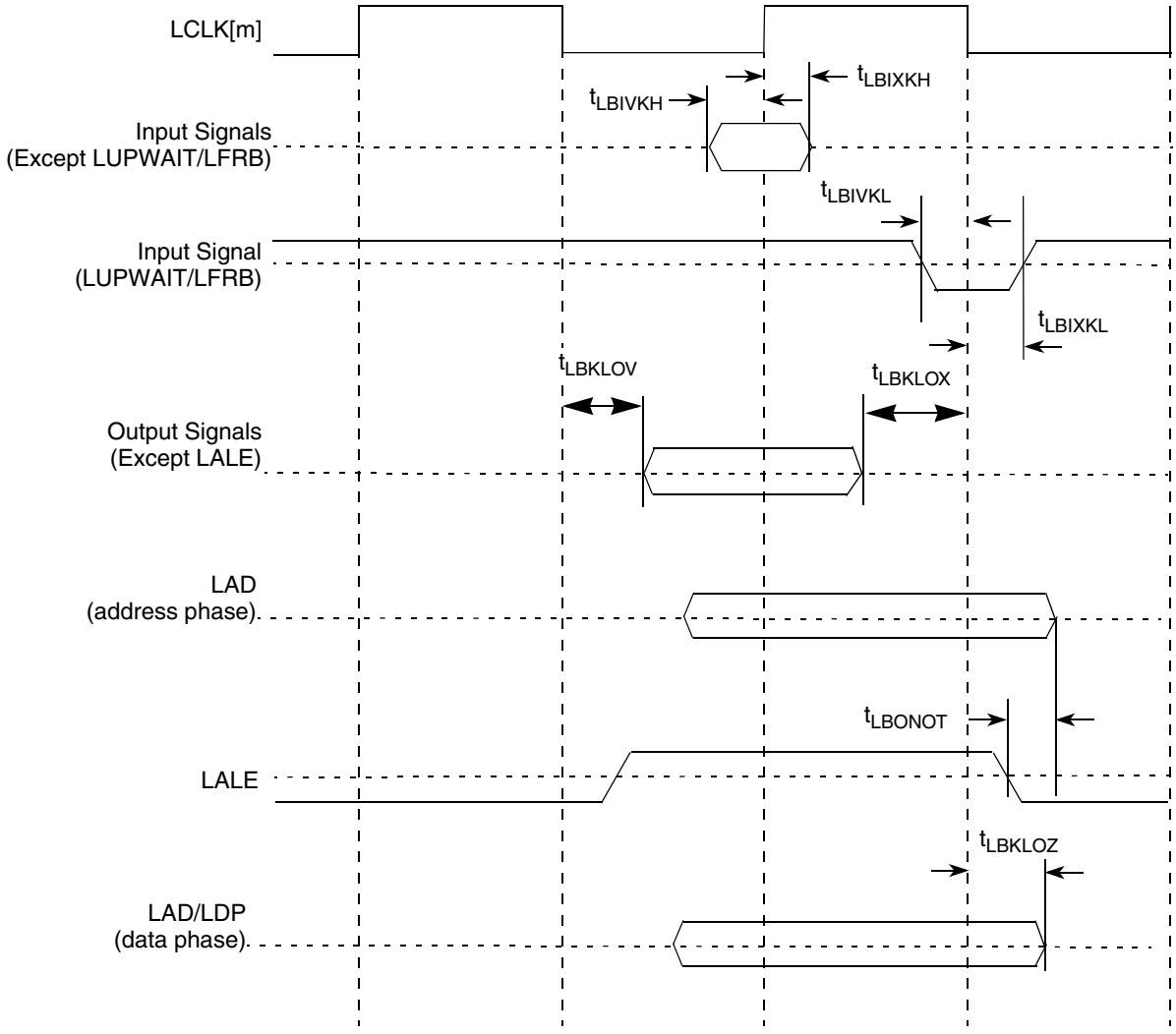



**Figure 59. Enhanced Local Bus Signals (PLL Bypass Mode)**

The above figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by $t_{acs}$ (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

### 2.17.2 Timers AC Timing Specifications

The following table provides the timers input and output AC timing specifications.

**Table 71. Timers Input AC Timing Specifications**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Typ | Unit | Notes |
|---|---|---|---|---|
| Timers inputs—minimum pulse width | $t_{TIWID}$ | 20 | ns | 1, 2 |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs must be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least $t_{TIWID}$ ns to ensure proper operation.

The following figure provides the AC test load for the timers.

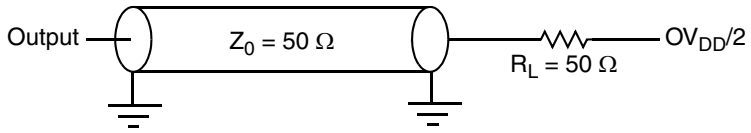



**Figure 63. Timers AC Test Load**

## 2.18 Programmable Interrupt Controller (PIC)

This section describes the DC and AC electrical specifications for the PIC of the MPC8569E.

### 2.18.1 PIC DC Electrical Characteristics

The following table provides the DC electrical characteristics for the external interrupt pins $\overline{IRQ}[0:6]$, $\overline{IRQ}[8:11]$ and $\overline{IRQ\_OUT}$ of the PIC, as well as the port interrupts of the QUICC Engine block.

**Table 72. PIC DC Electrical Characteristics**

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.8 | V | 1 |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±40 | μA | 2 |
| Output high voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Output low voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $OV_{IN}$ values found in Table 3.
2. The symbol $OV_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

**Table 81. UTOPIA/POS AC Timing Specifications[1] (continued)**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| UTOPIA/POS inputs—External clock input setup time | $t_{UEIVKH}$ | 4.0 | — | ns |
| UTOPIA/POS inputs—Internal clock input hold time | $t_{UIIXKH}$ | 0 | — | ns |
| UTOPIA/POS inputs—External clock input hold time | $t_{UEIXKH}$ | 1.2 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{UIKHOX}$ symbolizes the UTOPIA/POS outputs internal timing (UI) for the time $t_{Utopia}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the UTOPIA/POS.

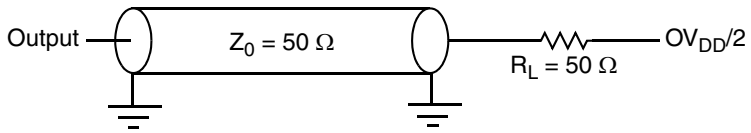



**Figure 70. UTOPIA/POS AC Test Load**

Figure 71 and Figure 72 represent the AC timing from Table 81. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the UTOPIA/POS timing with external clock.

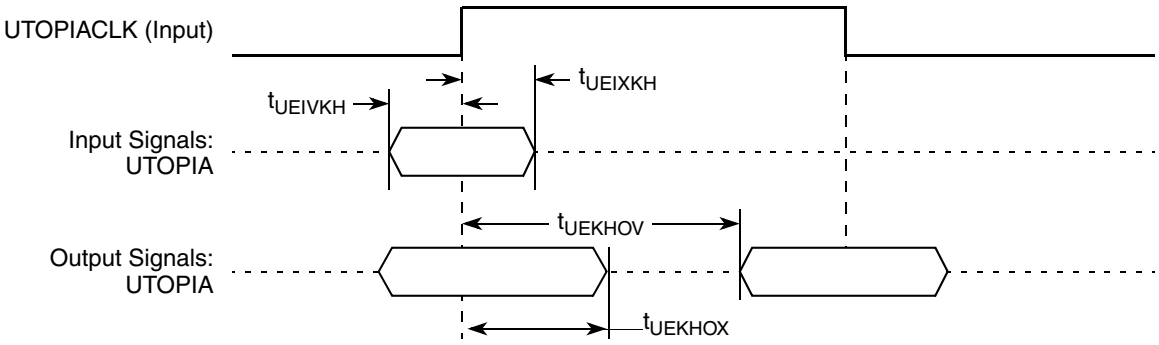



**Figure 71. UTOPIA/POS AC Timing (External Clock) Diagram**

The following figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

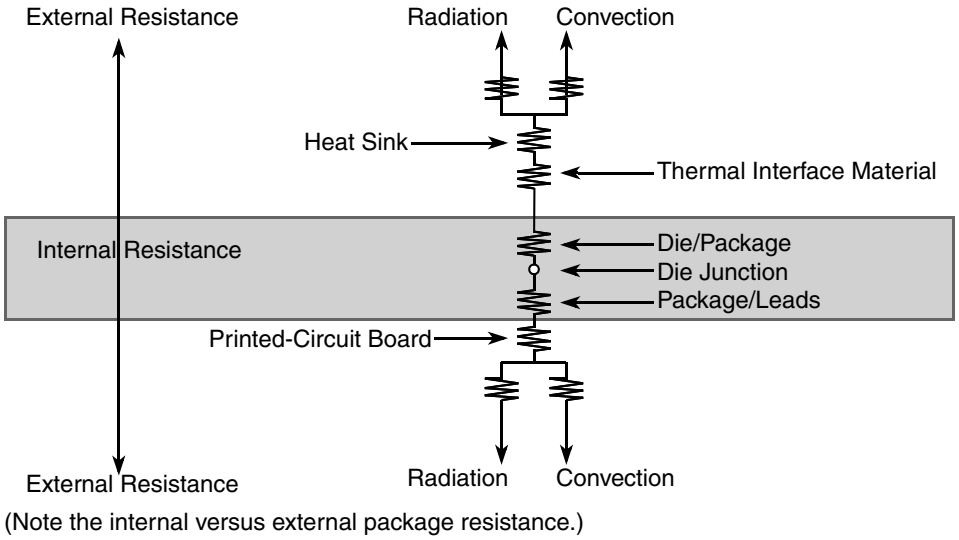



**Figure 74. Package with Heat Sink Mounted to a Printed-Circuit Board**

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and the heat sink attach material (or thermal interface material), and to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

### 3.3.2 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increased contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 73).

The system board designer can choose among several types of commercially-available thermal interface materials.

### 3.3.3 Temperature Diode

The device has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the MPC8569E on-board temperature diode:

Operating range: 10 – 230 μA

Ideality factor over 13.5 – 220 μA; n = 1.006 +/- 0.008

# 4 Package Description

The following section describes the detailed content and mechanical description of the package.